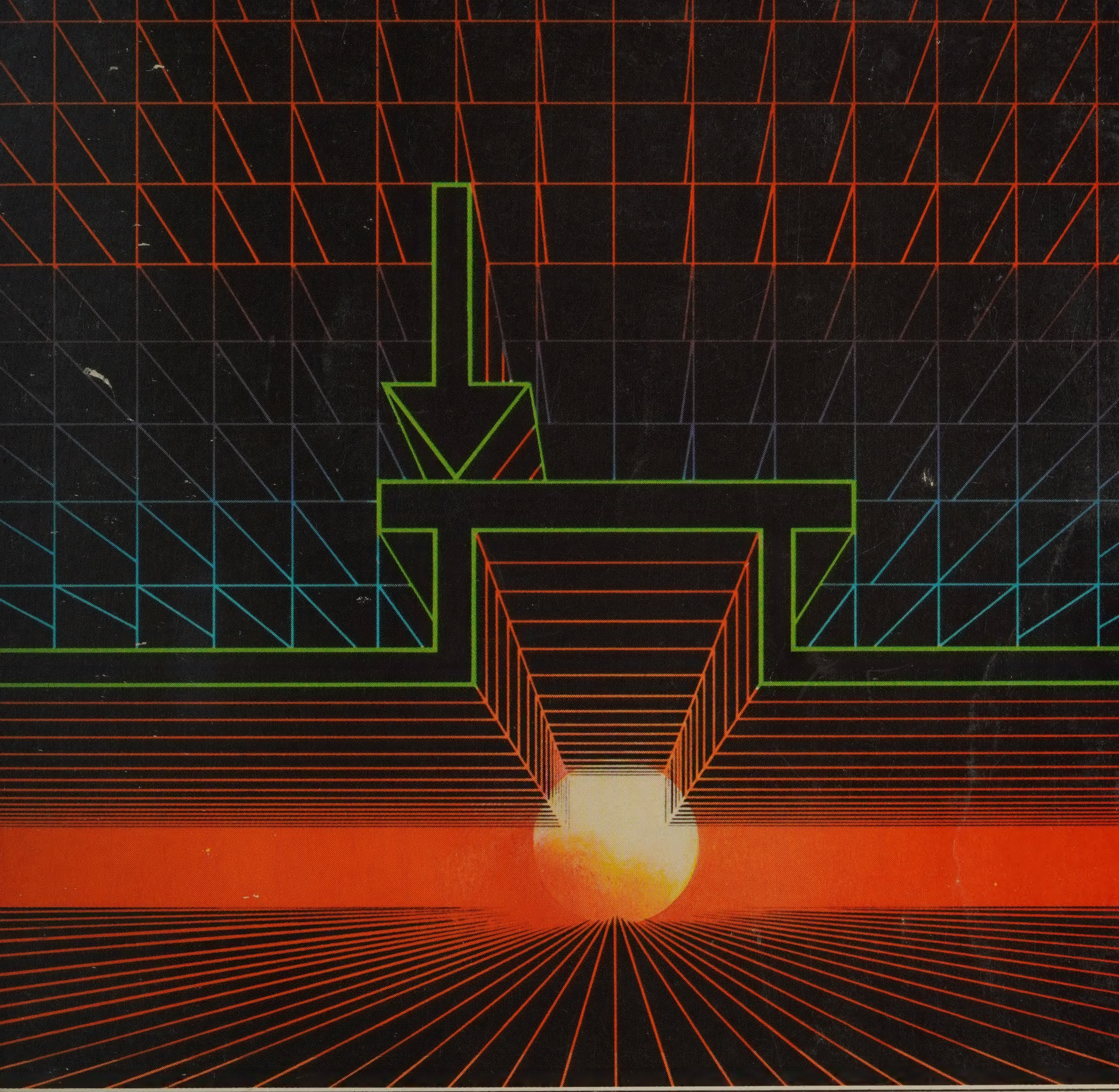

small signal

FET design catalog

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July 1983

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FET
Design Catalog
July 1983

Product Status and Definitions

DATA SHEET IDENTIFICATION	PRODUCT STATUS	DEFINITION
Preliminary	First Production	Data sheet finalized and limited production quantities available. Initial reliability and characterization curves available.
No Identification Noted	Full Production	Data sheet finalized and application information available. Sampling and production order subject to product demand and manufacturing availability.

NOTE: Siliconix reserves the right to make changes at any time without notice in order to improve design and supply the best product possible

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How to Use the FET Cross Reference *and* Index

The following examples illustrate how the FET Cross Reference and Index should be used:

Case (1) Recommended replacement offered by Siliconix is identical to Industry Part Number.

Industry Part Number	Type and Classification	Recommended Replacement
2N4391	N JFET	2N4391

Case (2) Recommended replacement offered by Siliconix is not identical to Industry Part Number.

Industry Part Number	Type and Classification	Recommended Replacement
2N3457	N JFET	2N4338

The recommended replacement may be exact, tighter or looser on electrical characteristics, and may be a different package or pin-out. Data sheets for both parts should, if possible, be reviewed for a complete comparison. Send for *your* new November, 1982 Small Signal FET Design Catalog.

Type and classification abbreviations are described as follows:

BF	(JFET Plastic)
CR	(Current Limited)
CRR	(Current Limiter)
D	(Dual)
DN	(Dual N-Channel Metal Can)
DPAD	(Dual Pico Ampere Diode)
FN	(N-Channel Metal Can)
ENH	(Enhancement-Mode Normally-Off)
JPAD	(Plastic Pico Ampere Diode)
JR	(Plastic High Voltage Diode)
N	(N-Channel)
P	(P-Channel)
PAD	(Pico Ampere Diode)
SD	(N-Channel Enhancement-Mode DMOS)
MOSPOWER	
M	(N-Channel Enhancement-Mode MOS-FET)

FET Cross Reference

Industry Part Number	Type and Classification	Recommended Replacement
1N5283	CL N JFET	CR022
1N5284	CL N JFET	CR024
1N5285	CL N JFET	CR027
1N5286	CL N JFET	CR030
1N5287	CL N JFET	CR033
1N5288	CL N JFET	CR039
1N5289	CL N JFET	CR043
1N5290	CL N JFET	CR047
1N5291	CL N JFET	CR056
1N5292	CL N JFET	CR062
1N5293	CL N JFET	CR068
1N5294	CL N JFET	CR075
1N5295	CL N JFET	CR082
1N5296	CL N JFET	CR091
1N5297	CL N JFET	CR100
1N5298	CL N JFET	CR110
1N5299	CL N JFET	CR120
1N5300	CL N JFET	CR130
1N5301	CL N JFET	CR140
1N5302	CL N JFET	CR150
1N5303	CL N JFET	CR160
1N5304	CL N JFET	CR180
1N5305	CL N JFET	CR200
1N5306	CL N JFET	CR220
1N5307	CL N JFET	CR240
1N5308	CL N JFET	CR270
1N5309	CL N JFET	CR300
1N5310	CL N JFET	CR330
1N5311	CL N JFET	CR360
1N5312	CL N JFET	CR390
1N5313	CL N JFET	CR430
1N5314	CL N JFET	CR470
2N2386	P JFET	2N2609
2N2386A	P JFET	2N2609
2N2497	P JFET	2N3329
2N2498	P JFET	2N3330
2N2499	P JFET	2N3331
2N2500	P JFET	2N3332
2N2609	P JFET	2N2609
2N2609JAN	P JFET	2N2609JAN
2N2841	P JFET	2N3329
2N2842	P JFET	2N3329
2N2843	P JFET	2N3329
2N2844	P JFET	2N2608
2N3066	N JFET	2N4340
2N3067	N JFET	2N4338
2N3068	N JFET	2N4338
2N3069	N JFET	2N4341
2N3070	N JFET	2N4339
2N3071	N JFET	2N4338
2N3084	N JFET	2N4341
2N3085	N JFET	2N4341
2N3086	N JFET	2N4341
2N3087	N JFET	2N4341

Industry Part Number	Type and Classification	Recommended Replacement
2N3088	N JFET	2N4339
2N3088A	N JFET	2N4339
2N3089	N JFET	2N4339
2N3089A	N JFET	2N4339
2N3113	P JFET	2N3329
2N3277	P JFET	2N2608
2N3278	P JFET	2N2608
2N3328	P JFET	2N3438
2N3329	P JFET	2N3329
2N3330	P JFET	2N3330
2N3331	P JFET	2N2609
2N3332	P JFET	2N2609
2N3365	N JFET	2N4340
2N3366	N JFET	2N4338
2N3367	N JFET	2N4338
2N3368	N JFET	2N4341
2N3369	N JFET	2N4340
2N3370	N JFET	2N4339
2N3376	P JFET	2N3329
2N3378	P JFET	2N3330
2N3380	P JFET	2N3331
2N3382	P JFET	2N3382
2N3384	P JFET	2N3384
2N3386	P JFET	2N3386
2N3436	N JFET	2N4341
2N3437	N JFET	2N4341
2N3438	N JFET	2N4341
2N3452	N JFET	2N4340
2N3453	N JFET	2N4338
2N3454	N JFET	2N4338
2N3455	N JFET	2N4340
2N3456	N JFET	2N4338
2N3457	N JFET	2N4338
2N3458	N JFET	2N4341
2N3459	N JFET	2N4341
2N3460	N JFET	2N4340
2N3574	P JFET	2N3329
2N3575	P JFET	2N3329
2N3578	P JFET	2N2608
2N3608	P MOS ENH	3N163
2N3684	N JFET	2N4339
2N3685	N JFET	2N4339
2N3686	N JFET	2N4340
2N3687	N JFET	2N2609
2N3819	N JFET	2N3819
2N3820	P JFET	J270
2N3821	N JFET	2N3821
2N3822	N JFET	2N3822
2N3823	N JFET	2N3823
2N3824	N JFET	2N3824
2N3909	P JFET	2N2608
2N3909A	P JFET	2N3909
2N3921	D N JFET	2N3921
2N3922	D N JFET	2N3922
2N3954	D N JFET	2N3954

Industry Part Number	Type and Classification	Recommended Replacement
2N3954A	D N JFET	2N3954A
2N3955	D N JFET	2N3955
2N3955A	D N JFET	2N3955A
2N3956	D N JFET	2N3956
2N3957	D N JFET	2N3957
2N3958	D N JFET	2N3958
2N3966	N JFET	2N3966
2N3967	N JFET	2N4221
2N3967A	N JFET	2N4221
2N3968	N JFET	2N4339
2N3968A	N JFET	2N4339
2N3969	N JFET	2N4339
2N3969A	N JFET	2N3686
2N3970	N JFET	2N3970
2N3971	N JFET	2N3971
2N3972	N JFET	2N3972
2N3993	P JFET	2N3386
2N3993A	P JFET	2N3386
2N3994	P JFET	2N3382
2N3994A	P JFET	2N3382
2N4084	D N JFET	2N4084
2N4085	D N JFET	2N4085
2N4091	N JFET	2N4091
2N4091A	N JFET	2N4091
2N4092	N JFET	2N4092
2N4092A	N JFET	2N4092
2N4093	N JFET	2N4093
2N4093A	N JFET	2N4093
2N4117	N JFET	2N4117
2N4117A	N JFET	2N4117A
2N4118	N JFET	2N4118
2N4118A	N JFET	2N4118A
2N4119	N JFET	2N4119
2N4119A	N JFET	2N4119A
2N4120	P MOS ENH	3N163
2N4139	N JFET	2N3822
2N4220	N JFET	2N4220
2N4220A	N JFET	2N4220A
2N4221	N JFET	2N4221
2N4221A	N JFET	2N4221A
2N4222	N JFET	2N4222
2N4222A	N JFET	2N4222A
2N4223	N JFET	2N4223
2N4224	N JFET	2N4224
2N4267	P MOS ENH	3N163
2N4302	N JFET	PN4302-18
2N4303	N JFET	PN4303-18
2N4304	N JFET	PN4304-18
2N4338	N JFET	2N4338
2N4339	N JFET	2N4339
2N4340	N JFET	2N4340
2N4341	N JFET	2N4341
2N4352	P MOS ENH	3N163
2N4381	P JFET	2N2609
2N4382	P JFET	2N5115

FET Cross Reference (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement
2N4391	N JFET	2N4391
2N4392	N JFET	2N4392
2N4393	N JFET	2N4393
2N4416	N JFET	2N4416
2N4416A	N JFET	2N4416A
2N4445	N JFET	2N5432
2N4446	N JFET	2N5433
2N4447	N JFET	2N5432
2N4448	N JFET	2N5433
2N4856	N JFET	2N4856
2N4856A	N JFET	2N4856A
2N4856JAN	N JFET	2N4856JAN
2N4856JANTX	N JFET	2N4856JANTX
2N4856JANTXV	N JFET	2N4856JANTXV
2N4857	N JFET	2N4857
2N4857A	N JFET	2N4857A
2N4857JAN	N JFET	2N4857JAN
2N4857JANTX	N JFET	2N4857JANTX
2N4857JANTXV	N JFET	2N4857JANTXV
2N4858	N JFET	2N4858
2N4858A	N JFET	2N4858A
2N4858JAN	N JFET	2N4858JAN
2N4858JANTX	N JFET	2N4858JANTX
2N4858JANTXV	N JFET	2N4858JANTXV
2N4859	N JFET	2N4859
2N4859A	N JFET	2N4859A
2N4859JAN	N JFET	2N4859JAN
2N4859JANTX	N JFET	2N4859JANTX
2N4859JANTXV	N JFET	2N4859JANTXV
2N4860	N JFET	2N4860
2N4860A	N JFET	2N4860A
2N4860JAN	N JFET	2N4860JAN
2N4860JANTX	N JFET	2N4860JANTX
2N4860JANTXV	N JFET	2N4860JANTXV
2N4861	N JFET	2N4861
2N4861A	N JFET	2N4861A
2N4861JAN	N JFET	2N4861JAN
2N4861JANTX	N JFET	2N4861JANTX
2N4861JANTXV	N JFET	2N4861JANTXV
2N4867	N JFET	2N4867
2N4867A	N JFET	2N4867A
2N4868	N JFET	2N4868
2N4868A	N JFET	2N4868A
2N4869	N JFET	2N4869
2N4869A	N JFET	2N4869A
2N4977	N JFET	2N5432
2N4978	N JFET	2N5433
2N4979	N JFET	2N5434
2N5018	P JFET	2N5018
2N5019	P JFET	2N5019
2N5020	P JFET	2N3329
2N5021	P JFET	2N2608
2N5033	P JFET	2N2608
2N5045	D N JFET	2N5045
2N5046	D N JFET	2N5046

Industry Part Number	Type and Classification	Recommended Replacement
2N5047	D N JFET	2N5047
2N5103	N JFET	2N4416
2N5104	N JFET	2N4416
2N5105	N JFET	2N4416
2N5114	P JFET	2N5114
2N5115	P JFET	2N5115
2N5116	P JFET	2N5116
2N5158	N JFET	2N5434
2N5159	N JFET	2N5433
2N5196	D N JFET	2N5196
2N5197	D N JFET	2N5197
2N5198	D N JFET	2N5198
2N5199	D N JFET	2N5199
2N5245	N JFET	PN4416
2N5246	N JFET	J305-18
2N5247	N JFE	J304-18
2N5248	N JFET	2N5486
2N5257	N JFET	2N5457
2N5258	N JFET	2N5458
2N5259	N JFET	2N5459
2N5265	P JFET	2N2608
2N5266	P JFET	2N2608
2N5267	P JFET	2N2608
2N5268	P JFET	2N2608
2N5269	P JFET	2N3331
2N5270	P JFET	2N3331
2N5358	N JFET	2N4340
2N5359	N JFET	2N4340
2N5360	N JFET	2N4339
2N5361	N JFET	2N4339
2N5362	N JFET	2N4339
2N5363	N JFET	2N4222A
2N5364	N JFET	2N4224
2N5391	N JFET	2N4867A
2N5392	N JFET	2N4868A
2N5393	N JFET	2N4869A
2N5394	N JFET	2N4869A
2N5395	N JFET	2N4869A
2N5396	N JFET	2N4869A
2N5397	N JFET	U310
2N5398	N JFET	U312
2N5432	N JFET	2N5432
2N5433	N JFET	2N5433
2N5434	N JFET	2N5434
2N5452	D N JFET	2N5452
2N5453	D N JFET	2N5453
2N5454	D N JFET	2N5454
2N5457	N JFET	2N5457
2N5458	N JFET	2N5458
2N5459	N JFET	2N5459
2N5484	N JFET	2N5484
2N5485	N JFET	2N5485
2N5486	N JFET	2N5486
2N5515	D N JFET	2N5515
2N5516	D N JFET	2N5516

Industry Part Number	Type and Classification	Recommended Replacement
2N5517	D N JFET	2N5517
2N5518	D N JFET	2N5518
2N5519	D N JFET	2N5519
2N5520	D N JFET	2N5520
2N5521	D N JFET	2N5521
2N5522	D N JFET	2N5522
2N5523	D N JFET	2N5523
2N5524	D N JFET	2N5524
2N5545	D N JFET	2N5545
2N5546	D N JFET	2N5546
2N5547	D N JFET	2N5547
2N5549	N JFET	2N4392
2N5561	D N JFET	U401
2N5562	D N JFET	U402
2N5563	D N JFET	U404
2N5564	D N JFET	2N5564
2N5565	D N JFET	2N5565
2N5566	D N JFET	2N5566
2N5592	N JFET	2N3822
2N5593	N JFET	2N3822
2N5594	N JFET	2N3822
2N5638	N JFET	2N5638
2N5639	N JFET	2N5639
2N5640	N JFET	2N5640
2N5647	N JFET	2N4117A
2N5648	N JFET	2N4117A
2N5649	N JFET	2N4117A
2N5797	P JFET	2N2608
2N5798	P JFET	2N2608
2N5799	P JFET	2N2608
2N5800	P JFET	2N2608
2N5801	N JFET	2N4393
2N5802	N JFET	2N4393
2N5803	N JFET	2N4392
2N5902	D N JFET	2N5902
2N5903	D N JFET	2N5903
2N5904	D N JFET	2N5904
2N5905	D N JFET	2N5905
2N5906	D N JFET	2N5906
2N5907	D N JFET	2N5907
2N5908	D N JFET	2N5908
2N5909	D N JFET	2N5909
2N5911	D N JFET	2N5911
2N5912	D N JFET	2N5912
2N5949	N JFET	PN4416
2N5950	N JFET	PN4416
2N5951	N JFET	PN4416
2N5952	N JFET	J305
2N5953	N JFET	J305
2N6451	N JFET	2N4393
2N6452	N JFET	2N4393
2N6453	N JFET	2N4393
2N6454	N JFET	2N4393
2N6483	D N JFET	U401
2N6484	D N JFET	U402
2N6585	D N JFET	U404

FET Cross Reference (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement
2N6568	N JFET	U290
2N6656	V MOS N ENH	2N6656
2N6657	V MOS N ENH	2N6657
2N6658	V MOS N ENH	2N6658
2N6659	V MOS N ENH	2N6659
2N6660	V MOS N ENH	2N6660
2N6661	V MOS N ENH	2N6661
3N145	P MOS ENH	3N163
3N146	P MOS ENH	3N163
3N155	P MOS ENH	3N163
3N155A	P MOS ENH	3N163
3N156	P MOS ENH	3N163
3N156A	P MOS ENH	3N163
3N157	P MOS ENH	3N163
3N157A	P MOS ENH	3N163
3N158	P MOS ENH	3N163
3N158A	P MOS ENH	3N163
3N163	P MOS ENH	3N163
3N164	P MOS ENH	3N164
3N174	P MOS ENH	3N163
14T	N JFET	2N3819
142T	N JFET	PN4392
158T	N JFET	PN4302
159T	N JFET	PN4416
100S	N JFET	PN4304
100U	N JFET	2N3684
102M	N JFET	2N5486
102S	N JFET	2N4302
103M	N JFET	2N5457
103S	N JFET	2N5459
104M	N JFET	2N5458
105M	N JFET	2N5459
105U	N JFET	2N4222
106M	N JFET	2N5485
107M	N JFET	2N5486
110U	N JFET	2N4339
115U	N JFET	
120U	N JFET	2N4340
125U	N JFET	2N4339
130U	N JFET	2N4341
135U	N JFET	2N4339
155U	N JFET	2N4416
182S	N JFET	2N4391
183S	N JFET	2N3823
197S	N JFET	2N4338
198S	N JFET	2N4340
199S	N JFET	2N4341
200S	N JFET	2N4392
200U	N JFET	2N3824
201S	N JFET	2N4391
202S	N JFET	2N4392
203S	N JFET	2N3821
204S	N JFET	2N3821
210U	N JFET	2N4416
231S	D N JFET	2N3954
232S	D N JFET	2N3955
233S	D N JFET	2N3956
234S	D N JFET	2N3957
235S	D N JFET	2N3958
241U	N JFET	2N4869
250U	N JFET	2N4091
251U	N JFET	2N4392
703U	N JFET	2N4220
704U	N JFET	2N4220
705U	N JFET	2N4224
707U	N JFET	2N4860
714U	N JFET	2N3822
734U	N JFET	2N4416
734EU	N JFET	PN4416
751U	N JFET	2N4340
752U	N JFET	2N4340
753U	N JFET	2N4341
754U	N JFET	2N4340
755U	N JFET	2N4341
756U	N JFET	2N4340
1277A	N JFET	2N3822
1278A	N JFET	2N3821
1279A	N JFET	2N3821
1280A	N JFET	2N4224
1281A	N JFET	2N3822
1282A	N JFET	2N4341
1283A	N JFET	2N4340
1284A	N JFET	2N4222
1285A	N JFET	2N3821
1286A	N JFET	2N4220
1325A	N JFET	2N4222
1714A	N JFET	2N4340
2000M	N JFET	2N3823
2001M	N JFET	2N3823
2078A	D N JFET	2N3955
2079A	D N JFET	2N3955
2080A	D N JFET	2N5546
2081A	D N JFET	2N5546
2093M	N JFET	2N3687
2094M	N JFET	2N3686
2095M	N JFET	2N3686
2098A	D NJFET	2N5545
2099A	D N JFET	2N5546
2130U	D N JFET	2N5452
2132U	D N JFET	2N3955
2134U	D N JFET	2N3956
2136U	D N JFET	2N3957
2138U	D N JFET	2N3958
2139U	D N JFET	2N3958
2147U	D N JFET	2N3958
2148U	D N JFET	2N3958
2149U	D N JFET	2N3958
A5T3821	N JFET	J305
A5T3822	N JFET	J305
A5T3823	N JFET	PN4416
A5T3824	N JFET	J302-18
A192	N JFET	2N4416
AD830	D N JFET	U421
AD831	D N JFET	U421
AD832	D N JFET	U422
AD833	D N JFET	U426
AD833A	D N JFET	U423
AD835	D N JFET	2N3921
AD836	D N JFET	2N3921
AD837	D N JFET	2N3922
AD838	D N JFET	2N4085
AD839	D N JFET	2N4085
AD840	D N JFET	2N5196
AD841	D N JFET	2N5197
AD842	D N JFET	2N5199
AD3954	D N JFET	2N3954
AD3954A	D N JFET	2N3954A
AD3955	D N JFET	2N3955
AD3956	D N JFET	2N3956
AD3957	D N JFET	2N3957
AD3958	D N JFET	2N3958
BC264	N JFET	PN4304
BC264A	N JFET	PN4302
BC264B	N JFET	PN4304
BC264C	N JFET	PN4304
BC264D	N JFET	PN4416
BF244A/B/C*	N JFET	*Contact factory
BF245A/B/C*	D N JFET	*Contact factory
BFR45	D N JFET	2N4416
BFS21	N JFET	2N5199
BFS21A	D N JFET	2N5199
BFS67	N JFET	2N3821
BFS67P	N JFET	2N4303
BFS68	N JFET	2N3823
BFS68P	N JFET	PN4416
BFS70	N JFET	2N3821
BFS71	N JFET	2N3822
BFS72	N JFET	2N3823
BFS73	N JFET	2N3821
BFS74	N JFET	2N4856
BFS75	N JFET	2N4857
BFS76	N JFET	2N4858
BFS77	N JFET	2N4859
BFS78	N JFET	2N4860
BFS79	N JFET	2N4861
BFS80	N JFET	2N4416A
BFW10	N JFET	2N3823
BFW11	N JFET	2N3822
BFW54	N JFET	2N3822
BFW55	N JFET	2N3822
BFW56	N JFET	2N4869
BFW61	N JFET	2N4224

FET Cross Reference (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement
BSV22	N JFET	2N4416
BSV78	N JFET	2N4856A
BSV80	N JFET	2N4858A
C413N	N JFET	2N5434
C673	N JFET	2N4341
C674	N JFET	2N4341
C680	N JFET	2N4338
C680A	N JFET	2N4338
C681	N JFET	2N4338
C681A	N JFET	2N4338
C682	N JFET	2N4339
C682A	N JFET	2N4339
C683	N JFET	2N4339
C683A	N JFET	2N4339
C684	N JFET	2N4220
C684A	N JFET	2N4220
C685	N JFET	2N4220
C685A	N JFET	2N4220
C6690	N JFET	2N4341
C6691	N JFET	2N4341
C6692	N JFET	2N4340
CM600	N JFET	2N4092
CM601	N JFET	2N4091
CM602	N JFET	2N4091
CM603	N JFET	2N4091
CM640	N JFET	2N4093
CM641	N JFET	2N4093
CM642	N JFET	2N4093
CM643	N JFET	2N4092
CM644	N JFET	2N4092
CM645	N JFET	2N4092
CM646	N JFET	2N4092
CM647	N JFET	2N4091
CM650	N JFET	2N5432
CM651	N JFET	2N5433
CM652	N JFET	2N5432
CM653	N JFET	2N5433
CM697	N JFET	2N5434
CM800	N JFET	2N5434
CMX740	N JFET	U290
CP640	N JFET	U296
CP643	N JFET	2N5434
CP650	N JFET	U322
CP651	N JFET	U320
CP652	N JFET	U322
CP653	N JFET	U320
CR022 Thru CR470 Referenced Under 1N Series		
CRR0240-4300	CL N FET	CRR0240-4300
DN5564-66	D N JFET	DN5564-66
DN5567	D N JFET	DN5567
DPAD1	D PAD N JFET	DPAD1
DPAD2	D PAD N JFET	DPAD2
DPAD5	D PAD N JFET	DPAD5
DPAD10	D PAD N JFET	DPAD10
DPAD20	D PAD N JFET	DPAD20
DPAD50	D PAD N JFET	DPAD50
DPAD100	D PAD N JFET	DPAD100
DU4339	D N JFET	U235
DU4340	D N JFET	U235
E100	N JFET	J203-18
E101	N JFET	J201-18
E102	N JFET	J202-18
E103	N JFET	J105-18
E105	N JFET	J105-18
E106	N JFET	J106-18
E107	N JFET	J107-18
E108	N JFET	J108-18
E109	N JFET	J109-18
E110	N JFET	J110-18
E111	N JFET	J111-18
E112	N JFET	J112-18
E113	N JFET	J113-18
E114	N JFET	J114
E174	P JFET	J174-18
E175	P JFET	J175-18
E176	P JFET	J176-18
E177	P JFET	J177-18
E201	N JFET	J201-18
E202	N JFET	J202-18
E203	N JFET	J203-18
E204	N JFET	J204-18
E210	N JFET	J210
E211	N JFET	J211
E212	N JFET	J212
E230	N JFET	J230-18
E231	N JFET	J231-18
E232	N JFET	J232-18
E270	P JFET	J270-18
E271	P JFET	J271-18
E300	N JFET	J300
E304	N JFET	J304
E305	N JFET	J305
E308	N JFET	J308
E309	N JFET	J309
E310	N JFET	J310
E400	D N JFET	U410
E401	D N JFET	U411
E402	D N JFET	U410
E410	D N JFET	U410
E411	D N JFET	U411
E412	D N JFET	U412
E413	D N JFET	U410
E414	D N JFET	U411
E415	D N JFET	U412
E420	D N JFET	U440
E421	D N JFET	U441
E430	D N JFET	U430
E431	D N JFET	U431
E500	CL N JFET	J500
E501	CL N JFET	J501
E502	CL N JFET	J502
E503	CL N JFET	J503
E504	CL N JFET	J504
E505	CL N JFET	J505
E506	CL N JFET	J506
E507	CL N JFET	J507
EPAD50	DD N JFET	JPAD50
EPAD100	DD N JFET	JPAD100
EPAD200	DD N JFET	JPAD200
EPAD500	DD N JFET	JPAD500
FE100	N JFET	2N3821
FE100A	N JFET	2N3821
FE102	N JFET	2N4119
FE102A	N JFET	2N4119
FE104	N JFET	2N4118
FE104A	N JFET	2N4118
FE200	N JFET	2N3821
FE202	N JFET	2N3821
FE204	N JFET	2N3821
FE300	N JFET	2N3822
FE302	N JFET	2N3821
FE304	N JFET	2N3821
FE0654A	N JFET	2N5486
FE0654B	N JFET	2N5485
FE3819	N JFET	2N3819
FE5457	N JFET	2N5457
FE5458	N JFET	2N5458
FE5459	N JFET	2N5459
FE5484	N JFET	2N5484
FE5485	N JFET	2N5485
FE5486	N JFET	2N5486
FM3954	D N JFET	2N3954
FM3954A	D N JFET	2N3954A
FM3955	D N JFET	2N3955
FM3955A	D N JFET	2N3955A
FM3956	D N JFET	2N3956
FM3957	D N JFET	2N3957
FM3958	D N JFET	2N3958
FN4117	N J FET	FN4117
FN4117A	N J FET	FN4117A
FN4118	N J FET	FN4118
FN4118A	N J FET	FN4118A
FN4119	N J FET	FN4119
FN4119A	N J FET	FN4119A
FN4392	N J FET	FN4392
FN4393	N J FET	FN4393
FT0654A	N JFET	2N5486
FT0654B	N JFET	2N5486
FT0654C	N JFET	2N4221
FT0654D	N JFET	2N4221
FT704	P MOS ENH	3N163

FET Cross Reference (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement
GET5457	N JFET	2N5457
GET5458	N JFET	2N5458
GET5459	N JFET	2N5459
HDIG1030	P MOS ENH	3N163
ID100	D PAD N JFET	DPAD1
ID101	D PAD N JFET	DPAD10
IMF3954	D N JFET	2N3954
IMF3954A	D N JFET	2N3954A
IMF3955	D N JFET	2N3955
IMF3955A	D N JFET	2N3955A
IMF3956	D N JFET	2N3956
IMF3957	D N JFET	2N3957
IMF3958	D N JFET	2N3958
iMF6485	D N JFET	U405
IT100	P JFET	2N5116
IT101	P JFET	2N5114
IT108	N JFET	2N5486
IT109	N JFET	U310
IT1700	P MOS ENH	3N163
IT1702	P MOSENH	3N163
ITE500	CL N JFET	J500
ITE501	CL N JFET	J501
ITE502	CL N JFET	J502
ITE503	CL N JFET	J503
ITE504	CL N JFET	J504
ITE505	CL N JFET	J505
ITE506	CL N JFET	J506
ITE507	CL N JFET	J507
ITE3066	N JFET	J202-18
ITE3067	N JFET	J201-18
ITE3068	N JFET	J201-18
ITE4117	N JFET	2N4117
ITE4118	N JFET	2N4118
ITE4119	N JFET	2N4119
ITE4338	N JFET	J201-18
ITE4339	N JFET	J201-18
ITE4340	N JFET	J202-18
ITE4341	N JFET	J203-18
ITE4391	N JFET	PN4391-18
ITE4392	N JFET	PN4392-18
ITE4393	N JFET	PN4393-18
ITE4416	N JFET	PN4416
ITE4867	N JFET	J230-18
ITE4868	N JFET	J231-18
ITE4869	N JFET	J232-18
J105	N JFET	J105
J105-18	N JFET	J105-18
J106	N JFET	J106
J106-18	N JFET	J106-18
J107	N JFET	J107
J107-18	N JFET	J107-18
J108	N JFET	J108
J108-18	N JFET	J108-18
J109	N JFET	J109
J109-18	N JFET	J109-18
J110	N JFET	J110
J110-18	N JFET	J110-18
J111	N JFET	J111
J111-18	N JFET	J111-18
J112	N JFET	J112
J112-18	N JFET	J112-18
J113	N JFET	J113
J113-18	N JFET	J113-18
J174	P JFET	J174
J174-18	P JFET	J174-18
J175	P JFET	J175
J175-18	P JFET	J175-18
J176	P JFET	J176
J176-18	P JFET	J176-18
J177	P JFET	J177
J177-18	P JFET	J177-18
J201	N JFET	
J201-18	N JFET	
J202	N JFET	
J202-18	N JFET	
J203	N JFET	
J203-18	N JFET	
J204	N JFET	J204
J204-18	N JFET	J204-18
J210	N JFET	J210
J211	N JFET	J211
J212	N JFET	J212
J230	N JFET	J230
J230-18	N JFET	J230-18
J231	N JFET	J231
J231-18	N JFET	J231-18
J232	N JFET	J232
J232-18	N JFET	J232-18
J270	P JFET	J270
J270-18	P JFET	J270-18
J271	P JFET	J271
J271-18	P JFET	J271-18
J300	N JFET	J300
J300A/B/C/D	N JFET	J300A/B/C/D
J304	N JFET	J304
J305	N JFET	J305
J308	N JFET	J308
J309	N JFET	J309
J310	N JFET	J310
J401	D N JFET	U401
J402	D N JFET	U402
J403	D N JFET	U403
J404	D N JFET	U404
J405	D N JFET	U405
J406	D N JFET	U406
J410	D N JFET	U410
J411	D N JFET	U411
J412	D N JFET	U412
J500	CL N JFET	J500
J501	CL N JFET	J501
J502	CL N JFET	J502
J503	CL N JFET	J503
J504	CL N JFET	J504
J505	CL N JFET	J505
J506	CL N JFET	J506
J507	CL N JFET	J507
J508	CL N JFET	J508
J509	CL N JFET	J509
J510	CL N JFET	J510
J511	CL N JFET	J511
J552	CL N JFET	J552
J553	CL N JFET	J553
J554	CL N JFET	J554
J555	CL N JFET	J555
J556	CL N JFET	J556
J557	CL N JFET	J557
JPAD5	PAD N JFET	JPAD5
JPAD10	PAD N JFET	JPAD10
JPAD20	PAD N JFET	JPAD20
JPAD50	PAD N JFET	JPAD50
JPAD100	PAD N JFET	JPAD100
JPAD200	PAD NJFET	JPAD200
JPAD500	PAD N JFET	JPAD500
JR135V	CL N JFET	JR135V
JR170V	CL N JFET	JR170V
JR200V	CL N JFET	JR200V
JR220V	CL N JFET	JR220V
JR240V	CL N JFET	JR240V
J1401	D N JFET	U401
J1402	D N JFET	U402
J1403	D N JFET	U403
J1404	D N JFET	U404
J1405	D N JFET	U405
J1406	D N JFET	U406
J9100	CL N JFET	J9100
K210-18	N JFET	J210
K211-18	N JFET	J211
K212-18	N JFET	J212
K300-18	N JFET	J210
K304-18	N JFET	J304
K305-18	N JFET	J305
K308-18	N JFET	J308
K309-18	N JFET	J309
K310-18	N JFET	J310
KE3684	N JFET	2N4339
KE3685	N JFET	2N4339
KE3686	N JFET	2N4340
KE3687	N JFET	2N4341
KE3823	N JFET	J304-18
KE3970	N JFET	PN4391-18
KE3971	N JFET	PN4392-18
KE3972	N JFET	PN4393-18
KE4091	N JFET	PN4391-18
KE4092	N JFET	PN4392-18
KE4093	N JFET	PN4393-18
KE4220	N JFET	2N5457
KE4221	N JFET	2N5457
KE4222	N JFET	2N5459

FET Cross Reference (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement
KE4223	N JFET	J304-18
KE4224	N JFET	J304-18
KE4391	N JFET	PN4391-18
KE4392	N JFET	PN4392-18
KE4393	N JFET	PN4393-18
KE4416	N JFET	PN4416
KE4856	N JFET	PN4391-18
KE4857	N JFET	PN4392-18
KE4858	N JFET	PN4393-18
KE4859	N JFET	PN4391-18
KE4860	N JFET	PN4392-18
KE4861	N JFET	PN4393-18
KE5103	N JFET	J305
KE5104	N JFET	J304
KE5105	N JFET	J305
KK4416-18	N JFET	PN4416
LDF603	N JFET	2N4221A
LDF604	N JFET	2N4221A
LDF605	N JFET	2N4221A
M163	P MOS ENH	3N163
M164	P MOS ENH	3N164
MEM520	P MOS ENH	3N164
MEM520C	P MOS ENH	3N164
MEM561	P MOS ENH	3N163
MEM561C	P MOS ENH	3N163
MEM806	P MOS ENH	3N163
MEM806A	P MOS ENH	3N163
MFE823	P MOS ENH	MFE823
MFE2000	N JFET	2N4416
MFE2001	N JFET	2N4416
MFE2004	N JFET	2N4093
MFE2005	N JFET	2N4092
MFE2006	N JFET	2N4091
MFE2007	N JFET	2N4860
MFE2008	N JFET	2N4859
MFE2009	N JFET	2N4859
MFE2010	N JFET	2N5434
MFE2011	N JFET	2N5433
MFE2012	N JFET	2N5432
MFE2093	N JFET	2N4341
MFE2094	N JFET	2N4340
MFE2095	N JFET	2N4339
MFE4007	P JFET	2N2609
MFE4008	P JFET	2N2609
MFE4009	P JFET	2N3329
MFE4010	P JFET	2N3330
MFE4011	P JFET	2N3330
MFE4012	P JFET	2N3331
MK10	N JFET	2N4416
MMF1	D N JFET	2N3921
MMF2	D N JFET	2N3921
MMF3	D N JFET	2N3921
MMF4	D N JFET	2N3921
MMF5	D N JFET	2N3921
MMF6	D N JFET	2N3921
MMT3823	N JFET	2N3823
MPF102	N JFET	MPF102
MPF103	N JFET	2N5457
MPF104	N JFET	2N5458
MPF105	N JFET	2N5459
MPF106	N JFET	2N5485
MPF107	N JFET	2N5486
MPF108	N JFET	MPF108
MPF109	N JFET	MPF109
MPF111	N JFET	MPF111
MPF112	N JFET	MPF112
MPF256	N JFET	J309
MPF820	N JFET	U310
MPF970	P JFET	J174
MPF971	P JFET	J176
MPF4391	N JFET	PN4391-18
MPF4392	N JFET	PN4392-18
MPF4393	N JFET	PN4393-18
NF500	N JFET	2N4416
NF501	N JFET	2N4416
NF506	N JFET	2N4416
NF510	N JFET	2N4393
NF511	N JFET	2N4393
NF520	N JFET	2N4339
NF521	N JFET	2N4339
NF522	N JFET	2N4339
NF523	N JFET	2N4340
NF530	N JFET	2N4341
NF531	N JFET	2N4339
NF532	N JFET	2N4341
NF533	N JFET	2N4339
NF580	N JFET	2N5432
NF581	N JFET	2N5432
NF582	N JFET	2N5433
NF583	N JFET	2N5434
NF584	N JFET	2N5433
NF585	N JFET	2N4859
NF4302	N JFET	PN4302
NF4303	N JFET	PN4303
NF4304	N JFET	PN4304
NF4445	N JFET	2N5432
NF4446	N JFET	2N5433
NF4447	N JFET	2N5432
NF4448	N JFET	2N5433
NF5163	N JFET	PN5163
NF5457	N JFET	2N5457
NF5458	N JFET	2N5458
NF5459	N JFET	2N5459
NF5484	N JFET	2N5484
NF5485	N JFET	2N5485
NF5486	N JFET	2N5486
NF5555	N JFET	2N5555
NF5638	N JFET	2N5638
NF5639	N JFET	2N5639
NF5640	N JFET	2N5640
NF5653	N JFET	2N5653
NF5654	N JFET	2N5654
PAD1	PAD N JFET	PAD1
PAD2	PAD N JFET	PAD2
PAD5	PAD N JFET	PAD5
PAD10	PAD N JFET	PAD10
PAD20	PAD N JFET	PAD20
PAD50	PAD N JFET	PAD50
PAD100	PAD N JFET	PAD100
P1086	P JFET	P1086
P1086-18	P JFET	P1086-18
P1087	P JFET	P1087
P1087-18	P JFET	P1087-18
PN4091	N JFET	PN4091
PN4092	N JFET	PN4092
PN4093	N JFET	PN4093
PN4117	N JFET	PN4117
PN4117A	N JFET	PN4117A
PN4118	N JFET	PN4118
PN4118A	N JFET	PN4118A
PN4119	N JFET	PN4119
PN4119A	N JFET	PN4119A
PN4120	N JFET	PN4120
PN4120A	N JFET	PN4120A
PN4302	N JFET	PN4302
PN4302-18	N JFET	PN4302-18
PN4303	N JFET	PN4303
PN4303-18	N JFET	PN4303-18
PN4304	N JFET	PN4304
PN4304-18	N JFET	PN4304-18
PN4391	N JFET	PN4391
PN4391-18	N JFET	PN4391-18
PN4392	N JFET	PN4392
PN4392-18	N JFET	PN4392-18
PN4393	N JFET	PN4393
PN4393-18	N JFET	PN4393-18
PN4416	N JFET	PN4416
PN5163	N JFET	PN5163
PF510	P JFET	2N5018
PF511	P JFET	2N5014
SD210DE	N D MOS ENH	SD210DE
SD211DE	N D MOS ENH	SD211DE
SD212DE	N D MOS ENH	SD212DE
SD213DE	N D MOS ENH	SD213DE
SD214DE	N D MOS ENH	SD214DE
SD215DE	D N JFET	SD215DE
SU2078	D N JFET	U425
SU2079	D N JFET	U425
SU2098	D N JFET	2N5197
SU2098A	D N JFET	2N5197
SU2098B	D N JFET	2N5196
SU2099	D N JFET	2N5197
SU2099A	D N JFET	2N5197
SU2365	D N JFET	U401

FET Cross Reference (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement
SU2365A	D N JFET	U401
SU2366	D N JFET	U402
SU2366A	D N JFET	U402
SU2367	D N JFET	U403
SU2367A	D N JFET	U403
SU2368	D N JFET	U404
SU2368A	D N JFET	U404
SU2369	D N JFET	U405
SU2369A	D N JFET	U405
SU2410	D N JFET	U424
SU2411	D N JFET	U425
SU2412	D N JFET	U426
TD5902	D N JFET	2N5902
TD5902	D N JFET	2N5902
TD5902A	D N JFET	2N5902
TD5903	D N JFET	2N5903
TD5903A	D N JFET	2N5903
TD5904	D N JFET	2N5904
TD5904A	D N JFET	2N5904
TD5905	D N JFET	2N5905
TD5905A	D N JFET	2N5905
TD5906	D N JFET	2N5906
TD5906A	D N JFET	2N5906
TD5907	D N JFET	2N5907
TD5907A	D N JFET	2N5907
TD5908	D N JFET	2N5908
TD5908A	D N JFET	2N5908
TD5909	D N JFET	2N5909
TD5909A	D N JFET	2N5909
TD5911	D N JFET	2N5911
TD5911A	D N JFET	2N5911
TD5912	D N JFET	2N5912
TD5912A	D N JFET	2N5912
TIS14	N JFET	2N4340
TIS25	D N JFET	U401
TIS26	D N JFET	U402
TIS27	D N JFET	U404
TIS41	N JFET	2N4859
TIS58	N JFET	J305-18
TIS59	D N JFET	U1837
TIS73	N JFET	PN4391-18
TIS74	N JFET	PN4392-18
TIS75	N JFET	PN4393-18
TIS88	N JFET	2N5486
TIXS41	N JFET	2N4859
TIXS42	N JFET	PN4393-18
TN4117	N JFET	**PN4117**
TN4117A	N JFET	**PN4117A**
TN4118	N JFET	**PN4118**
TN4118A	N JFET	**PN4118A**
TN4119	N JFET	**PN4119**
TN4119A	N JFET	**PN4119A**
TN4338	N JFET	2N4338
TN4339	N JFET	2N4339
TN4340	N JFET	2N4340
TN4341	N JFET	2N4341
TP5114	P JFET	2N5114
TP5115	P JFET	2N5115
TP5116	P JFET	2N5116
U110	P JFET	**2N2609**
U112	P JFET	**2N2609**
U133	P JFET	**2N2609**
U146	P JFET	**2N2609**
U147	P JFET	**2N2609**
U148	P JFET	**2N2609**
U149	P JFET	2N2609
U168	P JFET	2N2609
U182	N JFET	2N4857
U183	N JFET	2N3824
U197	N JFET	2N4339
U198	N JFET	2N4340
U199	N JFET	2N4341
U200	N JFET	**2N3970**
U201	N JFET	**2N3971**
U202	N JFET	**2N3972**
U221	N JFET	2N4391
U222	N JFET	2N4391
U231	D N JFET	U231
U232	D N JFET	U232
U233	D N JFET	U233
U234	D N JFET	U234
U235	D N JFET	U235
U240	N JFET	2N5432
U241	N JFET	2N5433
U242	N JFET	2N5432
U243	N JFET	2N5433
U248	D N JFET	2N5902
U248A	D N JFET	2N5906
U249	D N JFET	2N5903
U249A	D N JFET	2N5907
U250	D N JFET	2N5904
U250A	D N JFET	2N5908
U251	D N JFET	2N5905
U251A	D N JFET	2N5909
U254	N JFET	2N4859
U255	N JFET	2N4860
U256	N JFET	2N4861
U257	D N JFET	U257
U273	N JFET	2N4118A
U273A	N JFET	2N4118A
U274	N JFET	2N4119A
U274A	N JFET	2N4119A
U275	N JFET	2N4119A
U275A	N JFET	2N4119A
U280	D N JFET	U231
U281	D N JFET	U231
U282	D N JFET	U232
U283	D N JFET	U232
U284	D N JFET	U233
U285	D N JFET	U234
U290	N JFET	U290
U291	N JFET	U291
U295	N JFET	U295
U296	N JFET	U296
U300	P JFET	2N5114
U301	P JFET	2N5115
U304	P JFET	U304
U305	P JFET	U305
U306	P JFET	U306
U308	N JFET	U308
U309	N JFET	U309
U310	N JFET	U310
U311	N JFET	U311
U320	N JFET	U290
U321	N JFET	U291
U322	N JFET	U290
U401	D N JFET	U401
U402	D N JFET	U402
U403	D N JFET	U403
U404	D N JFET	U404
U405	D N JFET	U405
U406	D N JFET	U406
U410	D N JFET	U410
U411	D N JFET	U411
U412	D N JFET	U412
U421	D N JFET	U421
U422	D N JFET	U422
U423	D N JFET	U423
U424	D N JFET	U424
U425	D N JFET	U425
U426	D N JFET	U426
U427	D N JFET	U427
U428	D N JFET	U428
U430	D N JFET	U430
U431	D N JFET	U431
U440	D N JFET	U440
U441	D N JFET	U441
U443	D N JFET	U443
U444	D N JFET	U444
U508	N JFET	CR030
U1177	N JFET	2N4220A
U1178	N JFET	2N3821
U1179	N JFET	2N3821
U1180	N JFET	2N4221A
U1181	N JFET	2N4220A
U1182	N JFET	2N3821
U1277	N JFET	2N4339
U1278	N JFET	2N4339
U1279	N JFET	2N4340
U1280	N JFET	2N4339
U1281	N JFET	2N3822
U1282	N JFET	2N4341
U1283	N JFET	2N4340

FET Cross Reference (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement
U1284	N JFET	2N4341
U1285	N JFET	2N4220
U1288	N JFET	2N4341
U1287	N JFET	2N4092
U1321	N JFET	2N3966
U1322	N JFET	2N4221A
U1323	N JFET	2N4221A
U1324	N JFET	2N4220A
U1325	N JFET	2N4222
U1420	N JFET	2N3821
U1421	N JFET	2N3822
U1422	N JFET	2N3822
U1714	N JFET	2N4340
U1837E	N JFET	PN4416
U1897	N JFET	U1897
U1897-18	N JFET	U1897-18
U1897E	N JFET	U1897-18
U1898	N JFET	U1898
U1898-18	N JFET	U1898-18
U1898E	N JFET	U1898-18
U1899	N JFET	U1899
U1899-18	N JFET	U1899-18
U1899E	N JFT	U1899-18
U1994E	N JFET	PN4416
U2047E	N JFET	PN4416
U3000	N JFET	2N4341
U3001	N JFET	2N4339
U3002	N JFET	2N4338
U3010	N JFET	2N4341
U3011	N JFET	2N4340
U3012	N JFET	2N4338
UC20	N JFET	2N4341
UC40	P JFET	2N2609
UC41	P JFET	2N2609
UC100	N JFET	2N4339
UC110	N JFET	2N4339
UC115	N JFET	2N4340
UC120	N JFET	2N4339
UC130	N JFET	2N4341
UC155	N JFET	2N4416
UC200	N JFET	2N3824
UC201	N JFET	2N3824
UC210	N JFET	2N4416
UC220	N JFET	2N3822
UC240	N JFET	2N4869
UC241	N JFET	2N4869
UC250	N JFET	2N4091
UC251	N JFET	2N4392
UC300	P JFET	2N2609
UC310	P JFET	2N2609
UC320	P JFET	2N2609
UC330	P JFET	2N2609
UC340	P JFET	2N2609
UC400	P JFET	2N3331
UC401	P JFET	2N5116
UC410	P JFET	2N3330
UC420	P JFET	2N3329
UC450	P JFET	2N5114
UC451	P JFET	2N5116
UC588	N JFET	PN4416
UC703	N JFET	2N4220
UC704	N JFET	2N4220
UC705	N JFET	2N4224
UC707	N JFET	2N4860
UC714	N JFET	2N3822
UC714E	N JFET	J203-18
UC734	N JFET	2N4416
UC734E	N JFET	PN4416
UC751	N JFET	2N4340
UC752	N JFET	2N4340
UC753	N JFET	2N4341
UC754	N JFET	2N4340
UC755	N JFET	2N4341
UC756	N JFET	2N4340
UC805	P JFET	2N3331
UC807	N JFET	2N4860
UC814	P JFET	2N3331
UC851	P JFET	2N2608
UC853	P JFET	2N2608
UC854	P JFET	2N2608
UC855	P JFET	2N2609
UC1700	P MOS ENH	3N163
UC1764	P MOS ENH	3N163
UC2130	D N JFET	2N5452
UC2132	D N JFET	2N3955
UC2134	D N JFET	2N3956
UC2136	D N JFET	2N3957
UC2138	D N JFET	2N3958
UC2139	D N JFET	2N3958
UC2147	D N JFET	2N3958
UC2148	D N JFET	2N3958
UC2149	D N JFET	2N3958
VCR2N	N JFET	VCR2N
VCR3P	P JFET	VCR3P
VCR4N	N JFET	VCR4N
VCR5P	P JFET	VCR5P
VCR6P	P JFET	2N5116
VCR7N	N JFET	VCR7N
VCR11N	N JFET	VCR11N
WK5457	N JFET	2N5457
WK5458	N JFET	2N5458
WK5459	N JFET	2N5459

FET Product Information

Siliconix products are divided into three basic categories:

Standard Products, Modified Standard Products, Custom Products

- **Standard Products** — All the part numbers described in this catalog are standard products. A summary list of the prefixes used is shown below in the Device Identification Table. Ordering any of the standard products is easily done by referring to the data sheet part number. For example, a 2N4391 is simply ordered by that number: "2N4391." It will also appear in that form on the price lists, published separately.

- **Examples of Modified Standard Products are:**

Electrical Specials — Devices with either tightened, relaxed and/or special electrical specifications selected from a standard product.

Mechanical Specials — Devices with standard or modified electrical specifications mounted in non-standard packages or modified (lead formed) standard packages. Modifications and/or additions to standard marking are also considered mechanical specials.

High Reliability Specials — Siliconix has a number of standard High-Reliability screening options that can be ordered as standard products. These options include MIL-STD-750B. High-Rel process option details will be found in the introductory section of this data book. In addition, Siliconix offers certain JEDEC-registered FETs with JAN, JANTX, or JANTXV processing. Refer to any current Siliconix OEM price list for details on specific part numbers. If existing screening processes do not meet individual customer requirements, Siliconix can provide special additional inspections and controls to meet the stringent demands.

In all of the above cases (with the exception of JAN, JANTX, or JANTXV parts), a special part number is assigned which defines the part either by reference to customer's print(s) or by associated special requirements. Each special product is proprietary to the customer, and is *not* made available to other customers.

- **Custom Products** — Are designed to meet customer requirements not realizable by selection from standard parts; usually, these products require special engineering development. The proprietary relationship described above also applies to custom products.

Inquiries for *SPECIAL DEVICES* may be directed to the nearest field sales office or to:

FET Marketing Department, Siliconix incorporated, 2201 Laurelwood Road, Santa Clara, California 95054,
Telephone: (408) 988-8000.

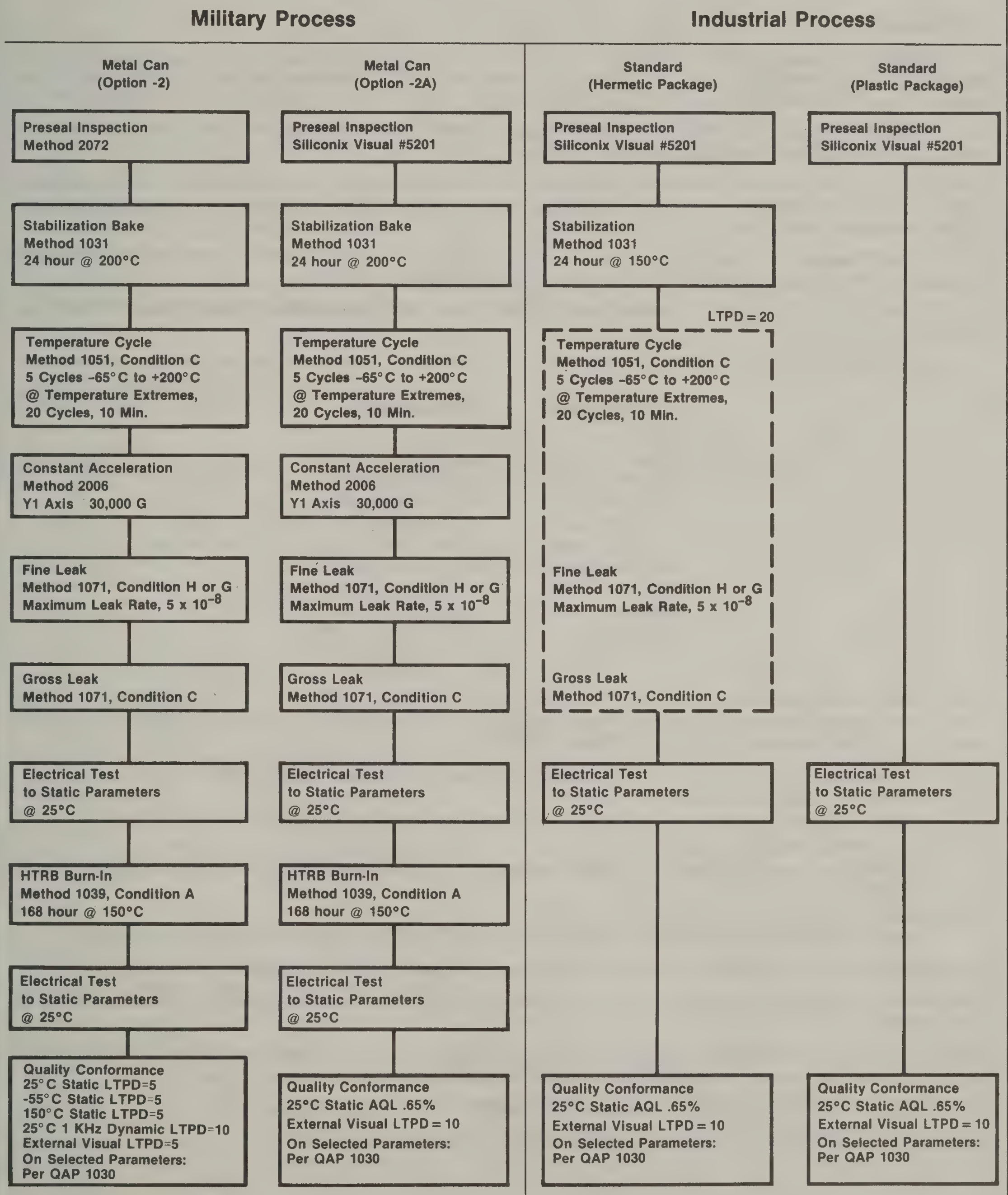
FETs/Part Number Prefixes and Suffixes

Prefix	XXX	XXXX
BF	European Transistor Standard	
CR	Si Standard N-Channel Current Regulator	
CRR	Si Standard N-Channel Current Regulator	
DM		Si Special DMOS FET
DN		Si Dual N-Channel JFET
FN		Si N-Channel JFET
DPAD	Si Standard Dual JFET Diode	
J	Si Standard TO-92 Cased FET	Special TO-92 Cased FET
JR	Si Standard Current Limiter Diode TO-92 Cased FET	
JPAD	Si Standard JFET Diode	
PAD	Si Standard JFET Diode	
PN		Si Standard TO-92 Cased FET
SD		Si Standard DMOS FET
U	Si Standard FET	
VCR	Si Standard N- and P-Channel Voltage Controlled Resistors	
2N		JEDEC-Registered Device
3N	JEDEC—Registered Device	

Suffix	
-05	Std TO-92 Pkg. Lead Formed to TO-5 Pin Circle
-18	Std TO-92 Pkg. with Center Lead Formed Toward Flat in TO-18 Pin Circle
-TRF	Tape and Reel available on TO-92 FETs.

PROCESS OPTION 750B-MIL-STD 750 = -2 Contact Factory
= -2A Contact Factory

FET Process Option Flow Chart


Military Process
Industrial Process
Metal Can (Option -2)
Preseal Inspection Method 2072
Stabilization Bake Method 1031 24 hour @ 200°C
Temperature Cycle Method 1051, Condition C 5 Cycles -65°C to +200°C @ Temperature Extremes, 20 Cycles, 10 Min.
Constant Acceleration Method 2006 Y1 Axis 30,000 G
Fine Leak Method 1071, Condition H or G Maximum Leak Rate, 5 x 10^-8
Gross Leak Method 1071, Condition C
Electrical Test to Static Parameters @ 25°C
HTRB Burn-In Method 1039, Condition A 168 hour @ 150°C
Electrical Test to Static Parameters @ 25°C
Quality Conformance 25°C Static LTPD=5 -55°C Static LTPD=5 150°C Static LTPD=5 25°C 1 KHz Dynamic LTPD=10 External Visual LTPD=5 On Selected Parameters: Per QAP 1030
Metal Can (Option -2A)
Preseal Inspection Siliconix Visual #5201
Stabilization Bake Method 1031 24 hour @ 200°C
Temperature Cycle Method 1051, Condition C 5 Cycles -65°C to +200°C @ Temperature Extremes, 20 Cycles, 10 Min.
Constant Acceleration Method 2006 Y1 Axis 30,000 G
Fine Leak Method 1071, Condition H or G Maximum Leak Rate, 5 x 10^-8
Gross Leak Method 1071, Condition C
Electrical Test to Static Parameters @ 25°C
HTRB Burn-In Method 1039, Condition A 168 hour @ 150°C
Electrical Test to Static Parameters @ 25°C
Quality Conformance 25°C Static AQL .65% External Visual LTPD = 10 On Selected Parameters: Per QAP 1030
Standard (Hermetic Package)
Preseal Inspection Siliconix Visual #5201
Stabilization Method 1031 24 hour @ 150°C
LTPD = 20
Temperature Cycle Method 1051, Condition C 5 Cycles -65°C to +200°C @ Temperature Extremes, 20 Cycles, 10 Min.
Fine Leak Method 1071, Condition H or G Maximum Leak Rate, 5 x 10^-8
Gross Leak Method 1071, Condition C
Electrical Test to Static Parameters @ 25°C
Quality Conformance 25°C Static AQL .65% External Visual LTPD = 10 On Selected Parameters: Per QAP 1030
Standard (Plastic Package)
Preseal Inspection Siliconix Visual #5201
Electrical Test to Static Parameters @ 25°C
Quality Conformance 25°C Static AQL .65% External Visual LTPD = 10 On Selected Parameters: Per QAP 1030

NOTES: Processing and test methods are MIL-STD750 unless specified otherwise
-2A Significant savings.

Additional Product Options for European Customers

CECC 50 000

CECC 50 000 is a European system of continuous product assessment intended to produce electronic components of assessed quality to specifications and procedures which conform to internationally recognized standards. Components produced under the system are accepted by all participating countries without further testing being necessary.

At this time, member countries of the CECC are Belgium, Denmark, Germany, France, Ireland, Italy, the Netherlands, Norway, Sweden, Switzerland and the United Kingdom.

Under this assessment scheme, devices are manufactured on an approved line to nationally approved specifications written in accordance with CECC rules. The manufacturer must comply with defined standards relating to organization, facilities and quality control procedures.

Specific device types are individually qualified against a fixed detail specification which has been approved by the British Standards Institute acting as the national supervising agency on behalf of CECC.

The CECC 50 000 scheme is administered in the UK by the BSI, and UK generated specifications are prefixed with the letters BS.

A number of popular standard device types are now qualified and the following detail specifications are available:

Type Number	BS Specification
2N3970/1/2	BS CECC 50012-001
2N4091/2/3	BS CECC 50012-002
2N4391/2/3	BS CECC 50012-004
2N4856/7/8	BS CECC 50012-005
2N4859/60/61	BS CECC 50012-005
2N4856A/7A/8A	BS CECC 50012-006
2N4859A/60A/61A	BS CECC 50012-006
2N3821/2	BS CECC 50012-007
2N3824	BS CECC 50012-008
2N4220/1/2	BS CECC 50012-009
2N4220/1A/2A	BS CECC 50012-009

Each of the approved types is now available with additional screening options, including high temperature reverse bias burn-in, of either 48, 72 or 168 hours duration. Screening details are appended to the detail specification and conform to appendix VI of the European Standard CECC 50 0000 ISSUE 3.

Product is released with a BS CECC certificate of conformity and will have been submitted to:

1. Group A sample inspection (lot by lot)
   quality assessment tests, assuring product conforms to electrical specification.
2. Group B sample inspection (lot by lot)
   reliability tests, including package related tests and 168 hours electrical endurance, to identify potential early failures.
3. Group C sample inspection (periodic—3 monthly)
   long term reliability tests including 1000 hours of high temperature storage and electrical endurance.

Data from the inspection tests is available to the customer in the form of CTRs (certified test records).

Manufacturing of BS CECC product is carried out at the Siliconix UK facility located in Morriston, Swansea SA6 6NE, South Wales

In addition to BS CECC approved product, the Siliconix UK facility can provide internationally recognized high-reliability screening options on standard products. These include Mil-750B and custom screening options.

JAN, JANTX or JANTXV processing for certain JEDEC-registered FETs can also be supplied.

For additional information, enquiries may be directed to the nearest field sales office.

Die Process Information

Siliconix is a large volume supplier of die to the hybrid industry. Both military and industrial grades are available. Screening includes 100% DC electrical probe and 100% visual inspection of each die.

Physical Data

- Physical layout and dimensions are presented in the die topography section.
- Each die is passivated with approximately 8,000 angstroms of non-crystalline glass.
- All die are gold backed. Gold backing is approximately 1,500 angstroms thick.
- Die metallization is deposited aluminum approximately 12,000 angstroms thick.
- Standard thickness 0.008 ± 0.002 in inches.

Die Screening Criteria

- **Probe Test Capability** — Siliconix performs three classes of electrical tests. The first category is a group of tests that may be performed on a 100 percent basis in wafer form. Examples are pinch-off voltage $V_{GS(off)}$ and breakdown voltage BV_{GSS}.

  A second group consists of tests such as very low leakage I_{GSS} where 100 percent testing is impractical, but sample testing may be performed. Generally, test time is the factor that renders these tests impractical on a 100 percent basis.

  Finally, there are those tests that cannot be performed unless a sample group of units are assembled for evaluation. Capacitance and differential voltage drift are two examples (On request only).

  The adjacent table summarizes our wafer probe test capability and serves as a guide line to your design needs. Actual testing condition and procedure may vary. For specific parameters and test conditions, refer to the appropriate data sheet.

TEST PARAMETER	Condition Range			100% Wafer Sort Capability		Sample Wafer Sort Capability		Sample Test in Package Form	
				Limit Range		Limit Range		Limit Range	
	Cond.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
IGSS, IGSO, IOGD	VGS	0.01V	200V	100pA	10μA		0.5pA		0.5pA
IDSX, ISDX, IDSS, ISDS	VGS	0.01V	100V	100pA	100mA				
	VDS	0.01V							
IG	ID	10μA	100mA	100pA	10μA				
	VDG	0.01V	100V						
VGS(th), Vp, VGS	ID	100pA	100mA	0.01V	100V				
	VDS	0.01V	100V						
BVGSS, BVGDD, BVGSO	IG	100pA	10μA	0.01V	200V				
BVDSX, BVSOX	ID	100pA	100mA	0.1V	100V				
VDS (on)	ID	10μA	100mA	1mV	10V				
rDS (on)	ID	10μA	100mA	1 ohm	10M ohm				
gfs (constant VGS)	VGS	0.01V	100V	10 μmho	100 mmho				
	VDS	0.01V							
gfs (constant ID)	ID	10μA	100mA	10 μmho	100 mmho				
	VDS	0.01V	100V						
$\overline{en}$ (constant VGS)	VGS	0	30V					$\frac{3nv}{\sqrt{Hz}}$	$\frac{300\ nv}{\sqrt{Hz}}$
	VDS	0	100V						
	Freq	10 Hz	100 KHz						
$\overline{en}$ (constant ID)	ID	1μA	30 mA					$\frac{3nv}{\sqrt{Hz}}$	$\frac{300\ nv}{\sqrt{Hz}}$
	VDS	0V	100V						
	Freq	10 Hz	100 KHz						
|VGS1 - VGS2|	VDG	0.01V	100V	0.1mV	100mV			20mV	
	ID	1μA	10mA						
Capacitance high Frequency	VDS	0V	100V					0.1pF	1000pF
	VGS	0V	100V						
	ID	0A	100mA						
gfs1/gfs2 IDSS1/IDSS2 goss1-goss2 CMRR, Δ|Vgs1-VGS2|/ΔT	TESTS PERFORMED AFTER SAMPLE IS ASSEMBLED FOR EVALUATION								
QC Inspection	*			*0.65 AQL			1.5 AQL		1.5 AQL

* all in die form not after Customer Assembly

- **Visual Criteria** — Die are supplied with 100% visual sort to the criteria of MIL-STD-750 method 2072.

Die Process Information (Cont'd)

Assembly

- Chips supplied in waffle packs normally do not require cleaning. Wafers should be cleaned after sawing or scribing, and fracturing.
- Chips should be handled with a vacuum pick-up with protected tip or with tweezers gripping the chip on its sides.
- When handling MOSFET chips, particularly non-gate protected types, steps must be taken to prevent damage by static discharge. In some extreme cases, handling precautions may be necessary for junction FET chips.
- Chips can be die attached either eutectically or by conductive epoxy when lower temperatures are necessary. Gold silicon eutectic occurs at temperatures between 385°C and 425°C.
- Bonding of wires from chip pads to posts can be achieved by thermocompression gold wire or ultrasonic aluminum wire bonded.

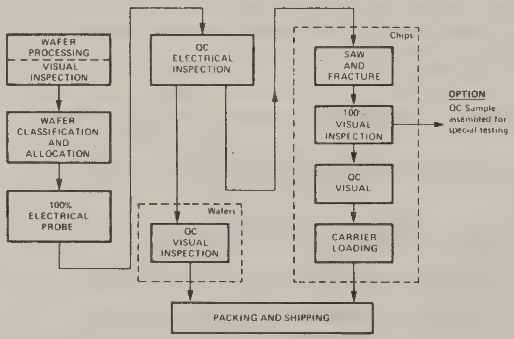
Options

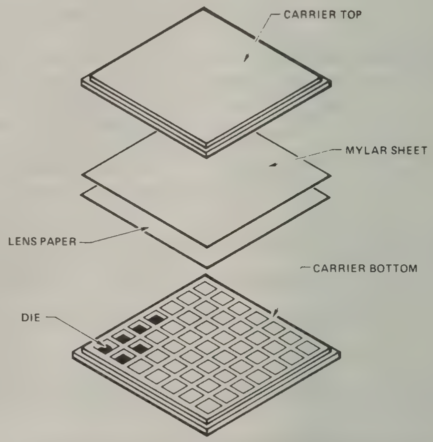
- **SEM** — Scanning electron microscope examination and control in accordance with MIL-STD-883 Method 2018 can be ordered on chips and wafers.
- **Wafer qualification to unprobed parameters** — sample testing of purchased chips to demonstrate capability to perform at data sheet temperature extremes by use of LTPD techniques can be provided.
- **Hot probe** — Siliconix has a chip processor/distributor with hot probe capability available.

Chip Packaging

- Chips are packaged as individual die in the flat waffle carrier illustrated in Figure 1. The carrier has a cavity size adequate to allow ease of loading/unloading and also prevents die from rotating within the cavity.
- Standard carrier 20 x 20 (400 die)

Chip and Wafer Processing





NOTE. CARRIER TOP & BOTTOM SECURED BY CLIPS

Figure 1

PC Board Layout and Construction for Low Leakage Applications

In order to realize the full capability of these devices in circuits that are sensitive to very low currents, considerable care should be exercised in PC board layout and construction techniques. If proper care is not taken, board leakage currents can easily become much larger than the leakage currents of the devices themselves, especially under conditions of high temperature and humidity. Excessive leakage currents can be produced by poor quality boards, socket leakage, poor board layout, imperfectly cleaned boards, or improperly applied or cured protective coatings.

It is important to start with quality PC boards which have high resistivity and low susceptance to moisture. Boards of Teflon® or polycarbonate composition exhibit these attributes and are preferred. Glass-epoxy boards are less desirable because they will absorb moisture, and if used must be protected with a conformal coating.

The use of sockets should be avoided wherever possible since the pin-to-pin isolation is often not great enough to prevent small leakage currents from occurring. These currents can significantly degrade device performance in low leakage applications. If sockets cannot be avoided use the highest quality available, preferably teflon.

In laying out PC boards, care should be taken to keep pins and runs which are sensitive to very low currents away from pins and runs which will be at significantly higher or lower voltages. The most common leakage current problems occur between pins sensitive to low current levels and nearby pins at or near one of the supply voltages. Thus, if the isolation between critical pins and nearby high or low voltage pins is increased, leakage is minimized.

In order to reduce leakage currents, it is very important that all PC boards and experimental breadboards be thoroughly cleaned with a solvent after construction. A recommended procedure is to wash each board in an ultrasonic cleaning bath of alcohol, trichloroethylene, or some other commercial solvent, and to blow dry with compressed air. The purpose of this is to remove all skin oils (the greatest cause of leakage in improperly cleaned boards), solder fluxes, and other films and residues left over from the construction process which can cause gross leakage problems and erratic device behavior, especially at temperatures above 85°C.

For best results, the thoroughly cleaned boards should be protected against dirt, conductive films, and humidity by the application of a conformal coating. Urethane and Dow Corning's R-4-3117 Silicone are easy to use and offer sufficient protection under most operating conditions. Epoxy results in a more durable coating but care must be taken to insure that it is cured properly; an improperly cured layer of epoxy will make the high temperature leakage problem worse. Union Carbide's Parylene also results in a relatively durable coating.

The ultimate leakage protection method consists of printed circuit metalization guard rings driven from a low impedance buffer amplifier whose output is at the same potential as the pin being protected. This completely eliminates board surface leakage at critical pins by removing any difference in potential, but it is difficult to implement due to the extra buffer amplifier required and the tight PC board metalization spacings encountered.

Teflon® is a registered trademark of DuPont.

Introduction 1

Data Sheets 2

Selector Guides 3

Geometry 4

Application Notes 5

Appendices 6

Other Products 7

Worldwide Sales Offices 8

p-channel JFETs designed for . . .

Siliconix

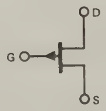
Performance Curves PC PD
See Section 4

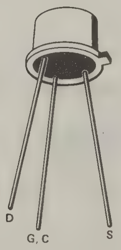
■ General Purpose Amplifiers

BENEFITS

- JAN Approved Version Available

TO-18
See Section 6





*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain and Gate-Source Voltage (Note 3). . . . . .30 V
Gate Current, Forward Biased (Note 1). . . . . 50 mA
Total Device Dissipation (Derate 2 mW/°C) . . . . 300 mW
Storage Temperature Range . . . . −65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N2609 Min	2N2609 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)		30	nA	V_{GS} = 30 V, V_{DS} = 0 V	
2					30	μA	V_{GS} = 5 V, V_{DS} = 0, T_A = 150°C	
3		BV_{GSS}	Gate-Source Breakdown Voltage	30		V	I_G = 1 μA, V_{DS} = 0 V	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	1	4	V	V_{DS} = -5 V, I_D = 1 μA	
5		I_{DSS}	Saturation Drain Current	-2	-10	mA	V_{DS} = -5 V, V_{GS} = 0 V	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2500		μmho	V_{DS} = -5 V, V_{GS} = 0 V	f = 1 kHz
7		C_{iss}	Common-Source Input Capacitance		30	pF	V_{DS} = -5 V, V_{GS} = 1 V	f = 140 kHz
8		NF	Noise Figure		3	dB	V_{DS} = -5 V, V_{GS} = 0, R_G = 1M Ω	f = 1 kHz

PD

*JEDEC Registered Data

NOTES:
1. Not JEDEC Registered
2. I_{GSS} is JEDEC Registered at V_{GS} = 5 V
3. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

2N3819
PREFERRED PART 2N5457

n-channel JFET
designed for . . .

- **General Purpose Amplifiers**
- **Analog Switching**

Siliconix

Performance Curves NH NRL
See Section 4

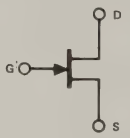
BENEFITS

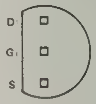
- Low Cost
- Specified at 100 MHz
- Automatic Insertion Package

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	25 V
Drain-Source Voltage	25 V
Reverse Gate-Source Voltage	–25 V
Gate Current	10 mA
Continuous Device Dissipation at (or Below) 25°C Free Air Temperature (Note 1)	200 mW
Storage Temperature Range	–55°C to +150°C
Lead Temperature (1/16″ from Case for 10 seconds)	260°C

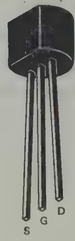
TO-92
See Section 6





Bottom View

Plastic



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–25		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current		–2	nA	$V_{GS} = -15\ V$, $V_{DS} = 0$	
3					–2	μA		$T_A = 100°C$
4		I_{DSS}	Saturation Drain Current	2	20	mA	$V_{DS} = 15\ V$, $V_{GS} = 0$ (Note 2)	
5		V_{GS}	Gate-Source Voltage	–0.5	–7.5	V	$V_{DS} = 15\ V$, $I_D = 200\ \mu A$	
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage		–8	V	$V_{DS} = 15\ V$, $I_D = 2\ nA$	
7	DYNAMIC	$\lvert y_{fs} \rvert$	Common-Source Forward Transfer Admittance	2000	6500	μmho	$V_{DS} = 15\ V$, $V_{GS} = 0$ (Note 2)	f = 1 kHz
8		$\lvert y_{os} \rvert$	Common Source Output Admittance		50	μmho		
9		C_{iss}	Common Source Input Capacitance		8	pF	$V_{DS} = 15\ V$, $V_{GS} = 0$	f = 1 MHz
10		C_{rss}	Common Source Reverse Transfer Capacitance		4	pF		
11		$\lvert y_{fs} \rvert$	Common Source Forward Transfer Admittance	1600		μmho	$V_{DS} = 15\ V$, $V_{GS} = 0$	f = 100 MHz

*JEDEC registered data

NH
NRL

NOTES:

1. Derate linearly to 125°C (free air temperature at a rate of 2 mW/°C).
2. Pulse tested pulse width = 100 ms, duty cycle ≤ 10%.

n-channel JFETs *designed for . . .*

- **Small-Signal Amplifiers**
- **Oscillators**

Siliconix

Performance Curves NRL
See Section 4

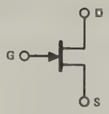
BENEFITS

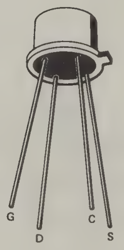
- Operates from High Supply Voltages
  $BV_{GSS} > 50$ V

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	–50 V
Gate Current	10 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature (Note 2)	300 mW
Storage Temperature Range	–65 to +200°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

TO-72
See Section 6





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3821		2N3822		2N3823		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1		-0.1		-0.5	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-0.1		-0.1		-0.5	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-30		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-4		-6		-8		V_{DS} = 15 V, I_D = 0.5 nA	
5		V_{GS}	Gate-Source Voltage	-0.5	-2						V_{DS} = 15 V, I_D = 50 μA	
						-1	-4				V_{DS} = 15 V, I_D = 200 μA	
								-1.0	-7.5		V_{DS} = 15 V, I_D = 400 μA	
6		I_{DSS}	Saturation Drain Current (Note 3)	0.5	2.5	2	10	4	20	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	1500	4500	3000	6500	3,500	6,500	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		$\|y_{fs}\|$	Common-Source Forward Transadmittance	1500		3000		3,200				f = 100 MHz
9		g_{os}	Common-Source Output Conductance (Note 3)		10		20		35			f = 1 kHz
10		C_{iss}	Common-Source Input Capacitance		6		6		6	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		2		2		2			
12		NF	Noise Figure		5		5		6	dB	V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1 meg, BW = 5 Hz	f = 10 Hz
13		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		200		200		200	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 15 V, V_{GS} = 0, BW = 5 Hz	

*JEDEC Registered Data.

NRL

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

2N3824

n-channel JFET designed for . . .

Performance Curves NRL
See Section 4

- High Speed Commutators
- Choppers

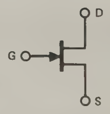
BENEFITS

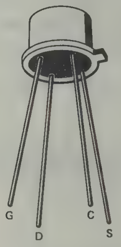
- Low Insertion Loss
  $r_{ds(on)} < 250\ \Omega$
- High Off-Isolation
  $I_{D(off)} < 0.1$ nA

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	–50 V
Gate Current	10 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature (Note 2)	300 mW
Storage Temperature Range	–65 to +200°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

TO-72
See Section 6





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-0.1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 μA, V_{DS} = 0	
4		$I_{D(off)}$	Drain Cutoff Current		0.1	nA	V_{DS} = 15 V, V_{GS} = -8 V	
					0.1	μA		150°C
5	DYNAMIC	$r_{ds(on)}$	Drain-Source ON Resistance		250	Ω	V_{GS} = 0 V, I_D = 0	f = 1 kHz
6		C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
7		C_{rss}	Common-Source Reverse Transfer Capacitance		3	pF	V_{GS} = -8 V, V_{DS} = 0	

*JEDEC registered data.

NRL

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.

dual n-channel JFETs *designed for . . .*

Siliconix

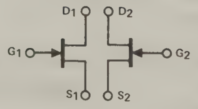
Performance Curves NNR
See Section 4

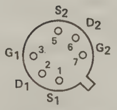
■ Differential Amplifiers

BENEFITS

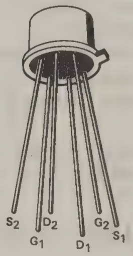
- Minimum System Error and Calibration
  5 mV Offset Maximum (2N3921)
- Simplifies Amplifier Design
  Low Output Conductance

TO-71
See Section 6





Bottom View



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	–50 V
Gate Current	50 mA
Total Device Dissipation (Derate 1.7 mW/°C to 200°C)	300 mW
Storage Temperature Range	–65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-1	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-1	μA		100°C
3		BV_{DGO}	Drain-Gate Breakdown Voltage	50		V	I_D = 1 μA, I_S = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-3		V_{DS} = 10 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.2	-2.7		V_{DS} = 10 V, I_D = 100 μA	
6		I_G	Gate Operating Current		-250	pA	V_{DG} = 10 V, I_D = 700 μA	
7					-25	nA		100°C
8		I_{DSS}	Saturation Drain Current (Note 1)	1	10	mA	V_{DS} = 10 V, V_{GS} = 0	
9	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	1500	7500	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
10		g_{os}	Common-Source Output Conductance		35			
11		C_{iss}	Common-Source Input Capacitance		18	pF		
12		C_{rss}	Common-Source Reverse Transfer Capacitance		6			
13		g_{fs}	Common-Source Forward Transconductance	1500		μmho	V_{DG} = 10 V, I_D = 700 μA	f = 1 kHz
14		g_{os}	Common-Source Output Conductance		20			
15		NF	Spot Noise Figure		2	dB	V_{DS} = 10 V, V_{GS} 0	f = 1 kHz, R_G = 1 meg

		Characteristic		2N3921		2N3922		2N4084		2N4085		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
16	MATCH	$\|V_{GS1}-V_{GS2}\|$	Differential Gate-Source Voltage		5		5		15		15	mV	V_{DG} = 10 V, I_D = 700 μA	
17		$\frac{\Delta\|V_{GS1}-V_{GS2}\|}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature (Note 2)		10		25		10		25	μV/°C		T_A = 0°C T_B = 100°C
18		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 3)	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	–		f = 1 kHz

*JEDEC registered data.

NNR

NOTES:

1. Pulse test duration = 2 ms.
2. Measured at end points; T_A and T_B.
3. Assumes smaller value in numerator.

2N3954 2N3954A 2N3955 2N3955A
PREFERRED PART 2N5196

Siliconix

matched dual n-channel JFETs *designed for . . .*

- **Low and Medium Frequency Differential Amplifiers**
- **High Input Impedance Amplifiers**

Performance Curves NQP
See Section 4

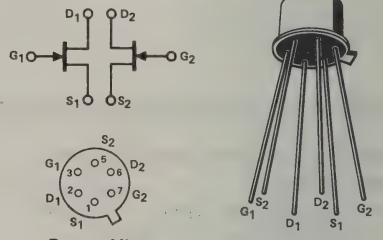
BENEFITS

- High Accuracy & Stability
  Offset Less Than 5 mV (2N3954, 54A)
  Drift Less Than 5 μV/°C (2N3954A)
- Wide Dynamic Range
  I_G Specified @ V_{DS} = 20 V
- Low Capacitance
  $C_{iss} < 4$ pF

ABSOLUTE MAXIMUM RATINGS (25°C)

Any Case-To-Lead Voltage		±100 V
Gate-Drain or Gate-Source Voltage		−50 V
Gate-To-Gate Voltage		±100 V
Gate Current		50 mA
Total Device Dissipation 85°C	(Each Side)	250 mW
Case Temperature	(Both Sides)	500 mW
Power Derating	(Each Side)	2.86 mW/°C
	(Both Sides)	4.3 mW/°C
Storage Temperature Range		−65 to +200°C
Lead Temperature (1/16″ from case for 10 seconds)		300°C

TO-71
See Section 6



Bottom View

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3954		2N3954A		2N3955		2N3955A		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		−100		−100		−100		−100	pA	V_{GS} = −30 V, V_{DS} = 0	
2					−500		−500		−500		−500	nA		T_A = 125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−50		−50		−50		−50		V	V_{DS} = 0, I_G = −1 μA	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−1.0	−4.5	−1.0	−4.5	−1.0	−4.5	−1.0	−4.5		V_{DS} = 20 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Forward Voltage		2.0		2.0		2.0		2.0		V_{DS} = 0, I_G = 1 mA	
6		V_{GS}	Gate-Source Voltage		−4.2		−4.2		−4.2		−4.2		V_{DS} = 20 V	I_D = 50 μA
7				−0.5	−4.0	−0.5	−4.0	−0.5	−4.0	−0.5	−4.0			I_D = 200 μA
8		I_G	Gate Operating Current		−50		−50		−50		−50	pA	V_{DS} = 20 V, I_D = 200 μA	
9					−250		−250		−250		−250	nA		T_A = 125°C
10		I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
11	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
12				1000		1000		1000		1000				f = 200 MHz
13		g_{os}	Common-Source Output Conductance		35		35		35		35			f = 1 kHz
14		C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0		4.0	pF		f = 1 MHz
15		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2		1.2			
16		C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		1.5		V_{DG} = 10 V, I_S = 0	
17		NF	Common Source Spot Noise Figure		0.5		0.5		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = 0, R_G = 10 MΩ	f = 100 Hz
18	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		10		10		10		10	nA	V_{DS} = 20 V, I_D = 200 μA,	T = 125°C
19		I_{DSS1}/I_{DSS2}	Saturation Drain Current Ratio (Note 1)	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	–	V_{DS} = 20 V V_{GS} = 0	
20		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5.0		5.0		10.0		5.0	mV	V_{DS} = 20 V, I_D = 200 μA	
21		$\Delta\lvert V_{GS1}-V_{GS2}\rvert$	Gate-Source Differential Voltage Change with Temperature		0.8		0.4		2.0		1.2			T = 25°C to −55°C
22					1.0		0.5		2.5		1.5			T = 25°C to 125°C
23		g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	0.97	1.0	0.97	1.0	0.97	1.0	0.95	1.0	–		f = 1 kHz

*JEDEC registered data
NOTE:
1. Assumes smaller value in numerator.

NQP

2N3956 2N3957 2N3958
PREFERRED PART 2N5196

matched dual n-channel JFETs designed for . . .

Siliconix

Performance Curves NQP
See Section 4

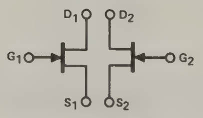
BENEFITS

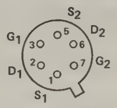
- Wide Dynamic Range
  I_G Specified @ V_{DS} = 20 V
- Low Capacitance
  $C_{iss} < 4$ pF

■ Low and Medium Frequency Differential Amplifiers

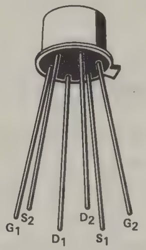
■ High Input Impedance Amplifiers

TO-71
See Section 6





Bottom View



*ABSOLUTE MAXIMUM RATINGS (25°C)

Any Lead-To-Case Voltage		±100 V
Gate-Drain or Gate-Source Voltage		-50 V
Gate-To-Gate Voltage		±100 V
Gate Current		50 mA
Total Device Dissipation 85°C	(Each Side)	250 mW
Case Temperature	(Both Sides)	500 mW
Power Derating	(Each Side)	2.86 mW/°C
	(Both Sides)	4.3 mW/°C
Storage Temperature Range		-65 to +250°C
Lead Temperature (1/16″ from case for 10 seconds)		300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3956		2N3957		2N3958		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	S T A T I C	I_{GSS}	Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-500		-500		-500	nA		T_A = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	V_{DS} = 0 V, I_G = -1 μA	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5		V_{DS} = 20 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Forward Voltage		2.0		2.0		2.0		V_{DS} = 0 V, I_G = 1 mA	
6		V_{GS}	Gate-Source Voltage		-4.2		-4.2		-4.2		V_{DS} = 20 V, I_D = 50 μA	
7				-0.5	-4.0	-0.5	-4.0	-0.5	-4.0		V_{DS} = 20 V, I_D = 200 μA	
8		I_G	Gate Operating Current		-50		-50		-50	pA	V_{DS} = 20 V, I_D = 200 μA	
9					-250		-250		-250	nA		T_A = 125°C
10		I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
11	D Y N A M I C	$\|y_{fs}\|$	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
12				1000		1000		1000				f = 200 MHz
13		g_{os}	Common-Source Output Conductance		35		35		35			f = 1 kHz
14		C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0	pF		f = 1 MHz
15		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2			
16		C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		V_{DG} = 10 V, I_S = 0	
17		NF	Common-Source Spot Noise Figure		0.5		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = 0 V, R_G = 10 MΩ	f = 100 Hz
18	M A T C H I N G	$\|I_{G1}-I_{G2}\|$	Differential Gate Reverse Current		10		10		10	nA	V_{DS} = 20 V, I_D = 200 μA	T = 125°C
19		I_{DSS1}/I_{DSS2}	Saturation Drain Current Ratio (Note 1)	0.95	1.0	0.90	1.0	0.85	1.0	—	V_{DS} = 20 V, V_{GS} = 0	
20		$\|V_{GS1}-V_{GS2}\|$	Differential Gate-Source Voltage		15		20		25	mV	V_{DS} = 20 V, I_D = 200 μA	
21		$\Delta\|V_{GS1}-V_{GS2}\|$	Gate-Source Voltage Differential Change With Temperature		4.0		6.0		8.0			T = 25°C to -55°C
22					5.0		7.5		10.0			T = 25°C to 125°C
23		g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	0.95	1.0	0.90	1.0	0.85	1.0	—		f = 1 kHz

*JEDEC registered data

NOTE:

1. Assumes smaller value in numerator.

NQP

Siliconix

n-channel JFETs
designed for . . .

- **Analog Switches**
- **Choppers**
- **Amplifiers**

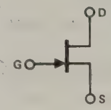
Performance Curves NCA
See Section 4

BENEFITS

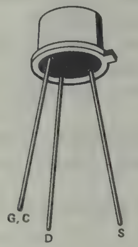
- Low Insertion Loss $r_{DS(on)} < 30\ \Omega$ (2N3970)
- Good Off-Isolation $I_{D(off)} < 250$ pA

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . −40 V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Note 1) . . . . 1.8 W
Storage Temperature Range . . . . −65 to +200°C
Lead Temperature
(1/16″ from case for 60 seconds) . . . . 300°C



TO-18
See Section 6

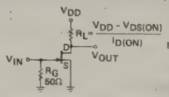


*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3970		2N3971		2N3972		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	BV_{GSS}	Gate Reverse Breakdown Voltage	-40		-40		-40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2		I_{DGO}	Drain Reverse Current		250		250		250	pA	$V_{DG} = 20$ V, $I_S = 0$	
3					500		500		500	nA		150°C
4		$I_{D(off)}$	Drain Cutoff Current		250		250		250	pA	$V_{DS} = 20$ V, $V_{GS} = -12$ V	
5					500		500		500	nA		150°C
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3	V	$V_{DS} = 20$ V, $I_D = 1$ nA	
7		I_{DSS}	Saturation Drain Current (Pulsewidth 300 μs, duty cycle ⩽ 3%)	50	150	25	75	5	30	mA	$V_{DS} = 20$ V, $V_{GS} = 0$	
8		$V_{DS(on)}$	Drain-Source ON Voltage						2	V	$V_{GS} = 0$	$I_D = 5$ mA
9							1.5					$I_D = 10$ mA
10					1							$I_D = 20$ mA
11		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0$, $I_D = 1$ mA	
12	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
13		C_{iss}	Common-Source Input Capacitance		25		25		25	pF	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance		6		6		6		$V_{DS} = 0$, $V_{GS} = -12$ V	
15	SW	$t_{d(on)}$	Turn-On Delay Time		10		15		40	ns	$V_{DD} = 10$ V, $V_{GS(on)} = 0$ $I_{D(on)}$ R_L $V_{GS(off)}$ 2N3970 20 mA 450 Ω -10 V 2N3971 10 mA 850 Ω - 5 V 2N3972 5 mA 1.6KΩ - 3 V	
16		t_r	Rise Time		10		15		40			
17		t_{off}	Turn-Off Time		30		60		100			

*JEDEC registered data.

NOTE:
1. Derate linearly at the rate of 10 mW/°C.



NCA

INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 200 ns
PULSE RATE 550 pps

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.5 pF

2N4091 2N4092 2N4093 JAN TX PLASTIC EQUIVALENT PN4091 SERIES

n-channel JFETs *designed for . . .*

Siliconix

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

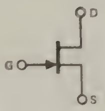
Performance Curves NCA
See Section 4

BENEFITS

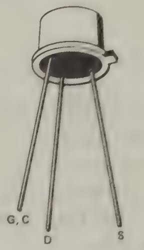
- Low Insertion Loss
  High Accuracy in Test Systems
  $r_{DS(on)} < 30\ \Omega$ (2N4091)
- High Off-Isolation
  $I_{D(off)} < 200$ pA
- High Speed
  $t_{rise} < 10$ ns (2N4091)
- Short Sample and Hold Aperture Time
  $C_{rss} < 5$ pF

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage	−40 V
Gate Current	10 mA
Total Device Dissipation at 25°C Case Temperature (Derate 10 mW/°C)	1.8 W
Storage Temperature Range	−55 to +200°C
Lead Temperature (1/16″ from case for 60 seconds)	300°C



TO-18
See Section 6



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

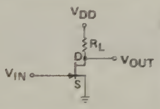
		Characteristic		2N4091		2N4092		2N4093		Unit	Test Conditions		
				Min	Max	Min	Max	Min	Max				
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		−40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$		
2		I_{DGO}	Drain Reverse Current		200		200		200	pA	$V_{GS} = -20$ V, $I_S = 0$		
3					400		400		400	nA			150°C
4		$I_{D(off)}$	Drain Cutoff Current						200	pA	$V_{DS} = 20$ V	$V_{GS} = -6$ V	
5									400	nA			150°C
6							200			pA		$V_{GS} = -8$ V	
7							400			nA			150°C
8					200					pA		$V_{GS} = -12$ V	
9					400					nA			150°C
10		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−5	−10	−2	−7	−1	−5	V	$V_{DS} = 20$ V, $I_D = 1$ nA		
11		I_{DSS}	Saturation Drain Current (Note 1)	30		15		8		mA	$V_{DS} = 20$ V, $V_{GS} = 0$		
12		$V_{DS(on)}$	Drain-Source ON Voltage						0.2	V	$V_{GS} = 0$	$I_D = 2.5$ mA	
13							0.2					$I_D = 4$ mA	
14					0.2							$I_D = 6.6$ mA	
15		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		50		80	Ω	$V_{GS} = 0$, $I_D = 1$ mA		
16	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		30		50		80	Ω	$V_{GS} = 0$, $I_D = 0$		f = 1 kHz
17		C_{iss}	Common-Source Input Capacitance		16		16		16	pF	$V_{DS} = 20$ V, $V_{GS} = 0$		f = 1 MHz
18		C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5		$V_{DS} = 0$, $V_{GS} = -20$ V		
19	SW	$t_{d(on)}$	Turn-ON Delay Time		15		15		20	ns	$V_{DD} = 3$ V, $V_{GS(on)} = 0$		
20		t_r	Rise Time		10		20		40				
21		t_{off}	Turn-OFF Time		40		60		80				

	$I_{D(on)}$	$V_{GS(off)}$	R_L
2N4091	6.6 mA	−12 V	425 Ω
2N4092	4	−8	700
2N4093	2.5	−6	1120

NCA

*JEDEC registered data.

NOTE:
1. Pulsewidth = 300 µs, duty cycle ≤ 3%.



INPUT PULSE
RISE TIME < 1 ns
FALL TIME < 1 ns
PULSE WIDTH 1 µs
PULSE DUTY CYCLE < 10%
PULSE GENERATOR IMPEDANCE 50Ω

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.7 pF

2N4117 2N4117A 2N4118 2N4118A 2N4119 2N4119A
PREFERRED PARTS FN4117 SERIES, PLASTIC EQUIVALENT PN4117 SERIES

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NT
See Section 4

- **Ultra-High Input Impedance Amplifiers**
  - **Electrometers**
  - **pH Meters**
  - **Smoke Detectors**

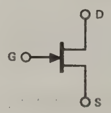
BENEFITS

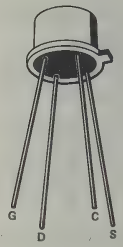
- Low Power
  $I_{DSS} < 90\ \mu A$ (2N4117)
- Minimum Circuit Loading
  $I_{GSS} < 1$ pA (2N4117A Series)

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	–40 V
Gate-Current	50 mA
Total Device Dissipation (Derate 2 mW/°C to 175°C)	300 mW
Storage Temperature Range	–65 to +175°C
Lead Temperature (1/16″ from case for 10 seconds)	255°C

TO-72
See Section 6





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4117 2N4117A		2N4118 2N4118A		2N4119 2N4119A		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current 2N4117 Series Only		–10		–10		–10	pA	V_{GS} = –20 V, V_{DS} = 0	
2					–25		–25		–25	nA		150°C
3		I_{GSS}	Gate Reverse Current 2N4117A Series Only		–1		–1		–1	pA	V_{GS} = –20 V, V_{DS} = 0	
4					–2.5		–2.5		–2.5	nA		150°C
5		BV_{GSS}	Gate-Source Breakdown Voltage	–40		–40		–40		V	I_G = –1 μA, V_{DS} = 0	
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.6	–1.8	–1	–3	–2	–6		V_{DS} = 10 V, I_D = 1 nA	
7		I_{DSS}	Saturation Drain Current (Note 2)	0.03	0.09	0.08	0.24	0.20	0.60	mA	V_{DS} = 10 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	70	210	80	250	100	330	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
9		g_{os}	Common-Source Output Conductance		3		5		10			
10		C_{iss}	Common-Source Input Capacitance		3		3		3	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5		1.5			

NT

*JEDEC registered data.

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. This parameter is measured during a 2 ms interval 100 ms after power is applied. (Not a JEDEC condition.)

n-channel JFETs *designed for . . .*

- **Small-Signal Amplifiers**
- **VHF Amplifiers**
- **Oscillators**
- **Mixers**

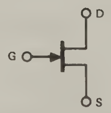
Performance Curves NRL
See Section 4

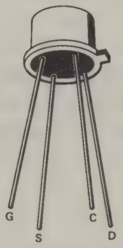
BENEFITS
- High Gain
- Low Receiver Noise Figure

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	−30 V
Gate Current	10 mA
Drain Current	15 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature (Note 2)	300 mW
Storage Temperature Range	−65 to +200°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

TO-72
See Section 6





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	2N4220, 2N4220A		2N4221, 2N4221A		2N4222, 2N4222A		Units	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		−0.1		−0.1		−0.1	nA	V_{GS} = −15 V, V_{DS} = 0	
2					−0.1		−0.1		−0.1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−30		−30		−30		V	I_G = −10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		−4		−6		−8		V_{DS} = 15 V, I_D = 0.1 nA	
5		V_{GS}	Gate-Source Voltage	−0.5	−2.5	−1	−5	−2	−6	V	V_{DS} = 15 V, I_D = ( )	
				(50)	(50)	(200)	(200)	(500)	(500)	(μA)		
6		I_{DSS}	Saturation Drain Current (Note 3)	0.5	3	2	6	5	15	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	1000	4000	2000	5000	2500	6000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		$\|y_{fs}\|$	Common-Source Forward Transadmittance	750		750		750				f = 100 MHz
9		g_{os}	Common-Source Output Conductance (Note 3)		10		20		40			f = 1 kHz
10		C_{iss}	Common-Source Input Capacitance		6		6		6	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		2		2		2			
12		NF	Noise Figure, Only 2N4220A, 2N4221A, 2N4222A		2.5		2.5		2.5	dB	V_{DS} = 15 V, V_{GS} = 0 R_{gen} = 1 meg	f = 100 Hz

*JEDEC registered data.

NRL

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

Siliconix

n-channel JFETs *designed for . . .*

Performance Curves NRL
See Section 4

■ VHF Amplifiers

■ Mixers

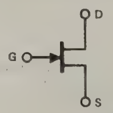
BENEFITS

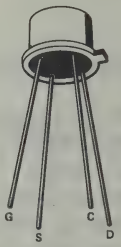
- Low Noise
  NF = 3 dB Typical @ 200 MHz
- Easy Tuning
  $C_{rss} < 2$ pF

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . -30 V
Gate Current . . . . 10 mA
Drain Current . . . . 20 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature (Note 2) . . . . 300 mW
Storage Temperature Range . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . 300°C

TO-72
See Section 6





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4223		2N4224		Unit	Test Conditions	
				Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-0.25		-0.5	nA	V_{GS} = -20 V, V_{DS} = 0	
2					-0.25		-0.5	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		V	I_G = -10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.1	-8	-0.1	-8	V	V_{DS} = 15 V, I_D = ( )	
				(0.25)	(0.25)	(0.5)	(0.5)	(nA)		
5		V_{GS}	Gate-Source Voltage	-1.0	-7.0	-1.0	-7.5	V		
				(0.3)	(0.3)	(0.2)	(0.2)	(mA)		
6		I_{DSS}	Saturation Drain Current (Note 3)	3	18	2	20	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYN	g_{fs}	Common-Source Forward Transconductance (Note 3)	3000	7000	2000	7500	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		C_{iss}	Common-Source Input Capacitance (Output Shorted)		6		6	pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		2		2			
10	HIGH FREQ	$\|y_{fs}\|$	Common-Source Forward Transadmittance	2700		1700		μmho	V_{DS} = 15 V, V_{GS} = 0	f = 200 MHz
11		g_{iss}	Common-Source Input Conductance (Output Shorted)		800		800			
12		g_{oss}	Common-Source Output Conductance (Input Shorted)		200		200			
13		G_{ps}	Small Signal Power Gain	10				dB		
14		NF	Noise Figure		5				V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1 K	

*JEDEC registered data.

NRL

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NPA
See Section 4

- **Small-Signal Amplifiers**
- **Choppers**
- **Voltage-Controlled Resistors**

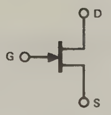
BENEFITS

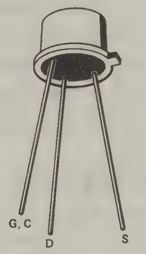
- Low Noise
  NF < 1 dB at 1 kHz
- Operation from Low Power Supply Voltages
  $V_{GS(off)} < 1$ V (2N4338)
- Simple Biasing Design with Tightly Specified Parameter Tolerances
  3:1 I_{DSS}, V_P, g_{fs} Ranges
- High Off-Isolation as a Switch
  $I_{D(off)} < 50$ pA

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	–50 V
Gate Current	50 mA
Total Device Dissipation (Note 2)	300 mW
Storage Temperature Range	–65 to +200°C
Maximum Operating Temperature	175°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-18
See Section 6





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

		Characteristic		2N4338		2N4339		2N4340		2N4341		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		–0.1		–0.1		–0.1		–0.1	nA	$V_{GS} = -30$ V, $V_{DS} = 0$	
2					–0.1		–0.1		–0.1		–0.1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–50		–50		–50		–50		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.3	–1	–0.6	–1.8	–1	–3	–2	–6		$V_{DS} = 15$ V, $I_D = 0.1\ \mu A$	
5		$I_D(off)$	Drain Cutoff Current		0.05 (–5)		0.05 (–5)		0.05 (–5)		0.07 (–10)	nA (V)	$V_{DS} = 15$ V $V_{GS} = (\quad)$	
6		I_{DSS}	Saturation Drain Current (Note 3)	0.2	0.6	0.5	1.5	1.2	3.6	3	9	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	600	1800	800	2400	1300	3000	2000	4000	μmho	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 kHz
8		g_{os}	Common-Source Output Conductance		5		15		30		60			
9		$r_{ds(on)}$	Drain-Source ON Resistance		2500		1700		1500		800	ohm	$V_{DS} = 0$, $V_{GS} = 0$	
10		C_{iss}	Common-Source Input Capacitance		7		7		7		7	pF	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		3		3		3		3			
12		NF	Noise Figure		1		1		1		1	dB	$V_{DS} = 15$ V, $V_{GS} = 0$ $R_{gen} = 1$ meg, BW = 200 Hz	f = 1 kHz

*JEDEC registered data

NPA

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 125 msec (I_{DSS}) and 625 msec (g_{fs}) after d–c power is applied. (Not a JEDEC condition.)

2N4391 2N4392 2N4393
PREFERRED PARTS FN4392 SERIES, PLASTIC EQUIVALENT PN4391 SERIES

n-channel JFETs *designed for . . .*

Siliconix

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Performance Curves NCA
See Section 4

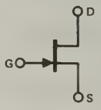
BENEFITS

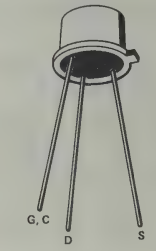
- Low Insertion Loss, High Accuracy in Test Systems $r_{DS(on)} < 30\ \Omega$ (2N4391)
- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- High Off-Isolation $I_{D(off)} < 100$ pA
- High Speed $t_{ON} < 20$ ns

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . −40 V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Derate 10 mW/°C) . . . . 1.8 W
Storage Temperature Range . . . . −65 to +200°C
Lead Temperature
(1/16'' from case for 60 seconds) . . . . .300°C

TO-18
See Section 6





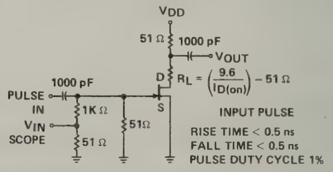
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4391		2N4392		2N4393		Unit	Test Conditions		
				Min	Max	Min	Max	Min	Max				
1	STATIC	I_{GSS}	Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -20 V, V_{DS} = 0		
2					-200		-200		-200	nA			150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0		
4		$I_{D(off)}$	Drain Cutoff Current						100	pA	V_{DS} = 20 V	V_{GS} = -5 V	
5									200	nA			150°C
6							100			pA		V_{GS} = -7 V	
7							200			nA			150°C
8					100					pA		V_{GS} = -12 V	
9					200					nA			150°C
10		$V_{GS(f)}$	Gate-Source Forward Voltage		1		1		1	V	I_G = 1 mA, V_{DS} = 0		
11		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3		V_{DS} = 20 V, I_D = 1 nA		
12		I_{DSS}	Saturation Drain Current (Note 1)	50	150	25	75	5	30	mA	V_{DS} = 20 V, V_{GS} = 0		
13		$V_{DS(on)}$	Drain Source ON-Voltage						0.4	V	V_{GS} = 0	I_D = 3 mA	
14							0.4					I_D = 6 mA	
15					0.4							I_D = 12 mA	
16		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 1 mA		
17	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 0		f = 1 kHz
18		C_{iss}	Common-Source Input Capacitance		14		14		14	pF	V_{DS} = 20 V, V_{GS} = 0		f = 1 MHz
19		C_{rss}	Common-Source Reverse Transfer Capacitance						3.5		V_{DS} = 0	V_{GS} = - 5 V	
20							3.5					V_{GS} = - 7 V	
21					3.5							V_{GS} = -12 V	
22	SW	$t_{d(on)}$	Turn-ON Delay Time		15		15		15	ns	V_{DD} = 10 V, $V_{GS(on)}$ = 0		
23		t_r	Rise Time		5		5		5			$I_{D(on)}$	$V_{GS(off)}$ R_L
24		$t_{d(off)}$	Turn-OFF Delay Time		20		35		50		2N4391	12 mA	-12 V
25		t_f	Fall Time		15		20		30		2N4392 2N4393	6 3	-7 -5

*JEDEC registered data.

NOTE:
1. Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%.

NCA



INPUT PULSE
RISE TIME < 0.5 ns
FALL TIME < 0.5 ns
PULSE DUTY CYCLE 1%

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 50 Ω

n-channel JFETs *designed for . . .*

Siliconix

2N4416 2N4416A PLASTIC EQUIVALENT PN4416

- **VHF Amplifiers**
- **Mixers**

Performance Curves NH
See Section 4

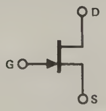
BENEFITS

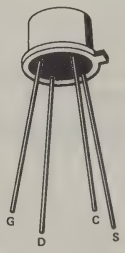
- Low Noise
  NF = 3 dB Typical at 400 MHz
- Wide Band
  High g_{fs}/C_{iss} Ratio

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage, 2N4416 . . . . –30 V
Gate-Drain or Gate-Source Voltage, 2N4416A . . . . . . –35 V
Gate Current . . . . 10 mA
Total Device Dissipation (Derate 1.7 mW/°C) . . . . . 300 mW
Storage Temperature Range . . . . –65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . 300°C

TO-72
See Section 6





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1	nA	V_{GS} = –20 V, V_{DS} = 0 V	
2					-0.1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		V	I_G = –1 μA, V_{DS} = 0 V	2N4416
				-35				2N4416A
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-6	V	V_{DS} = 15 V, I_D = 1 nA	2N4416
				-2.5	-6			2N4416A
5		I_{DSS}	Saturation Drain Current (Note 1)	5	15	mA	V_{DS} = 15 V, V_{GS} = 0 V	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4500	7500	μmho		f = 1 kHz
7		g_{os}	Common-Source Output Conductance		50	μmho		
8		C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	pF		f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		4	pF		
10		C_{oss}	Common-Source Output Capacitance		2			

		Characteristic		100 MHz		400 MHz		Unit	Test Conditions
				Min	Max	Min	Max		
11	HIGH FREQUENCY	g_{iss}	Common-Source Input Conductance		100		1000	μmho	V_{DS} = 15 V, V_{GS} = 0 V
12		b_{iss}	Common-Source Input Susceptance		2500		10,000	μmho	
13		g_{oss}	Common-Source Output Conductance		75		100	μmho	
14		b_{oss}	Common-Source Output Susceptance		1000		4000	μmho	
15		g_{fs}	Common-Source Forward Transconductance			4000		μmho	
16		G_{ps}	Common-Source Power Gain	18		10		dB	V_{DS} = 15 V, I_D = 5 mA
17		NF	Noise Figure		2		4	dB	V_{DS} = 15 V, I_D = 5 mA, R_G = 1K Ω

*JEDEC Registered data

NH

NOTES:
1. Pulse test duration = 300 μs.

2N4856 2N4857 2N4858 2N4859 2N4860 2N4861 JAN TX

n-channel JFETs
designed for . . .

Siliconix

Performance Curves NCA
See Section 4

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

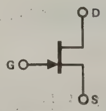
BENEFITS

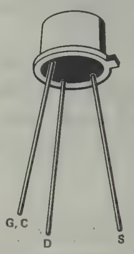
- Low Insertion Loss and High Accuracy in Test Systems
  $r_{DS(on)} < 25\ \Omega$ (2N4856, 59)
- High Off-Isolation
  $I_{D(off)} < 250$ pA
- High Speed
  $t_{ON} < 9$ ns

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage, 2N4856-58 . . . . –40 V
Reverse Gate-Drain or Gate-Source Voltage, 2N4859–61 . . . . –30 V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature (Derate 10 mW/°C) . . . . 1.8 W
Storage Temperature Range . . . . –65 to +200°C
Lead Temperature (1/16″ from case for 10 seconds) . . . . 300°C

TO-18
See Section 6



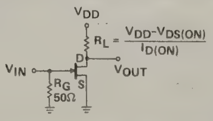


*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic			2N4856 2N4859		2N4857 2N4860		2N4858 2N4861		Unit	Test Conditions	
					Min	Max	Min	Max	Min	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	2N4856-58	–40		–40		–40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2				2N4859-61	–30		–30		–30				
3		I_{GSS}	Gate Reverse Current	2N4856-58		–250		–250		–250	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
4						–500		–500		–500	nA		150°C
5				2N4859-61		–250		–250		–250	pA	$V_{GS} = -15$ V, $V_{DS} = 0$	
6						–500		–500		–500	nA		150°C
7		$I_{D(off)}$	Drain Cutoff Current			250		250		250	pA	$V_{DS} = 15$ V, $V_{GS} = -10$ V	
8						500		500		500	nA		150°C
9		$V_{GS(off)}$	Gate-Source Cutoff Voltage		–4	–10	–2	–6	–0.8	–4	V	$V_{DS} = 15$ V, $I_D = 0.5$ nA	
10		I_{DSS}	Saturation Drain Current (Note 1)		50		20	100	8	80	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
11		$V_{DS(on)}$	Drain-Source ON Voltage			0.75 (20)		0.50 (10)		0.50 (5)	V (mA)	$V_{GS} = 0$, $I_D = (\ \ )$	
12	DYN	$r_{ds(on)}$	Drain-Source ON Resistance			25		40		60	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
13		C_{iss}	Common-Source Input Capacitance			18		18		18	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance			8		8		8			
15	SWITCHING	$t_{d(on)}$	Turn-ON Delay Time			6 (20) [–10]		6 (10) [–6]		10 (5) [–4]	ns (mA) [V]	$V_{DD} = 10$ V, $V_{GS(on)} = 0$, $I_{D(on)} = (\ \ )$, $V_{GS(off)} = [\ ]$	R_L = 464 Ω, 2N4856, 59 953 Ω, 2N4857, 60 1910 Ω, 2N4858, 61
16		t_r	Rise Time			3 (20) [–10]		4 (10) [–6]		10 (5) [–4]	ns (mA) [V]		
17		t_{off}	Turn-OFF Time			25 (20) [–10]		50 (10) [–6]		100 (5) [–4]	ns (mA) [V]		

*JEDEC registered data.

NOTE:
1. Pulse test required, pulsewidth = 100 μs, duty cycle ≤ 10%.



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 100 ns
PULSE DUTY CYCLE < 10%

SAMPLING SCOPE
RISE TIME 0.75 ns
INPUT RESISTANCE 1 M
INPUT CAPACITANCE 2.5 pF

NCA

n-channel JFETs
designed for . . .

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Siliconix

Performance Curves NCA
See Section 4

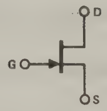
BENEFITS

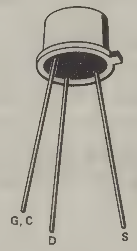
- Low Insertion Loss and High Accuracy in Test Systems
  $r_{DS(on)} < 25\ \Omega$ (2N4856A, 59A)
- High Off-Isolation
  $I_{D(off)} < 250$ pA
- Short Sample and Hold Aperture Time
  $C_{rss} < 4$ pF
- High Speed
  $t_{ON} < 8$ ns

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage,
2N4856A-58A . . . . −40 V
Reverse Gate-Drain or Gate-Source Voltage,
2N4859A-61A . . . . −30 V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Derate 10 mW/°C) . . . . 1.8 W
Storage Temperature Range . . . . −65 to +200°C
Lead Temperature
(1/16″ from case for 10 seconds) . . . . 300°C

TO-18
See Section 6





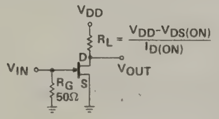
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic			2N4856A 2N4859A		2N4857A 2N4860A		2N4858A 2N4861A		Unit	Test Conditions	
					Min	Max	Min	Max	Min	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	2N4856A-58A	−40		−40		−40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2				2N4859A-61A	−30		−30		−30				
3		I_{GSS}	Gate Reverse Current	2N4856A-58A		−250		−250		−250	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
4						−500		−500		−500	nA		150°C
5				2N4859A-61A		−250		−250		−250	pA	$V_{GS} = -15$ V, $V_{DS} = 0$	
6						−500		−500		−500	nA		150°C
7		$I_{D(off)}$	Drain Cutoff Current			250		250		250	pA	$V_{DS} = 15$ V, $V_{GS} = -10$ V	
8						500		500		500	nA		150°C
9		$V_{GS(off)}$	Gate-Source Cutoff Voltage		−4	−10	−2	−6	−0.8	−4	V	$V_{DS} = 15$ V, $I_D = 0.5$ nA	
10		I_{DSS}	Saturation Drain Current (Note 1)		50		20	100	8	80	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
11		$V_{DS(on)}$	Drain-Source ON Voltage			0.75 (20)		0.50 (10)		0.50 (5)	V (mA)	$V_{GS} = 0$, $I_D = (\ \ )$	
12	DYN	$r_{ds(on)}$	Drain-Source ON Resistance			25		40		60	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
13		C_{iss}	Common-Source Input Capacitance			10		10		10	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance			4		3.5		3.5			
15	SWITCHING	$t_{d(on)}$	Turn-ON Delay Time			5 (20) [−10]		6 (10) [−6]		8 (5) [−4]	ns (mA) [V]	$V_{DD} = 10$ V, $V_{GS(on)} = 0$, $I_{D(on)} = (\ \ )$, $V_{GS(off)} = [\ ]$	$R_L =$ 464 Ω, 2N4856A, 59A 953 Ω, 2N4857A, 60A 1910 Ω, 2N4858A, 61A
16		t_r	Rise Time			3 (20) [−10]		4 (10) [−6]		8 (5) [−4]	ns (mA) [V]		
17		t_{off}	Turn-OFF Time			20 (20) [−10]		40 (10) [−6]		80 (5) [−4]	ns (mA) [V]		

NCA

*JEDEC registered data.

NOTE:
1. Pulse test required, pulsewidth = 100 μs, duty cycle ⩽ 10%.



INPUT PULSE	SAMPLING SCOPE
RISE TIME 0.25 ns	RISE TIME 0.75 ns
FALL TIME 0.75 ns	INPUT RESISTANCE 1 M
PULSE WIDTH 100 ns	INPUT CAPACITANCE 2.5 pF
PULSE DUTY CYCLE < 10%	

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NPA
See Section 4

- **Audio and Sub-Audio Amplifiers**

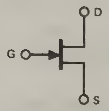
BENEFITS

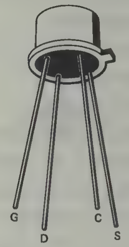
- Ultra Low Noise
  $\overline{e}_n$ = 8 nV/$\sqrt{Hz}$ Typical at 10 Hz
  $\overline{e}_n$ = 2 nV/$\sqrt{Hz}$ Typical at 1 kHz

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Souce Voltage (Note 1) . . . –40 V
Gate Current or Drain Current . . . . 50 mA
Total Device Dissipation
(Derate 1.7 mW/°C) . . . . 300 mW
Storage Temperature Range . . . . –65°C to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . .300°C

TO-72
See Section 6





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	2N4867 2N4867A		2N4868 2N4868A		2N4869 2N4869A		Unit	Test Conditions		
				Min	Max	Min	Max	Min	Max				
1	STATIC	I_{GSS}	Gate Reverse Current		-0.25		-0.25		-0.25	nA	V_{GS} = -30 V, V_{DS} = 0		
2					-0.25		-0.25		-0.25	μA		150°C	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0		
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-2	-1	-3	-1.8	-5		V_{DS} = 20 V, I_D = 1 μA		
5		I_{DSS}	Saturation Drain Current (Note 2)	0.4	1.2	1	3	2.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0		
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	700	2000	1000	3000	1300	4000	μmho	V_{DS} = 20 V, V_{GS} = 0		f = 1 kHz
7		g_{os}	Common-Source Output Conductance		1.5		4		10				
8		C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5	pF			f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		25		25		25				
10		$\overline{e}_n$	Short Circuit Equivalent Input Noise Voltage		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	2N4867 Series	f = 10 Hz
11					10		10		10			2N4867A Series	
12					10		10		10			2N4867 Series	f = 1 kHz
13					5		5		5			2N4867A Series	
14		NF	Spot Noise Figure		1		1		1	dB	V_{DS} = 10 V, V_{GS} = 0 R_{gen} = 20 K, 2N4867 Series 5 K, 2N4867A Series		f = 1 kHz

*JEDEC registered data.

NPA

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Pulse test duration = 2 ms.

p-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**

Siliconix

Performance Curves PSA
See Section 4

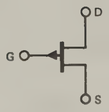
BENEFITS

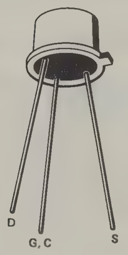
- Low Insertion Loss
  $r_{DS(on)} < 75\ \Omega$ (2N5018)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage (Note 1)	30 V
Gate Current	50 mA
Total Device Dissipation, Free-Air (Derate 3 mW/°C)	500 mW
Storage Temperature Range	–65 to +200°C
Lead Temperature (1/16" from case for 60 seconds)	300°C

TO-18
See Section 6



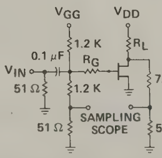


*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5018		2N5019		Unit	Test Conditions	
				Min	Max	Min	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30		30		V	$I_G = 1\ \mu A$, $V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current		2		2	nA	$V_{GS} = 15$ V, $V_{DS} = 0$	
3		$I_{D(off)}$	Drain Cutoff Current		–10		–10		$V_{DS} = -15$ V, $V_{GS} = 12$ V (2N5018)	
4					–10		–10	µA	$V_{GS} = 7$ V (2N5019)	150°C
5		I_{DGO}	Drain Reverse Current		–2		–2	nA	$V_{DG} = -15$ V, $I_S = 0$	
6					–3		–3	µA		150°C
7		$V_{GS(off)}$	Gate-Source Cutoff Voltage		10		5	V	$V_{DS} = -15$ V, $I_D = -1\ \mu A$	
8		I_{DSS}	Saturation Drain Current	–10		–5		mA	$V_{DS} = -20$ V, $V_{GS} = 0$	
9		$V_{DS(on)}$	Drain-Source ON Voltage		–0.5		–0.5	V	$V_{GS} = 0$, $I_D = -6$ mA (2N5018), $I_D = -3$ mA (2N5019)	
10	DYN	$r_{DS(on)}$	Static Drain-Source ON Resistance		75		150	Ω	$I_D = -1$ mA, $V_{GS} = 0$	
11		$r_{ds(on)}$	Drain-Source ON Resistance		75		150	Ω	$I_D = 0$, $V_{GS} = 0$	f = 1 kHz
12		C_{iss}	Common-Source Input Capacitance		45		45	pF	$V_{DS} = -15$ V, $V_{GS} = 0$	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		10		10		$V_{DS} = 0$, $V_{GS} = 12$ V (2N5018), $V_{GS} = 7$ V (2N5019)	
14	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	$V_{DD} = -6$ V, $V_{GS(on)} = 0$ $V_{GS(off)}$ $I_{D(on)}$ R_L 2N5018 12 V –6 mA 910 Ω 2N5019 7 V –3 mA 1.8K Ω	
15		t_r	Rise Time		20		75			
16		$t_{d(off)}$	Turn-OFF Delay Time		15		25			
17		t_f	Fall Time		50		100			

*JEDEC registered data.

NOTE:
1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.



PSA

INPUT PULSE
RISE TIME < 1 ns
FALL TIME < 1 ns
PULSE WIDTH 100 ns
REPETITION RATE 1 MHz

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 MΩ
INPUT CAPACITANCE 1.5 pF

monolithic dual n-channel JFETs *designed for . . .*

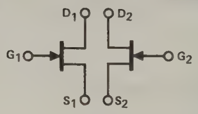
- **High Gain Differential Amplifiers**

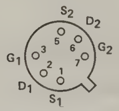
Performance Curves NQP
See Section 4

BENEFITS

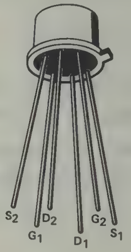
- Minimum System Error and Calibration
  5 mV Offset Maximum (2N5045)
- Low Drift
  5 mV Drift Maximum (2N5045)

TO-71
See Section 6





Bottom View



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	–50 V
Forward Gate Current	30 mA
Total Dissipation (25°C Free Air Temp.)	400 mW
Power Derating (to 175°C)	2.67 mW/°C
Storage Temperature Range	–65 to +200°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic (Note 1)		2N5045		2N5046		2N5047		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-1		-1		-1	μA	V_{GS} = -50 V, V_{DS} = 0 V	
2					-0.25		-0.25		-0.25	nA	V_{GS} = -30 V, V_{DS} = 0 V	
3					-250		-250		-250			T = 150°C
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-4.5	-0.5	-4.5	-0.5	-4.5	V	V_{DS} = 15 V, I_D = 0.5 nA	
5		I_{DSS}	Drain Saturation Current	0.5	8.0	0.5	8.0	0.5	8.0	mA		
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1.5	6.0	1.5	6.0	1.5	6.0	mmho	V_{DS} = 15 V, V_{GS} = 0 V	f = 1 kHz
7		$\lvert y_{fs} \rvert$	Common-Source Forward Admittance	1.5		1.5		1.5				f = 100 MHz
8		g_{os}	Common-Source Output Conductance		25		25		25	μmho		f = 1 kHz
9		C_{iss}	Common-Source Input Capacitance		8.0		8.0		8.0	pF		f = 1 MHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance		4.0		4.0		4.0			
11		NF	Spot Noise Figure		5.0		5.0			dB		f = 10 Hz, R_G = 1 MΩ
12		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		200		200			$\frac{nV}{\sqrt{Hz}}$		f = 10 Hz
13	MATCHING	$\lvert I_{GSS1}-I_{GSS2} \rvert$	Differential Gate Current		10		10		10	nA	V_{GS} = -15 V, V_{DS} = 0 V	T_A = 100°C
14		I_{DSS1}/I_{DSS2}	Drain Current Ratio (Note 2)	0.95	1.0	0.9	1.0	0.8	1.0	—	V_{GS} = 0 V, V_{DS} = 15 V	
15		$\lvert V_{GS1}-V_{GS2} \rvert$	Differential Gate-Source Voltage		5		10		15	mV	V_{DS} = 15 V	I_D = 50 μA
16					5		10		15			I_D = 200 μA
17		$\Delta\lvert V_{GS1}-V_{GS2} \rvert$	Gate-Source Voltage Differential Drift (Note 3)		5		10		15		V_{DS} = 15 V, I_D = 200 μA, T_A = 25°C	T_B = -25°C
18					5		10		15			T_B = 100°C
19		g_{fs1}/g_{fs2}	Transconductance Ratio (Note 2)	0.95	1.0	0.9	1.0	0.8	1.0	—	V_{DS} = 15 V, I_D = 200 μA	f = 1 kHz
20		$\lvert g_{os1}-g_{os2} \rvert$	Diff. Output Conductance		1.0		2.0		3.0	μmho		

*JEDEC registered data.

NOTES:
1. Individual FET characteristics. The terminals of the FET not under test are open-circuited for these measurements..
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.

NQP

p-channel JFETs *designed for . . .*

Siliconix

Performance Curves PSA
See Section 4

2N5114 2N5115 2N5116 (JAN PENDING)

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

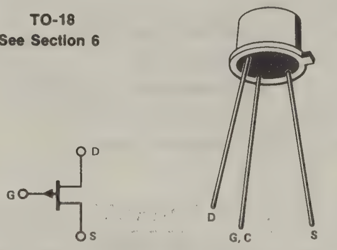
BENEFITS

- Simplifies Series-Shunt Switching when Combined with 2N4393, its N-Channel Complement
- Low Insertion Loss in Switching Systems $r_{DS(on)} < 75\ \Omega$ (2N5114)
- Short Sample and Hold Aperture Time $C_{rss} < 7$ pF
- High Off-Isolation $I_{D(off)} < 500$ pA

*ABSOLUTE MAXIMUM RATINGS (25° C)

Reverse Gate-Drain or Gate-Source Voltage (Note 1)	30 V
Gate Current	.50 mA
Total Device Dissipation, Free-Air (Derate 3 mW/°C)	500 mW
Storage Temperature Range	–65 to +200°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

TO-18
See Section 6

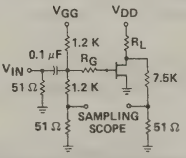


*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	2N5114		2N5115		2N5116		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	$I_G = 1\ \mu A, V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current		500		500		500	pA	$V_{GS} = 20\ V, V_{DS} = 0$	
3					1.0		1.0		1.0	μA		150°C
4		$I_{D(off)}$	Drain Cutoff Current		-500		-500		-500	pA	$V_{DS} = -15\ V, V_{GS} = 12\ V$ (2N5114) $V_{GS} = 7\ V$ (2N5115), $V_{GS} = 5\ V$ (2N5116)	
5					-1.0		-1.0		-1.0	μA		150°C
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	5	10	3	6	1	4	V	$V_{DS} = -15\ V, I_D = -1\ nA$	
7		I_{DSS}	Saturation Drain Current (Note 2)	-30	-90	-15	-60	-5	-25	mA	$V_{GS} = 0, V_{DS} = -18\ V$ (2N5114) $V_{DS} = -15\ V$ (2N5115, 2N5116)	
8		$V_{GS(f)}$	Forward Gate-Source Voltage		-1		-1		-1	V	$I_G = -1\ mA, V_{DS} = 0$	
9		$V_{DS(on)}$	Drain-Source ON Voltage		-1.3		-0.8		-0.6		$V_{GS} = 0, I_D = -15\ mA$ (2N5114) $I_D = -7\ mA$ (2N5115), $I_D = -3\ mA$ (2N5116)	
10		$r_{DS(on)}$	Static Drain-Source ON Resistance		75		100		150	Ω	$V_{GS} = 0, I_D = -1\ mA$	
11	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		75		100		150	Ω	$V_{GS} = 0, I_D = 0$	f = 1 kHz
12		C_{iss}	Common-Source Input Capacitance		25		25		25	pF	$V_{DS} = -15, V_{GS} = 0$	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		7		7		7		$V_{DS} = 0, V_{GS} = 12\ V$ (2N5114) $V_{GS} = 7\ V$ (2N5115), $V_{GS} = 5\ V$ (2N5116)	
14	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		6		10		12	ns		
15		t_r	Rise Time		10		20		30			
16		$t_{d(off)}$	Turn-OFF Delay Time		6		8		10			
17		t_f	Fall Time		15		30		50			

	2N5114	2N5115	2N5116
V_{DD}	-10 V	-6 V	-6 V
$V_{GS(off)}$	12 V	7 V	5 V
R_L	580 Ω	743 Ω	1800 Ω
$V_{GS(on)}$	0	0	0
$I_{D(on)}$	-15 mA	-7 mA	-3 mA

PSA



INPUT PULSE	SAMPLING SCOPE
RISE TIME < 1 ns	RISE TIME 0.4 ns
FALL TIME < 1 ns	INPUT RESISTANCE 10 MΩ
PULSE WIDTH 100 ns	INPUT CAPACITANCE 1.5 pF
REPETITION RATE 1 MHz	

*JEDEC registered data.

NOTES:

1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
2. Pulse Test PW 300 μs, duty cycle ⩽ 3%.

2N5196 2N5197 2N5198 2N5199

monolithic dual n-channel JFETs *designed for . . .*

- **Differential Amplifiers**
- **FET Input Op Amps**

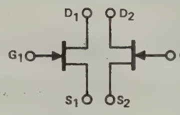
Siliconix

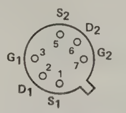
Performance Curves NQP
See Section 4

BENEFITS

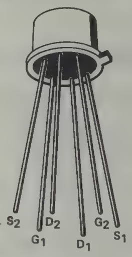
- Minimum System Error and Calibration
  5 mV Maximum Offset (2N5196, 97)
- Low Drift
  5 µV/°C Maximum (2N5196)
- Simplifies Amplifier Design
  Low Output Conductance

TO-71
See Section 6





Bottom View



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . -50 V
Gate Current . . . . 50 mA
Device Dissipation (Each Side), $T_A = 85°C$
(Derate 2.56 mW/°C) . . . . 250 mW
Total Device Dissipation, $T_A = 85°C$
(Derate 4.3 mW/°C) . . . . 500 mW
Storage Temperature Range . . . . -65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	S T A T I C	I_{GSS}	Gate Reverse Current		-25	pA	$V_{GS} = -30$ V, $V_{DS} = 0$	
2					-50	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	$I_G = -1$ µA, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-4		$V_{DS} = 20$ V, $I_D = 1$ nA	
5		V_{GS}	Gate-Source Voltage	-0.2	-3.8		$V_{DG} = 20$ V, $I_D = 200$ µA	
6		I_G	Gate Operating Current		-15	pA		
					-15	nA		125°C
7		I_{DSS}	Saturation Drain Current	0.7	7	mA	$V_{DS} = 20$ V, $V_{GS} = 0$	
8	D Y N A M I C	g_{fs}	Common-Source Forward Transconductance	1000	4000	µmho	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 kHz
9		g_{fs}	Common-Source Forward Transconductance	700	1600		$V_{DG} = 20$ V, $I_D = 200$ µA	
10		g_{os}	Common-Source Output Conductance		50		$V_{DS} = 20$ V, $V_{GS} = 0$	
11		g_{os}	Common-Source Output Conductance		4		$V_{DG} = 20$ V, $I_D = 200$ µA	
12		C_{iss}	Common-Source Input Capacitance		6	pF	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		2			
14		NF	Spot Noise Figure		0.5	dB		f = 100 Hz, $R_G = 10$ MΩ
15		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		20	$\frac{nV}{\sqrt{Hz}}$		f = 1 kHz

		Characteristic		2N5196		2N5197		2N5198		2N5199		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
16	M A T C H I N G	$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current		5		5		5		5	nA	$V_{DG} = 20$ V, $I_D = 200$ µA	125°C
17		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.95	1	–	$V_{DS} = 20$ V, $V_{GS} = 0$ V	
18		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.95	1	–	$V_{DG} = 20$ V, $I_D = 200$ µA	f = 1 kHz
19		$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		5		10		15	mV		
20		$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature (Note 2)		5		10		20		40	µV/°C		$T_A = 25°C$ $T_B = 125°C$
21					5		10		20		40			$T_A = -55°C$ $T_B = 25°C$
22		$\lvert g_{os1} - g_{os2} \rvert$	Differential Output Conductance		1		1		1		1	µmho		f = 1 kHz

*JEDEC registered data.

NQP

NOTES:

1. Assumes smaller value in numerator.
2. Measured at end points, T_A and T_B.

2N5432 2N5433 2N5434
PLASTIC EQUIVALENT J108 SERIES

Siliconix

n-channel JFETs *designed for . . .*

- **Low ON Resistance Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Capacitors**
- **Low Noise Audio Amplifiers**

Performance Curves NIP
See Section 4

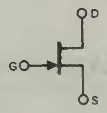
BENEFITS

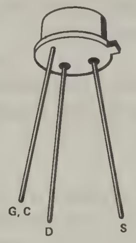
- Low Insertion Loss
  $r_{DS(on)} < 5\ \Omega$ (2N5432)
- Small Error in Measurement Systems
  $V_{DS(on)} < 50$ mV (2N5432)
- High Off-Isolation
  $I_{D(off)} < 200$ pA
- High Speed
  $t_{d(on)} < 4$ ns
- Low Noise Audio-Frequency Amplification
  $\overline{e}_n < 2\ \text{nV}/\sqrt{\text{Hz}}$ at 1 kHz Typical

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage	−25 V
Gate Current	100 mA
Drain Current	400 mA
Total Device Dissipation at 25°C Free-Air Temperature (Note 1)	300 mW
Storage Temperature Range	−65 to +150°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

TO-52
See Section 6





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

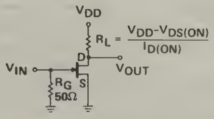
			Characteristic	2N5432		2N5433		2N5434		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		−200		−200		−200	pA	$V_{GS} = -15$ V, $V_{DS} = 0$	
2					−200		−200		−200	nA		150°C
3		BV_{GSS}	Gate Source Breakdown Voltage	−25		−25		−25		V	$I_G = -1\ \mu$A, $V_{DS} = 0$	
4		$I_{D(off)}$	Drain Cutoff Current		200		200		200	pA	$V_{DS} = 5$ V, $V_{GS} = -10$ V	
5					200		200		200	nA		150°C
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−4	−10	−3	−9	−1	−4	V	$V_{DS} = 5$ V, $I_D = 3$ nA	
7		I_{DSS}	Saturation Drain Current (Note 2)	150		100		30		mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
8		$r_{DS(on)}$	Static Drain-Source ON Resistance	2	5		7		10	ohm	$V_{GS} = 0$, $I_D = 10$ mA	
9		$V_{DS(on)}$	Drain-Source ON Voltage		50		70		100	mV		
10	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		5		7		10	ohm	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
11		C_{iss}	Common-Source Input Capacitance		30		30		30	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		15		15		15			
13	SW	$t_{d(on)}$	Turn-ON Delay Time		4		4		4	ns	$V_{DD} = 1.5$ V, $V_{GS(on)} = 0$, $V_{GS(off)} = -12$ V, $I_{D(on)} = 10$ mA	$R_L =$ 145 Ω (2N5432) 143 Ω (2N5433) 140 Ω (2N5434)
14		t_r	Rise Time		1		1		1			
15		$t_{d(off)}$	Turn-OFF Delay Time		6		6		6			
16		t_f	Fall Time		30		30		30			

*JEDEC registered data.

NIP

NOTES:

1. Derate linearly at the rate of 2.3 mW/°C.
2. Pulse test required pulsewidth 300 μs, duty cycle ⩽ 3%.



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 200 ns
PULSE RATE 550 pps

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.5 pF

Siliconix

matched dual n-channel JFETs *designed for . . .*

■ Low and Medium Frequency Differential Amplifiers

Performance Curves NQP
See Section 4

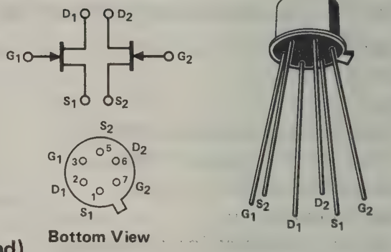
BENEFITS

- Minimum System Error and Calibration
  5 mV Offset Maximum (2N5452)
- Simplifies Amplifier Design
  Output Conductance Less that 1 µmho

*ABSOLUTE MAXIMUM RATINGS (25°C)

Any Lead-To-Case Voltage		±100 V
Gate-Drain or Gate-Source Voltage		-50 V
Gate-To-Gate Voltage		±100 V
Gate Current		50 mA
Total Device Dissipation 85°C Case Temperature	(Each Side)	250 mW
	(Both Sides)	500 mW
Power Derating	(Each Side)	2.86 mW/°C
	(Both Sides)	4.3 mW/°C
Storage Temperature Range		-65 to +250°C
Lead Temperature (1/16″ from case for 10 seconds)		300°C

TO-71
See Section 6



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5452		2N5453		2N5454		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1		I_{GSS}	Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -30 V, V_{DS} = 0 V	
2					-200		-200		-200	nA		T_A = 150°C
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	V_{DS} = 0 V, I_G = -1 µA	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-4.5	-1	-4.5	-1	-4.5		V_{DS} = 20 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.2	-4.2	-0.2	-4.2	-0.2	-4.2		V_{DS} = 20 V, I_D = 50 µA	
6		$V_{GS(f)}$	Gate-Source Forward Voltage		2		2		2		V_{DS} = 0 V, I_G = 1 mA	
7		I_{DSS}	Drain Saturation Current	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0 V	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	µmho	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
9				1000		1000		1000				f = 100 MHz
10		g_{os}	Common-Source Output Conductance		3.0		3.0		3.0			f = 1 kHz
11					1.0		1.0		1.0		V_{DS} = 20 V, I_D = 200 µA	
12		C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0	pF	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2			
14		C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		V_{DG} = 10 V, I_S = 0 V	
15		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
16		NF	Common-Source Spot Noise Figure		0.5		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = 0 V, R_G = 10 MΩ	f = 100 Hz
17	MATCHING	I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio (Note 1)	0.95	1.0	0.95	1.0	0.95	1.0	–	V_{DS} = 20 V, V_{GS} = 0 V	
18		$\|V_{GS1}-V_{GS2}\|$	Differential Gate-Source Voltage		5.0		10.0		15.0	mV	V_{DS} = 20 V, I_D = 200 µA	
19		$\Delta\|V_{GS1}-V_{GS2}\|$	Gate-Source Voltage Differential Change with Temperature		0.4		0.8		2.0			T = 25°C to -55°C
20					0.5		1.0		2.5			T = 25°C to +125°C
21		g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	0.97	1.0	0.97	1.0	0.95	1.0	–		f = 1 kHz
22		$\|g_{os1}-g_{os2}\|$	Differential Output Conductance		0.25		0.25		0.25	µmhos		

*JEDEC registered data

NOTE:
1. Assumes smaller value in numerator.

NQP

n-channel JFETs designed for . . .

2N5457 2N5458 2N5459

Siliconix

- **General Purpose Amplifiers**
- **Switches**

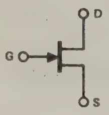
Performance Curves NRL, NPA
See Section 4

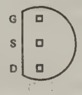
BENEFITS
- Low Cost
- Automated Insertion Package

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Voltage	25 V
Drain-Gate Voltage	25 V
Source-Gate Voltage	25 V
Total Device Dissipation at 25°C	310 mW
Derate above 25°C	2.82 mW/°C
Operating Junction Temperature	135°C
Storage Temperature Range	-65 to +150°C

TO-92
See Section 6





Bottom View

Plastic

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5457			2N5458			2N5459			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		−0.01	-1.0		−0.01	-1.0		−0.01	-1.0	nA	V_{GS} = -15 V, V_{DS} = 0	
2						-200			-200			-200			T_A = +100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25	-60		-25	-60		-25	-60		V	I_G = -10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5		-6.0	-1.0		-7.0	-2.0		-8.0		V_{DS} = 15 V, I_D = 10 nA	
5		I_{DSS}	Saturation Drain Current	1.0		5.0	2.0		9.0	4.0		16	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000		5,000	1,500		5,500	2,000		6,000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		10	50		15	50		20	50			
8		C_{iss}	Common-Source Input Capacitance		4.5	7.0		4.5	7.0		4.5	7.0	pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1.0	3.0		1.0	3.0		1.0	3.0			
10		NF	Noise Figure		0.04	3.0		0.04	3.0		0.04	3.0	dB	V_{DS} = 15 V, V_{GS} = 0 R_G = 1 MΩ, NBW =1 Hz	f = 1 kHz

*JEDEC registered data

NOTE:

1. Pulse test pulsewidth = 2 ms.

NRL, NPA

2N5484 2N5485 2N5486

n-channel JFETs *designed for . . .*

- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**
- **Analog Switches**

Siliconix

Performance Curves NH
See Section 4

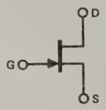
BENEFITS

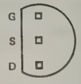
- Low Cost
- Completely Specified for 400 MHz Operation
- Low Error Analog Switch
  Very Little Charge Coupling
  $C_{rss} < 1.0$ pF

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	25 V
Source Gate Voltage	25 V
Drain Current	30 mA
Forward Gate Current	10 mA
Total Device Dissipation @ 25°C	360 mW
Derate above 25°C	3.27 mW/°C
Operating Junction Temperature Range	–65 to +135°C
Storage Temperature Range	–65 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	240°C

TO-92
See Section 6





Bottom View

Plastic

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	2N5484		2N5485		2N5486		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-1.0		-1.0		-1.0	nA	V_{GS} = -20 V, V_{DS} = 0	
2					-200		-200		-200			T_A = +100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		-25		-25		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.3	-3.0	-0.5	-4.0	-2.0	-6.0		V_{DS} = 15 V, I_D = 10 nA	
5		I_{DSS}	Saturation Drain Current	1.0	5.0	4.0	10	8.0	20	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	3,000	6,000	3,500	7,000	4,000	8,000	μmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		50		60		75			
8		$Re(y_{fs})$	Common-Source Forward Transconductance	2,500								f = 100 MHz
9						3,000		3,500				f = 400 MHz
10		$Re(y_{os})$	Common-Source Output Conductance		75							f = 100 MHz
11							100		100			f =400 MHz
12		$Re(y_{is})$	Common-Source Input Conductance		100							f = 100 MHz
13							1,000		1,000			f = 400 MHz
14		C_{iss}	Common-Source Input Capacitance		5.0		5.0		5.0	pF		f = 1 MHz
15		C_{rss}	Common-Source Reverse Transfer Capacitance		1.0		1.0		1.0			
16		C_{oss}	Common-Source Output Capacitance		2.0		2.0		2.0			
17		NF	Noise Figure		2.5		2.5		2.5	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1 MΩ	f = 1 kHz
18					3.0						V_{DS} = 15 V, I_D = 1 mA, R_G = 1 kΩ	f = 100 MHz
19							2.0		2.0		V_{DS} = 15 V, I_D = 4 mA, R_G = 1 kΩ	
20							4.0		4.0			f = 400 MHz
21		G_{ps}	Common-Source Power Gain	16	25						V_{DS} = 15 V, I_D = 1 mA	f – 100 MHz
22						18	30	18	30		V_{DS} = 15 V, I_D = 4 mA	
23						10	20	10	20			f = 400 MHz

* JEDEC registered data

NH

NOTE:

1 Pulse Test PW 300 μs, duty cycle ⩽3%

Siliconix

matched dual n-channel JFETs designed for . . .

■ Differential Amplifiers

Performance Curves NQP
See Section 4

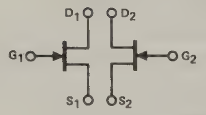
BENEFITS

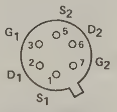
- Ultra-Low Noise
  $\overline{e}_n$ = 8 nV/$\sqrt{\text{Hz}}$ at 10 Hz (Typical)
  $\overline{e}_n$ = 2 nV/$\sqrt{\text{Hz}}$ at 1 kHz (Typical)
- Minimum System Error and Calibration
  5 mV Offset Maximum
  CMRR > 100 dB

ABSOLUTE MAXIMUM RATINGS (25°C)

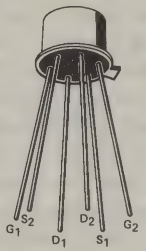
Gate-Drain or Gate-Souce Voltage .... -40 V
Gate Current .... 50 mA
Device Dissipation (Each Side), T_A = 85°C
(Derate 2.0 mW/°C ....250 mW
Total Device Dissipation T_A = 85°C
(Derate 3.0 mW/°C) ....375 mW
Storage Temperature Range .... -65°C to +200°C
Lead Temperature
(1/16" from case for 30 seconds) ....300°C

TO-71
* See Section 6





Bottom View



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-250	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-250	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-4		V_{DS} = 20 V, I_D = 1 nA	
5		V_{GS}	Gate Source Voltage	-0.2	-3.8		V_{DG} = 20 V, I_D = 200 μA	
6		I_G	Gate Operating Current		-100	pA		
					-100	nA		125°C
7		I_{DSS}	Saturation Drain Current (Note 1)	0.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	4000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
9		g_{fs}	Common-Source Forward Transconductance (Note 1)	500	1000		V_{DG} = 20 V, I_D = 200 μA	
10		g_{os}	Common-Source Output Conductance		10		V_{DS} = 20 V, V_{GS} = 0	
11		g_{os}	Common-Source Output Conductance		1		V_{DG} = 20 V, I_D = 200 μA	
12		C_{iss}	Common-Source Input Capacitance		25	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		5			
14		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage 2N5515-19		30	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$	V_{DG} = 20 V, I_D = 200 μA	f = 10 Hz
			2N5520-24		15			
			2N5515-24		10			f = 1 kHz

		Characteristic		2N5515,20		2N5516,21		2N5517,22		2N5518,23		2N5519,24		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
15	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		10		10		10		10		10	nA	V_{DG} = 20 V, I_D = 200 μA	125°C
16		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	0.95	1	0.95	1	0.90	1	–	V_{DS} = 20 V, V_{GS} = 0	
17		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15		15	mV	V_{DG} = 20 V, I_D = 200 μA	
18		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)		5		10		20		40		80	μV/°C		T_A = 25°C T_B = 125°C
					5		10		20		40		80			T_A = -55°C T_B = 25°C
19		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.1		0.1		0.1		0.1		0.1	μmho		f = 1 kHz
20		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1 and 2)	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	–		
21		CMRR	Common Mode Rejection Ratio (Note 4)	100		100		90						dB	V_{DD} = 10 to 20 V, I_D = 200 μA	

*JEDEC registered data.

NOTES:

1. Pulse test required, pulsewidth = 300 μs, duty cycle ⩽ 3%.
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.
4. CMRR = $20\log_{10}\left(\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right)$, ΔV_{DD} = 10 V.

NQP

Siliconix

monolithic dual n-channel JFETs *designed for . . .*

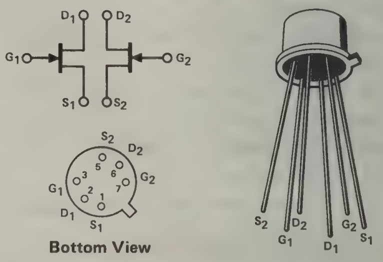
■ General Purpose Differential Amplifiers

Performance Curves NQP
See Section 4

BENEFITS

- High Input Impedance
  $I_G < 50$ pA
- Minimum System Error and Calibration
  5 mV Offset Maximum (2N5545)

TO-71
See Section 6



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . –50 V
Gate Current . . . . 30 mA
Device Dissipation (Each Side), T_A = 25°C
  (Derate 1.67 mW/°C) . . . . 250 mW
Total Device Dissipation, T_A = 25°C
  (Derate 2.67 mW/°C) . . . . 400 mW
Storage Temperature Range . . . . –65 to +200°C
Lead Temperature
  (1/16″ from case for 30 seconds) . . . . 300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions		
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -30 V, V_{DS} = 0		
2					-150	nA			T_A = 150°
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = –1 µA, V_{DS} = 0		
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-4.5		V_{DS} = 15 V, I_D = 0.5 nA		
5		I_G	Gate Operating Current		-50	pA	V_{DG} = 15 V, I_D = 200 µA		
6		I_{DSS}	Saturation Drain Current	0.5	8	mA	V_{DS} = 15 V, V_{GS} = 0		
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1500	6000	µmho	V_{DS} = 15 V, V_{GS} = 0		f = 1 kHz
8		g_{os}	Common-Source Output Conductance		25				
9		C_{iss}	Common-Source Input Capacitance		6	pF			f = 1 MHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance		2				
11		NF	Spot Noise Figure		3.5	dB	V_{DG} = 15 V, I_D = 200 µA	2N5545	f = 10 Hz, R_G = 1 MΩ
					5			2N5546	
12		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		180	$\frac{nV}{\sqrt{Hz}}$		2N5545	f = 10 Hz
					200			2N5546	

		Characteristic		2N5545		2N5546		2N5547		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
13	MATCHING	$\|I_{G1}-I_{G2}\|$	Differential Gate Current		5		5		5	nA	V_{DG} = 15 V, I_D = 200 µA	T_A = 125°C
14		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.90	1	0.90	1	–	V_{DS} = 15 V, V_{GS} = 0	
15		$\|V_{GS1}-V_{GS2}\|$	Differential Gate-Source Voltage		5		10		15	mV	V_{DG} = 15 V	I_D = 50 µA
					5		10		15			I_D = 200 µA
16		$\frac{\Delta\|V_{GS1}-V_{GS2}\|}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 2)		10		20		40	µV/°C	V_{DG} = 15 V, I_D = 200 µA	T_A = 25°C T_B = 125°C
					10		20		40			T_A = -55°C T_B = 25°C
17		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 1)	0.97	1	0.95	1	0.90	1	–		f = 1 kHz
18		$\|g_{os1}-g_{os2}\|$	Differential Output Conductance		1		2		3	µmho		

*JEDEC registered data.

NOTES:

1. Assumes smaller value in numerator.
2. Measured at end points, T_A and T_B.

NQP

Siliconix

matched dual n-channel JFETs designed for . . .

Performance Curves NCA
See Section 4

- **Wideband Differential Amplifiers**
- **Commutators**

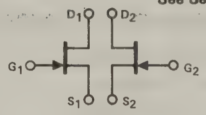
BENEFITS

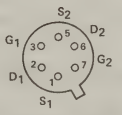
- High Gain
  7500 µmho Minimum g_{fs}
- Specified Matching Characteristics

*ABSOLUTE MAXIMUM RATINGS (25°C)

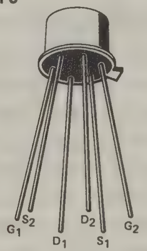
Gate–Gate Voltage . . . . ±80 V
Gate-Drain or Gate-Source Voltage . . . . -40 V
Gate Current . . . . 50 mA
Device Dissipation (Each Side), T_A = 25°C
(Derate 2.2 mW/°C) . . . . 325 mW
Total Device Dissipation, T_A = 25°C
(Derate 3.3 mW/°C) . . . . 650 mW
Storage Temperature Range . . . . -65 to +200°C
Lead Temperature
(1/16″ from case for 10 seconds) . . . . .300°C

TO-71
See Section 6





Bottom View



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate-Reverse Current		-100	pA	V_{GS} = -20 V, V_{DS} = 0	
2					-200	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		V	I_G = -1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-3		V_{DS} = 15 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Voltage		1.0		V_{DS} = 0 V, I_G = 2 mA	
6		I_{DSS}	Saturation Drain Current (Note 1)	5	30	mA	V_{DS} = 15 V, V_{GS} = 0	
7		$r_{DS(on)}$	Static Drain Source ON Resistance		100	Ω	I_D = 1 mA, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	7500	12,500	µmho	V_{DG} = 15 V, I_D = 2 mA	f = 1 kHz
				7000				f = 100 MHz
9		g_{os}	Common-Source Output Conductance		45			f = 1 kHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance		3	pF		f = 1 MHz
11		C_{iss}	Common-Source Input Capacitance		12			
12		NF	Spot Noise Figure		1.0	dB		f = 10 Hz, R_g = 1M
13		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		50	$\frac{nV}{\sqrt{Hz}}$		f = 10 Hz

		Characteristics		2N5564		2N5565		2N5566		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
14	MATCHING	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	0.95	1	–	V_{DS} = 15 V, V_{GS} = 0	
15		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		10		20	mV	V_{DS} = 15 V, I_D = 2 mA	
16		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)		10		25		50	µV/°C		T_A = 25°C T_B = 125°C
					10		25		50			T_A = -55°C T_B = 25°C
17		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1 and 2)	0.95	1	0.90	1	0.90	1	–		f = 1 kHz

*JEDEC registered data.

NCA

NOTES:
1. Pulse test required, pulse width 300 µs, duty cycle ⩽ 3%.
2. Assumes smaller value in numerator.
3. Measured at ends points, T_A and T_B.

Siliconix

n-channel JFETs designed for . . .

- **Analog Switches**
- **Commutators**
- **Choppers**

Performance Curves NCA
See Section 4

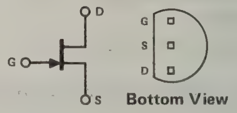
BENEFITS

- Low Cost
- Industry Standard Package
- Automatic Insertion Package
- Fast Switching
  $t_{rise} < 5$ ns (2N5638)
- Low Insertion Loss
  $r_{DS(on)} < 30\ \Omega$ (2N5638)
- Short Sample and Hold Aperture Time
  $C_{rss} < 4$ pF

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Breakdown Voltage	30 V
Drain-Gate Breakdown Voltage	30 V
Source-Gate Breakdown Voltage	30 V
Forward Gate Current	10 mA
Total Device Dissipation at T_{LEAD} = 25°C	625 mW
Derate above 25°C	5.68 mW/°C
Operating Junction Temperature Range	-65 to +135°C
Storage Temperature Range	-65 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-92
See Section 6



Bottom View

Plastic

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

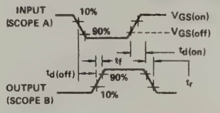
		Characteristic		2N5638		2N5639		2N5640		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	$I_G = -10\ \mu A$, $V_{DS} = 0$	
2	STATIC	I_{GSS}	Gate Reverse Current		-1.0		-1.0		-1.0	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	
3					-1.0		-1.0		-1.0	μA		$T_A = +100°C$
4		$I_{D(off)}$	Drain Cutoff Current		1.0		1.0		1.0	nA	$V_{DS} = 15$ V, $V_{GS} = -12$ V (2N5638) $V_{GS} = -8$ V (2N5639), $V_{GS} = -6$ V (2N5640)	
5					1.0		1.0		1.0	μA		$T_A = +100°C$
6		I_{DSS}	Saturation Drain Current	50		25		5.0		mA	$V_{DS} = 20$ V, $V_{GS} = 0$ (Note 1)	
7		$V_{DS(on)}$	Drain-Source ON Voltage		0.5		0.5		0.5	V	$V_{GS} = 0$, $I_D = 12$ mA (2N5638), $I_D = 6$ mA (2N5639), $I_D = 3$ mA (2N5640)	
8		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	$I_D = 1$ mA, $V_{GS} = 0$	
9	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100		$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
10		C_{iss}	Common-Source Input Capacitance		10		10		10	pF	$V_{GS} = -12$ V, $V_{DS} = 0$	f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		4.0		4.0		4.0			
12	SW	$t_{d(on)}$	Turn-On Delay Time		4.0		6.0		8.0	nsec	$V_{DD} = 10$ V $I_{D(on)} = 12$ mA (2N5638) $R_L = 800\ \Omega$ (2N5638) $V_{GS(on)} = 0$ $I_{D(on)} = 6$ mA (2N5639) $R_L = 1.6k\ \Omega$ (2N5639) $V_{GS(off)} = -10$ V $I_{D(on)} = 3$ mA (2N5640) $R_L = 3.2k\ \Omega$ (2N5640)	
13		t_r	Rise Time		5.0		8.0		10			
14		$t_{d(off)}$	Turn-OFF Delay Time		5.0		10		15			
15		t_f	Fall Time		10		20		30			

* JEDEC registered data

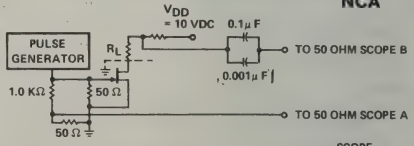
NOTE:

1 Pulse test PW ⩽ 300 μsec, duty cycle ⩽ 3.0%

$$R_L = \frac{V_{DD}}{I_D} - (r_{DS(on)} + 50)$$



NCA



SCOPE
TEKTRONIX 567A
OR EQUIVALENT

matched dual n-channel JFETs designed for . . .

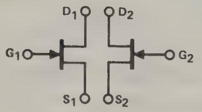
- **Differential Amplifiers**
- **High Input Impedance Amplifiers**

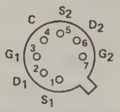
Performance Curves NT
See Section 4

BENEFITS

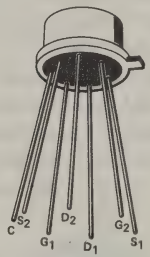
- Matching Characteristics Specified
- High Input Impedance
  I_G = 1 pA Max (2N5906–9)

TO-78
See Section 6





Bottom View



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-to-Gate Voltage	±80 V
Gate-Drain or Gate-Source Voltage	–40 V
Gate Current	10 mA
Device Dissipation (Each Side), T_A = 25°C (Derate 3 mW/°C)	367 mW
Total Device Dissipation, T_A = 25°C (Derate 4 mW/°C)	500 mW
Storage Temperature Range	–65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5902-5		2N5906-9		Unit	Test Conditions	
				Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-5		-2	pA	V_{GS} = -20 V, V_{DS} = 0	
2					-10		-5	nA		125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		V	I_G = -1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.6	-4.5	-0.6	-4.5		V_{DS} = 10 V, I_D = 1 nA	
5		V_{GS}	Gate Source Voltage		-4		-4		V_{DG} = 10 V, I_D = 30 µA	
6		I_G	Gate Operating Current		-3		-1	pA		
7					-3		-1	nA		125°C
8	DYNAMIC	I_{DSS}	Saturation Drain Current	30	500	30	500	µA	V_{DS} = 10 V, V_{GS} = 0	
9		g_{fs}	Common-Source Forward Transconductance	70	250	70	250	µmho		f = 1 kHz
10		g_{os}	Common-Source Output Conductance		5		5			
11		C_{iss}	Common-Source Input Capacitance		3		3	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5			
13		g_{fs}	Common-Source Forward Transconductance	50	150	50	150	µmho	V_{DG} = 10 V, I_D = 30 µA	f = 1 kHz
14		g_{os}	Common-Source Output Conductance		1		1			
15		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		0.2		0.1	$\frac{\mu V}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	
16		NF	Spot Noise Figure		3		1	dB		f = 100 Hz, R_G = 10 M

		Characteristic		2N5902, 6		2N5903, 7		2N5904, 8		2N5905, 9		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
17	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		2.0		2.0		2.0		2.0	nA	V_{DG} = 10 V, I_D = 30 µA, T_A = 125°C	2N5902-5
18					0.2		0.2		0.2		0.2			2N5906-9
19		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.95	1	–	V_{DS} = 10 V, V_{GS} = 0	
20		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.95	1	–	V_{DG} = 10 V, I_D = 30 µA	f = 1 kHz
21		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15	mV		
22		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 2)		5		10		20		40	µV/°C		T_A = 25°C T_B = 125°C
23					5		10		20		40			T_A = -55°C T_B = 25°C
24		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.2		0.2		0.2		0.2	µmho		f = 1 kHz

*JEDEC registered data.

NOTES:

1. Assumes smaller value in numerator.
2. Measured at end points, T_A and T_B.

NT

matched dual n-channel JFETs *designed for . . .*

■ Wideband Differential Amplifiers

Siliconix

Performance Curves NZF-D, NNZ See Section 4

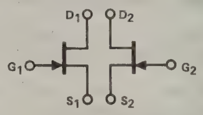
BENEFITS

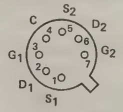
- High Gain through 100 MHz $g_{fs} > 5000\ \mu mho$
- Matching Characteristics Specified

ABSOLUTE MAXIMUM RATINGS (25°C)

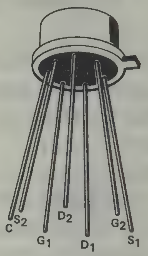
Gate-to-Gate Voltage	±80 V
Gate-Drain or Gate-Source Voltage	–25 V
Gate Current	50 mA
Device Dissipation (Each Side), (Derate 3 mW/°C)	367 mW
Total Device Dissipation, (Derate 4 mW/°C)	500 mW
Storage Temperature Range	–65 to +200°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

TO-78
See Section 6





Bottom View



*ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)

			Characteristic	Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -15 V, V_{DS} = 0	
2					-250	nA		T_A = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-5		V_{DS} = 10 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.3	-4		V_{DG} = 10 V, I_D = 5 mA	
6		I_G	Gate Operating Current		-100	pA		
					-100	nA		T_A = 125°C
7		I_{DSS}	Saturation Drain Current (Note 1)	7	40	mA	V_{DS} = 10 V, V_{GS} = 0 V	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	5000	10,000	µmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
9		g_{fs}	Common-Source Forward Transconductance	5000	10,000			f = 100 MHz
10		g_{os}	Common-Source Output Conductance		100			f = 1 kHz
11		g_{os}	Common-Source Output Conductance		150			f = 100 MHz
12		C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
14		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
15		NF	Spot Noise Figure		1	dB		f = 10 kHz R_G = 100K

			Characteristic	2N5911		2N5912		Unit	Test Conditions	
				Min	Max	Min	Max			
16	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		20		20	nA	V_{DG} = 10 V, I_D = 5 mA	T_A = 125°C
17		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	–	V_{DS} = 10 V, V_{GS} = 0	
18		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		10		15	mV	V_{DG} = 10 V, I_D = 5 mA	
19		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)		20		40	µV/°C		T_A = 25°C T_B = 125°C
20					20		40			T_A = -55°C T_B = 25°C
21		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 2)	0.95	1	0.95	1	–		f = 1 kHz

*JEDEC registered data.

NOTES:
1. Pulsewidth ⩽ 300 µs, duty cycle ⩽ 3%.
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.

NZF-D, NNZ

Siliconix

enhancement-type p-channel MOSFETs designed for . . .

Performance Curves MRA
See Section 4

- **Ultra-High Input Impedance Amplifiers**
  - **Electrometers**
  - **Smoke Detectors**
  - **pH Meters**
- **Digital Switching Interfaces**
- **Analog Switching**

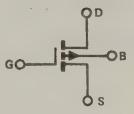
BENEFITS

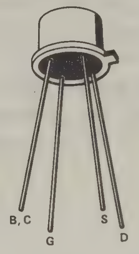
- Rugged MOS Gate Minimizes Handling Problems
  ±125 V Transient Capability
- Low Gate-Leakage
  Typically 0.02 pA
- High Off-Isolation as a Switch
  $I_{DSS} < 200$ pA

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source or Gate-Source Voltage 3N163	-40 V
Drain-Source or Gate-Source Voltage 3N164	-30 V
Transient Gate-Source Voltage (Note 1)	±125 V
Drain Current	-50 mA
Storage Temperature	-65 to +200°C
Operating Junction Temperature	-55 to +150°C
Total Device Dissipation (Derate 3.0 mW/°C to 150°C)	375 mW
Lead Temperature 1/16" From Case For 10 Seconds . .	265°C

TO-72
See Section 6





*ELECTRICAL CHARACTERISTICS (25°C and $V_{BS} = 0$ unless otherwise noted)

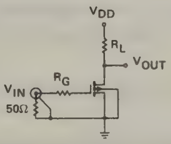
		Characteristic		3N163 Min	3N163 Max	3N164 Min	3N164 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate-Body Leakage Current		-10			pA	$V_{GS} = -40$ V, $V_{DS} = 0$	
2					-25					$T_A = 125°C$
3							-10		$V_{GS} = -30$ V, $V_{DS} = 0$	
4							-25			$T_A = 125°C$
5		BV_{DSS}	Drain-Source Breakdown Voltage	-40		-30		V	$I_D = -10\ \mu A$, $V_{GS} = 0$	
6		BV_{SDS}	Source-Drain Breakdown Voltage	-40		-30			$I_S = -10\ \mu A$, $V_{GD} = V_{BD} = 0$	
7		V_{GS}	Gate Source Voltage	-3	-6.5	-2.5	-6.5		$V_{DS} = -15$ V, $I_D = -0.5$ mA	
8		$V_{GS(th)}$	Gate-Source Threshold Voltage	-2	-5	-2	-5		$V_{DS} = V_{GS}$, $I_D = -10\ \mu A$	
9		I_{DSS}	Drain Cutoff Current		-200		-400	pA	$V_{DS} = -15$ V, $V_{GS} = 0$	
10		I_{SDS}	Source Cutoff Current		-400		-800		$V_{SD} = -20$ V, $V_{GD} = 0$, $V_{DB} = 0$	
11		$I_{D(on)}$	ON Drain Current	-5	-30	-3	-30	mA	$V_{DS} = -15$ V, $V_{GS} = -10$ V	
12		$r_{DS(on)}$	Drain-Source ON Resistance		250		300	Ω	$V_{GS} = -20$ V, $I_D = -100\ \mu A$	
13	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2,000	4,000	1,000	4,000	μmho	$V_{DS} = -15$ V, $I_D = -10$ mA	f = 1 kHz
14		g_{os}	Common-Source Output Conductance		250		250			
15		C_{iss}	Common-Source Input Capacitance		2.5		2.5	pF	$V_{DS} = -15$ V, $I_D = -10$ mA	f = 1 MHz
16		C_{rss}	Common-Source Reverse Transfer Capacitance		0.7		0.7			
17		C_{oss}	Common-Source Output Capacitance		3		3			
18	SW	$t_{d(on)}$	Turn-ON Delay Time		12		12	ns	$V_{DD} = -15$ V $I_{D(on)} = -10$ mA $R_G = R_L = 1.5\ k\Omega$	
19		t_r	Rise Time		24		24			
20		t_{off}	Turn-OFF Time		50		50			

*JEDEC registered data

MRA

NOTE:

1. Transient gate-source voltage JEDEC registered as ±125 V.



INPUT PULSE	SAMPLING SCOPE
RISE TIME ≤ 2 ns	$t_r \leq 0.2$ ns
PULSE WIDTH ≥ 200 ns	$C_{IN} \leq 2$ pF
	$R_{IN} \geq 10$ MΩ

n-channel JFETs *designed for . . .*

- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

Siliconix

Performance Curves NH
See Section 4

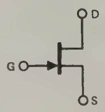
BENEFITS

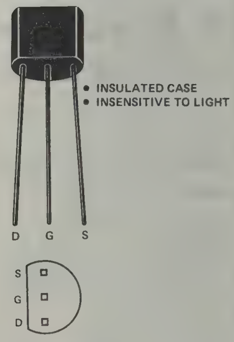
- Wide Band
  High y_{fs}/C_{iss} Ratio
- Low Feedback Capacitance
  $C_{rss} = 0.85$ pF Typical
- Selected I_{DSS} and V_{GS} Ranges

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	30 V
Drain-Source Voltage	30 V
Reverse Gate-Source Voltage	30 V
Forward Gate Current	10 mA
Continuous Device Dissipation at (or Below) 25°C Free Air Temperature (Note 1)	200 mW
Storage Temperature Range	−55°C to +150°C
Lead Temperature (1/16″ from case for 10 seconds)	260°C

TO-92
See Section 6





Bottom View

ELECTRICAL CHARACTERISTICS (25°C)

		Characteristic			Min	Typ	Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage		−30			V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current				−5	nA	$V_{GS} = -20$ V, $V_{DS} = 0$	
3		I_{DSS}	Saturation Drain Current		2		25	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
4		I_{DSS}	Selected into Following Groups (Note 2)	BF244A	2.0		6.5	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
5				BF244B	6.0		15	mA		
6				BF244C	12		25	mA		
7		V_{GS}	Corresponding to I_{DSS} groups	BF244A	−0.4		−2.2	V	$V_{DS} = 15$ V, $I_D = 200\ \mu A$	
8				BF244B	−1.6		−3.8	V		
9				BF244C	−3.2		−7.5	V		
10		$V_{GS(off)}$	Gate-Source Cutoff Voltage		−0.5		−8	V	$V_{DS} = 15$ V, $I_D = 10\ \mu A$	
11	DYNAMIC	g_{fs}	Small-Signal Common-Source Forward Transconductance		3	5.5	6.5	mmho	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1 kHz	
12		C_{rss}	Common-Source Reverse Transfer Capacitance			0.85		pF	$V_{DS} = 20$ V, $V_{GS} = -1$ V	
13		$\frac{1}{g_{is}}$	Input Resistance			25		kΩ	$V_{DS} = 20$ V, $V_{GS} = -1$ V	f = 100 MHz
14						10		kΩ		f = 200 MHz
15		C_{iss}	Common-Source Input Capacitance			4		pF	$V_{DS} = 20$ V, $V_{GS} = -1$ V	
16		C_{oss}	Common-Source Output Capacitance			1.6		pF	$V_{DS} = 20$ V, $V_{GS} = -1$ V	

NOTE:

1. Derate linearly to 125°C free-air temperature at the rate of 2.5 mW/°C.
2. Pulse test PW ⩽ 300 μs, duty cycle ⩽ 3%.

NH

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NH

- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

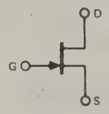
BENEFITS

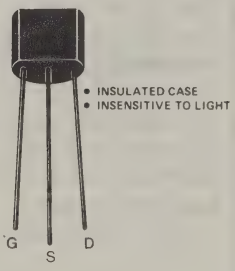
- Wide Band
  High y_{fs}/C_{iss} Ratio
- Low Feedback Capacitance
  C_{rss} = 0.85 pF Typical
- Selected I_{DSS} and V_{GS} Ranges

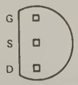
ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	30 V
Drain-Source Voltage	30 V
Reverse Gate-Source Voltage	30 V
Forward Gate Current	10 mA
Continuous Device Dissipation at (or Below) 25°C Free Air Temperature (Note 1)	200 mW
Storage Temperature Range	−55°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	260°C

TO-92
See Section 6







Bottom View

ELECTRICAL CHARACTERISTICS (25°C)

		Characteristic			Min	Typ	Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage		−30			V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current				−5	nA	$V_{GS} = -20$ V, $V_{DS} = 0$	
3		I_{DSS}	Saturation Drain Current		2		25	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
4		I_{DSS}	Selected into Following Groups (Note 2)	BF245A	2.0		6.5	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
5				BF245B	6.0		15	mA		
6				BF245C	12		25	mA		
7		V_{GS}	Corresponding to I_{DSS} groups	BF245A	−0.4		−2.2	V	$V_{DS} = 15$ V, $I_D = 200\ \mu A$	
8				BF245B	−1.6		−3.8	V		
9				BF245C	−3.2		−7.5	V		
10		$V_{GS(off)}$	Gate-Source Cutoff Voltage		−0.5		−8	V	$V_{DS} = 15$ V, $I_D = 10\ \mu A$	
11	DYNAMIC	g_{fs}	Small-Signal Common-Source Forward Transconductance		3	5.5	6.5	mmho	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1 kHz	
12		C_{rss}	Common-Source Reverse Transfer Capacitance			0.85		pF	$V_{DS} = 20$ V, $V_{GS} = -1$ V	
13		$\frac{1}{g_{is}}$	Input Resistance			25		kΩ	$V_{DS} = 20$ V, $V_{GS} = -1$ V	f = 100 MHz
14						10		kΩ		f = 200 MHz
15		C_{iss}	Common-Source Input Capacitance			4		pF	$V_{DS} = 20$ V, $V_{GS} = -1$ V	
16		C_{oss}	Common-Source Output Capacitance			1.6		pF	$V_{DS} = 20$ V, $V_{GS} = -1$ V	

NOTE:

NH

1. Derate linearly to 125°C free-air temperature at the rate of 2.5 mW/°C.
2. Pulse test PW ≤ 300 μs, duty cycle ≤ 3%.

n-channel JFETs *designed for . . .*

Siliconix

- **UHF Amplifiers**
- **Mixers**
- **Oscillators**

Performance Curves NH

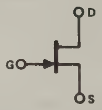
BENEFITS

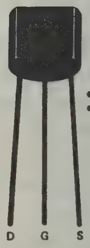
- High Gain
  G_{pg} = 14 dB Typical at 800 MHz
- Selected I_{DSS} Ranges

ABSOLUTE MAXIMUM RATINGS

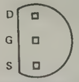
Drain-Gate Voltage . . . . .30 V
Drain-Source Voltage . . . . .30 V
Reverse Gate-Source Voltage. .30 V
Forward Gate Current. . . . . 50 mA
Total Device Dissipation @ 25°C. . . . . 350 mW
Derate above 25°C . . . . .3.5 mW/°C
Storage Temperature Range . . . . −65 to +150°C
Lead Temperature
(1/16″ from case for 10 seconds) . . . . .260°C

TO-92
See Section 6





- INSULATED CASE
- INSENSITIVE TO LIGHT



Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	BV_{DGO}	Drain-Gate Breakdown Voltage	−30			V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2		I_{GSS}	Gate-Reverse Current			−5	nA	$V_{GS} = -20$ V, $V_{DS} = 0$	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5		−7.5	V	$V_{DS} = 15$ V, $I_D = 10$ nA	
4		I_{DSS}	Drain Current at Zero Gate Voltage (Note 1)	3	12	18	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
5		I_{DSS}	Selected into Following Groups (Note 1) BF256LA	3		7	mA		
6			BF256LB	6		13	mA		
7			BF256LC	11		18	mA		
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	4.5	5.5		mmho		f = 1 kHz
9		g_{os}	Common-Source Output Conductance		50		μmho		
10		C_{iss}	Common-Source Input Capacitance			4.5	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance			1.2	pF		
12		$f(y_{fs})$	Cutoff Frequency (Note 2)		1000		MHz		
13		G_{pg}	Common-Gate Neutralized Insertion Power Gain		14		dB	$V_{DS} = 10$ V, $R_S = 47\ \Omega$, f = 800 MHz	
14		NF	Noise Figure		7.5		dB	$V_{DS} = 15$ V, $R_S = 47\ \Omega$, f = 800 MHz	

NH

NOTES:

1. Pulse test PW ≤ 300 μs, duty cycle ≤ 2%.
2. Frequency at which the real part of the forward transconductance falls 3 dB relative to the value at 1 kHz.

current regulator diodes designed for . . .

Siliconix

Performance Curves
NKL NKM NKO See Section 4

- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Low Voltage References**

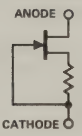
BENEFITS

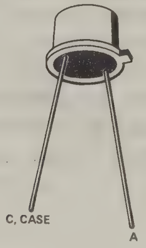
- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes
  Temperature Coefficient Better Than 1500 ppm/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources
  No Power Supplies Required

ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage	100 V
Forward Current	20 mA
Reverse Current	50 mA
Thermal Resistance θ_{JC}	100°C/W
Power Dissipation at T_C = 25°C	1.25 W
Operating Junction Temperature	−55 to +150°C
Storage Temperature	−55° to +200°C

TO-18 (MODIFIED)
See Section 6





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Symbol	I_{F1}			Z_d		Z_k		V_L		POV	θ_1			GEOM
Parameter	Regulator Current			Dynamic Impedance		Knee Impedance		Limiting Voltage		Peak Operating Voltage	Temperature Coefficient			
Test Conditions	V_F = 25 V (Note 1)			V_F = 25 V (Note 2)		V_F = 6 V		$I_F = 0.8\ I_{F1(Min)}$ (Note 3)		$I_F = 1.1\ I_{F1(Max)}$ (Note 4)	V_F = 25 V −55°C ≤ T_A ≤ 25°C	V_F = 25 V 0°C ≤ T_A ≤ 50°C	V_F = 25 V 25°C ≤ T_A ≤ 125°C	
Units	(mA)			MΩ		MΩ		Volts		Min Volts	Typ ppm/°C	Typ ppm/°C	Typ ppm/°C	
	Nom	Min	Max	Min	Typ	Min	Typ	Max	Typ					
CR022	0.22	0.198	0.242	8.0	16.0	2.3	3.5	1.0	0.40	100	+1350	+1050	+750	NKL
CR024	0.24	0.216	0.264	7.0	14.0	2.0	3.0	1.0	0.45	100	+1200	+900	+600	
CR027	0.27	0.243	0.297	6.0	13.0	1.7	2.8	1.0	0.50	100	+1000	+700	+400	
CR030	0.30	0.270	0.330	5.0	12.0	1.3	2.5	1.0	0.55	100	+800	+500	+200	
CR033	0.33	0.297	0.363	4.0	11.0	1.0	2.2	1.0	0.60	100	+600	+300	−50	
CR039	0.39	0.351	0.429	3.0	9.5	0.8	1.90	1.05	0.70	100	+300	+50	−300	
CR043	0.43	0.387	0.473	2.5	8.6	0.7	1.65	1.05	0.78	100	+150	−150	−450	
CR047	0.47	0.423	0.517	2.0	8.0	0.6	1.50	1.10	0.85	100	−50	−300	−600	
CR056	0.56	0.504	0.616	1.5	6.5	0.5	1.25	1.20	0.98	100	−300	−600	−900	
CR062	0.62	0.558	0.682	1.2	6.2	0.4	1.15	1.30	1.10	100	−500	−800	−1100	
CR068	0.68	0.612	0.748	1.2	8.5	0.400	1.70	1.15	0.70	100	+850	+400	−50	NKM
CR075	0.75	0.675	0.825	1.15	7.2	0.335	1.50	1.20	0.75	100	+650	+200	−250	
CR082	0.82	0.738	0.902	1.00	6.0	0.290	1.30	1.25	0.80	100	+450	+50	−450	
CR091	0.91	0.819	1.001	0.88	5.2	0.240	1.10	1.29	0.85	100	+300	−150	−600	
CR100	1.00	0.900	1.100	0.80	4.4	0.205	0.95	1.35	0.95	100	+150	−300	−750	
CR110	1.10	0.990	1.210	0.70	3.8	0.180	0.80	1.40	1.05	100	+50	−450	−900	
CR120	1.20	1.08	1.32	0.64	3.3	0.155	0.71	1.45	1.15	100	−150	−600	−1050	
CR130	1.30	1.17	1.43	0.58	3.2	0.135	0.60	1.50	1.25	100	−300	−750	−1200	
CR140	1.40	1.26	1.54	0.54	2.5	0.115	0.52	1.55	1.30	100	−400	−850	−1300	
CR150	1.50	1.35	1.65	0.51	2.2	0.105	0.46	1.60	1.35	100	−500	−950	−1400	
CR160	1.60	1.44	1.76	0.475	1.00	0.092	0.35	1.65	0.50	100	+650	+350	+50	NKO
CR180	1.80	1.62	1.98	0.420	0.95	0.074	0.30	1.75	0.55	100	+500	+200	−100	
CR200	2.00	1.80	2.20	0.395	0.88	0.061	0.25	1.85	0.60	100	+350	+50	−250	
CR220	2.20	1.98	2.42	0.370	0.80	0.052	0.22	1.95	0.65	100	+200	−100	−350	
CR240	2.40	2.16	2.64	0.345	0.75	0.044	0.20	2.00	0.70	100	+50	−200	−450	
CR270	2.70	2.43	2.97	0.320	0.68	0.035	0.18	2.15	0.75	100	−100	−300	−550	
CR300	3.00	2.70	3.30	0.300	0.60	0.029	0.14	2.25	0.85	100	−250	−450	−700	
CR330	3.30	2.97	3.63	0.280	0.56	0.024	0.13	2.35	0.90	100	−400	−600	−800	
CR360	3.60	3.24	3.96	0.265	0.52	0.020	0.11	2.50	0.95	100	−550	−750	−900	
CR390	3.90	3.51	4.29	0.255	0.48	0.017	0.10	2.60	1.00	100	−700	−850	−1000	
CR430	4.30	3.87	4.73	0.245	0.45	0.014	0.09	2.75	1.10	100	−850	−950	−1100	
CR470	4.70	4.23	5.17	0.235	0.40	0.012	0.08	2.90	1.40	100	−1000	−1100	−1200	

NOTES:

1. Pulse test — steady state currents may vary.
2. Pulse test — steady state impedances may vary.
3. Min V_F required to insure $I_F > 0.8\ I_{F1(min)}$.
4. Max V_F where $I_F < 1.1\ I_{F1(max)}$ is guaranteed.

NKL, NKM, NKO

current regulator diodes designed for . . .

Siliconix

- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Low Voltage References**

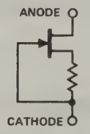
BENEFITS

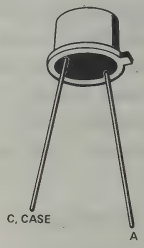
- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes
  Temperature Coefficient Better Than 0.15%/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources
  No Power Supplies Required

ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage	100 V
Forward Current	20 mA
Reverse Current	50 mA
Thermal Resistance θ_{JC}	100°C/W
Power Dissipation at T_C = 25°C	1.25 W
Operating Junction Temperature	-55 to +150°C
Storage Temperature	-55 to +200°C

TO-18 (MODIFIED)
See Section 6





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Symbol	POV	I_{F1}			Z_d		V_L	
Parameter	Peak Operating Voltage	Regulator Current			Dynamic Impedance		Limiting Voltage	
Test Conditions	$I_F = 1.1 I_{F1(Max)}$ (Note 1)	V_F = 25 V (Note 2)			V_F = 25 V (Note 3)		$I_F = 0.8 I_{F1(Min)}$ (Note 4)	
Units	Maximum Volts	(mA) Nom	Min	Max	(mΩ) Min	Typ	(V) Max	Typ
CRR0240	100	0.240	0.180	0.300	5	13	1.0	0.5
CRR0360	100	0.360	0.270	0.450	2.5	9.5	1.05	0.7
CRR0560	100	0.560	0.420	0.700	1.2	6	1.30	1.1
CRR0800	100	0.800	0.600	1.000	0.8	5.2	1.35	0.85
CRR1250	100	1.250	0.937	1.560	0.5	2.5	1.60	1.3
CRR1950	100	1.950	1.460	2.440	0.37	0.8	1.95	0.65
CRR2900	100	2.900	2.160	3.600	0.28	0.56	2.35	0.9
CRR4300	100	4.300	3.240	5.400	0.22	0.35	3.00	1.45

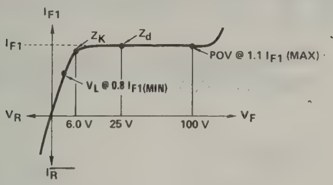
NOTES:
1. Max V_F where $I_F < 1.1\ I_{F1}$ (max) is guaranteed.
2. Pulse test — steady state current may vary.
3. Pulse test — steady state impedances may vary.
4. Min V_F required to insure $I_F > 0.8\ I_{F1}$ (min).

CRR0240-560 — NKL
CRR0800-1250 — NKM
CRR1950-4300 — NKO

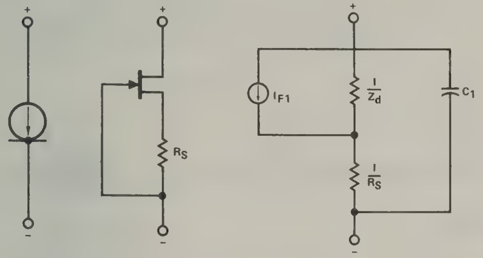
APPLICATIONS

The current-limiter diode is the electrical dual of the Zener diode.

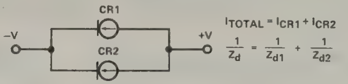
Current-Limiter Diode V-I Characteristic



EQUIVALENT CIRCUIT



Parallel Operation

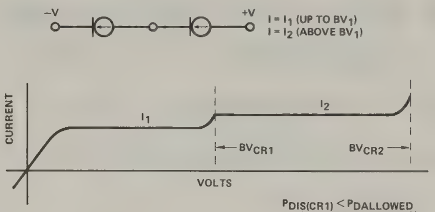


$$I_{TOTAL} = I_{CR1} + I_{CR2}$$

$$\frac{1}{Z_d} = \frac{1}{Z_{d1}} + \frac{1}{Z_{d2}}$$

Series Operation

(When $I_1 < I_2$, that is $I_2 - I_1 < 0.2\ I_1$)

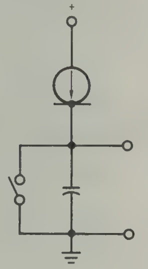


$P_{DIS(CR1)} < P_{DALLOWED}$
BV (FOR SERIES DEVICES) $= BV_1 + BV_2$

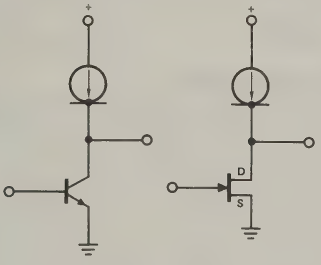
SYMBOLS AND DEFINITIONS

A	Anode (Drain)
C	Cathode (Source and Gate Shorted)
I_F	Forward Current (Anode Positive)
I_{F1}	Current at a specified Test Voltage, V_F
POV	Peak Operating Voltage
θ_I	Current Temperature Coefficient
θ_{JC}	Thermal Resistance Junction to Case
θ_{JA}	Thermal Resistance Junction to Ambient
Z_K	Knee AC Impedance at specified V_F. Z_K should be as high as possible and is specified as a minimum.
Z_d	Dynamic Impedance at specified V_F. Z_d is specified as a minimum.

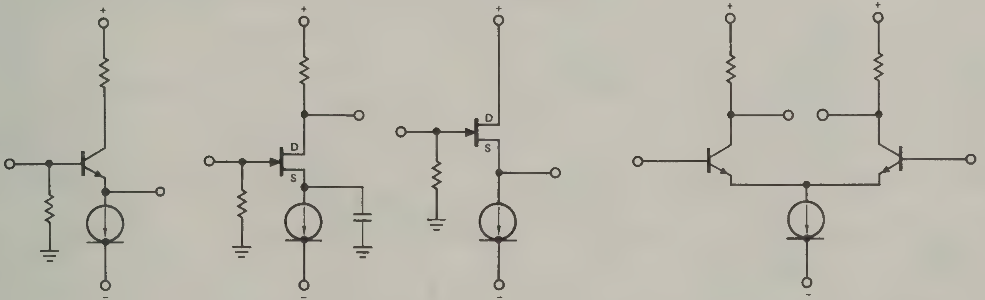
Constant-Current Timing Circuits



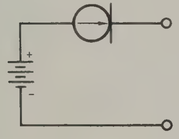
Collector or Drain Hi-Z Load Resistors



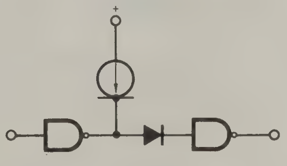
Emitter or Source Biasing



Constant-Current Supply or Current-Limiting Element



Logic Circuit Pull-Up Current Source



Siliconix

matched dual n-channel JFETs *designed for . . .*

- **Wideband Differential Amplifiers**
- **Commutators**

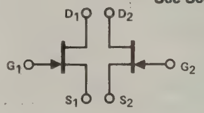
Performance Curves NCA
See Section 4

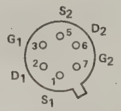
BENEFITS

- High Gain
  7500 μmho Minimum g_{fs}
- Specified Matching Characteristics

ABSOLUTE MAXIMUM RATINGS (25°C)

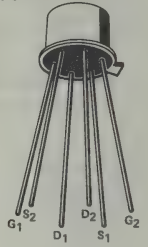
Gate–Gate Voltage	±80 V
Gate-Drain or Gate-Source Voltage	−40 V
Gate Current	50 mA
Device Dissipation (Each Side), $T_A = 25°C$ (Derate 2.2 mW/°C)	325 mW
Total Device Dissipation, $T_A = 25°C$ (Derate 3.3 mW/°C)	650 mW
Storage Temperature Range	−65 to +200°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C





Bottom View

TO-71
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate-Reverse Current		−100	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
2					−200	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5	−3		$V_{DS} = 15$ V, $I_D = 1$ nA	
5		$V_{GS(f)}$	Gate-Source Voltage		2		$V_{DS} = 0$ V, $I_G = 2$ mA	
6		I_{DSS}	Saturation Drain Current (Note 1)	5	50	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
7		$r_{DS(on)}$	Static Drain Source ON Resistance		100	Ω	$I_D = 1$ mA, $V_{GS} = 0$	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	7500	12,500	μmho	$V_{DG} = 15$ V, $I_D = 2$ mA	f = 1 kHz
				7000				f = 100 MHz
9		g_{os}	Common-Source Output Conductance		65			f = 1 kHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance		3	pF		f = 1 MHz
11		C_{iss}	Common-Source Input Capacitance		12			
12		NF	Spot Noise Figure		1.0	dB		f = 10 Hz, R_g = 1M
13		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		50	$\frac{nV}{\sqrt{Hz}}$		f = 10 Hz

		Characteristics		DN5564		DN5565		DN5566		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
14	MATCHING	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	0.95	1	–	$V_{DS} = 15$ V, $V_{GS} = 0$	
15		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		10		20	mV	$V_{DS} = 15$ V, $I_D = 2$ mA	
16		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)		10		25		50	μV/°C		T_A = 25°C T_B = 125°C
					10		25		50			T_A = −55°C T_B = 25°C
17		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1 and 2)	0.95	1	0.90	1	0.90	1	–		f = 1 kHz

NCA

NOTES:
1. Pulse test required, pulse width 300 μs, duty cycle ≤ 3%.
2. Assumes smaller value in numerator.
3. Measured at ends points, T_A and T_B.

Siliconix

matched dual n-channel JFETs *designed for...*

■ Dual FET

Performance Curves NCA-D
See Section 4

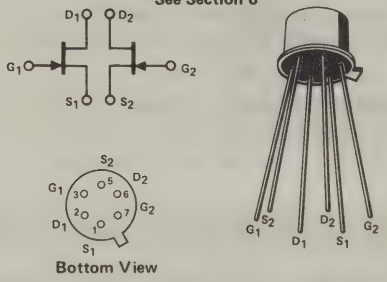
BENEFITS

- High Density
- Matched Switch Resistance
- Constant $r_{DS(on)}$ with Signal

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Gate Voltage . . . . ±80 V
Gate-Drain or Gate-Source Voltage . . . . −40 V
Gate Current . . . . 50 mA
Device Dissipation (Each Side), T_A = 25°C
(Derate 2.2 mW/°C) . . . . 325 mW
Total Device Dissipation, T_A = 25°C
(Derate 3.3 mW/°C) . . . . 650 mW
Storage Temperature Range . . . . −65°C to +200°C
Lead Temperature
(1/16″ from case for 10 seconds) . . . . 300°C

TO-71
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate-Reverse Current		−100	pA	V_{GS} = −20 V, V_{DS} = 0	
2					−200	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−40		V	I_G = 1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5	−3		V_{DS} = 15 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Voltage		2.0		V_{DS} = 0 V, I_G = 2 mA	
6		I_{DSS}	Saturation Drain Current (Note 1)	5	60	mA	V_{DS} = 15 V, V_{GS} = 0	
7		$r_{DS(on)}$	Static Drain Source ON Resistance		100	Ω	I_D = 1 mA, V_{GS} = 0	
8	DYN	C_{gd}	Drain-Gate Capacitance		7	pF	V_{GS} = −10 V	f = 1 MHz
9		C_{gs}	Gate-Source Capacitance		7		V_{DS} = 10 V	
10	MATCH	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.9	1	–	V_{DS} = 15 V, V_{GS} = 0	
11		$\lvert V_{GS1}-V_{GS2} \rvert$	Differential Gate-Source Voltage		20	mV		
12		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1 and 2)	0.9	1	–		f = 1 kHz

NOTES:

NCA-D

1. Pulse test required, pulse width 300 μs, duty cycle ⩽ 3%.
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.

DPAD1 DPAD2 DPAD5 DPAD10
DPAD20 DPAD50 DPAD100

Siliconix

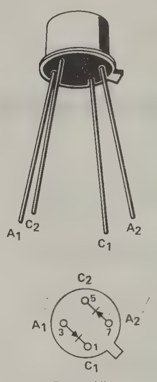
dual pico ampere diodes
designed for . . .

- **Clipping Circuits**
- **Diode Switching**
- **High Impedance Protection Circuits**

BENEFITS

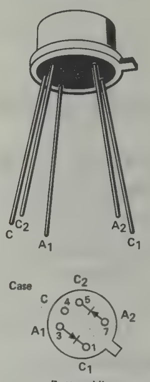
- Very High Off-Isolation
  1 pA Max (DPAD1)
- High Isolation Between Diodes
  20 Femto Amp Typical (DPAD1)
- Matched Capacitances
- Compact Packaging

TO-71 (MODIFIED)
(Pins 2 and 6 Removed)
See Section 6



Bottom View
(Alternate)

TO-78 (MODIFIED)
(DPAD1 Only)
See Section 6



Bottom View

ABSOLUTE MAXIMUM RATINGS (25°C)

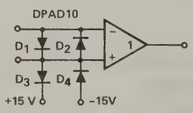
Forward Gate Current, Each Side	50 mA
Total Device Dissipation @ $T_A = 25°C$ Derate 4.0 mW/°C to 125°C	400 mW
Storage Temperature Range	−55 to +125°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

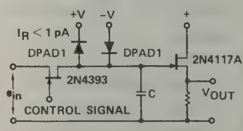
		CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITION	
1	STATIC	I_R	Reverse Current			−1	pA	$V_R = -20$ V	DPAD1
2						−2			DPAD2
3						−5			DPAD5
4						−10			DPAD10
5						−20			DPAD20
6						−50			DPAD50
7						−100			DPAD100
8		B_{VR}	Reverse Breakdown Voltage	−45		−120	V	$I_R = -1\ \mu A$	DPAD1, 2, 5
9				−35					DPAD10, 20, 50, 100
10		V_F	Forward Voltage Drop		0.8	1.5		$I_F = 1$ mA	DPAD1, 2, 5, 10, 20, 50, 100
11	DYN	C_R	Capacitance			0.8	pF	$V_R = -5$ V, f = 1 MHz	DPAD1, 2, 5
12						2.0			DPAD10, 20, 50, 100
13	MAT	$\lvert C_{R1}-C_{R2}\rvert$	Differential Capacitance		0.1	0.2	pF	$V_{R1} = V_{R2} = -5$ V, f = 1 MHz	DPAD1, 2, 5, 10, 20, 50, 100

APPLICATION

Operational Amplifier Protection. Input Differential Voltage limited to 0.8 V (typ) by DPADS D_1 and D_2 Common mode input voltage limited by DPADS D_3 and D_4 to ±15 V.



Typical sample and hold circuit with clipping. DPAD diodes reduce offset voltages fed capacitively from the FET switch gate.



FN4117 FN4117A FN4118 FN4118A FN4119 FN4119A
SEE ALSO 2N4117 SERIES

Siliconix

n-channel JFETs
designed for . . .

Performance Curves NT
See Section 4

■ Ultra-High Input Impedance Amplifiers

Electrometers
pH Meters
Smoke Detectors

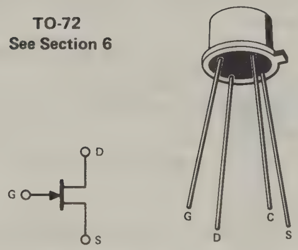
BENEFITS

- Low Power
  $I_{DSS} < 0.2$ mA (FN4117)
- Minimum Circuit Loading
  $I_{GSS} < 1$ pA (FN4117A Series)

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	-40 V
Gate-Current	50 mA
Total Device Dissipation (Derate 2 mW/°C to 175°C)	300 mW
Storage Temperature Range	-65 to +175°C
Lead Temperature (1/16" from case for 10 seconds)	255°C

TO-72
See Section 6



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	FN4117 FN4117A		FN4118 FN4118A		FN4119 FN4119A		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current FN4117 Series Only		-10		-10		-10	pA	V_{GS} = -20 V, V_{DS} = 0	
2					-25		-25		-25	nA		150°C
3		I_{GSS}	Gate Reverse Current FN4117A Series Only		-5		-5		-5	pA	V_{GS} = -20 V, V_{DS} = 0	
4					-2.5		-2.5		-2.5	nA		150°C
5		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0	
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.6	2.0	-1	-3	-2	-6		V_{DS} = 10 V, I_D = 1 nA	
7		I_{DSS}	Saturation Drain Current (Note 2)	0.03	0.2	0.08	0.4	0.20	1.2	mA	V_{DS} = 10 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	70	210	80	250	100	330	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
9		g_{os}	Common-Source Output Conductance		3		5		10			
10		C_{iss}	Common-Source Input Capacitance		3		3		3	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5		1.5			

NT

*JEDEC registered data.

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. This parameter is measured during a 2 ms interval 100 ms after power is applied. (Not a JEDEC condition.)

n-channel JFETs designed for . . .

Siliconix

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

Performance Curves NCA
See Section 4

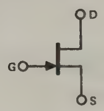
BENEFITS

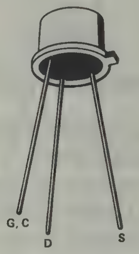
- Low Insertion Loss, High Accuracy in Test Systems r_{ON}
- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- High Off-Isolation $I_{D(off)} < 100$ pA
- High Speed $t_{ON} < 20$ ns

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . –40 V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Derate 10 mW/°C) . . . . 1.8 W
Storage Temperature Range . . . . –65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . 300°C

TO-18
See Section 6

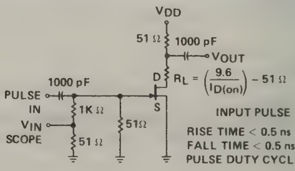




*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		FN4392		FN4393		Unit	Test Conditions			
				Min	Max	Min	Max					
1	STATIC	I_{GSS}	Gate Reverse Current		-100		-100	pA	V_{GS} = -20 V, V_{DS} = 0			
2					-200		-200	nA			150°C	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		V	I_G = -1 μA, V_{DS} = 0			
4		$I_{D(off)}$	Drain Cutoff Current				100	pA	V_{DS} = 20 V	V_{GS} = -5 V		
5							200	nA			150°C	
6					100			pA				
7					200			nA			150°C	
8		$V_{GS(f)}$	Gate-Source Forward Voltage		1		1	V	I_G = 1 mA, V_{DS} = 0			
9		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-2	-5	-0.5	-3		V_{DS} = 20 V, I_D = 1 nA			
10		I_{DSS}	Saturation Drain Current (Note 1)	25	100	5	60	mA	V_{DS} = 20 V, V_{GS} = 0			
11		$V_{DS(on)}$	Drain Source ON Voltage				0.4	V	V_{GS} = 0	I_D = 3 mA		
12					0.4					I_D = 6 mA		
13										I_D = 12 mA		
14		$r_{DS(on)}$	Static Drain-Source ON Resistance		60		100	Ω	V_{GS} = 0, I_D = 1 mA			
15	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		60		100	Ω	V_{GS} = 0, I_D = 0		f = 1 kHz	
16		C_{iss}	Common-Source Input Capacitance		16		16	pF	V_{DS} = 20 V, V_{GS} = 0		f = 1 MHz	
17		C_{rss}	Common-Source Reverse Transfer Capacitance				5		V_{DS} = 0	V_{GS} = - 5 V		
18					5					V_{GS} = - 7 V		
19										V_{GS} = -12 V		
20	SW	$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	V_{DD} = 10 V, $V_{GS(on)}$ = 0			
21		t_r	Rise Time		5		5			$I_{D(on)}$	$V_{GS(off)}$	R_L
22		$t_{d(off)}$	Turn-OFF Delay Time		35		50		FN4392	6	-7	1.6K Ω
23		t_f	Fall Time		20		30		FN4393	3	-5	3.2K Ω

NOTE:
1. Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%.



NCA

INPUT PULSE
RISE TIME < 0.5 ns
FALL TIME < 0.5 ns
PULSE DUTY CYCLE 1%

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 50 Ω

n-channel JFETs *designed for . . .*

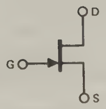
Siliconix

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves NVA
See Section 4

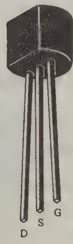
BENEFITS

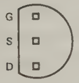
- Very Low Insertion Loss
  $r_{DS(on)} < 3\ \Omega$ (J105)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver



TO-92
See Section 6

Plastic





Bottom View

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . –25 V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J105			J106			J107			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-3			-3			-3	nA	$V_{DS} = 0\ V$, $V_{GS} = -15\ V$	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4.5		-10	-2		-6	-0.5		-4.5	V	$V_{DS} = 5\ V$, $I_D = 1\ \mu A$	
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25			–25			–25				$V_{DS} = 0\ V$, $I_G = -1\ \mu A$	
4		I_{DSS}	Drain Saturation Current (Note 2)	500			200			100			mA	$V_{DS} = 15\ V$, $V_{GS} = 0\ V$	
5		$I_{D(off)}$	Drain Cutoff Current (Note 1)			3			3			3	nA	$V_{DS} = 5\ V$, $V_{GS} = -10\ V$	
6		$r_{DS(on)}$	Drain Source ON Resistance			3			6			8	Ω	$V_{DS} \leqslant 0.1\ V$, $V_{GS} = 0\ V$	
7	DYNAMIC	$C_{dg(off)}$	Drain Gate OFF Capacitance			35			35			35	pF	$V_{DS} = 0\ V$, $V_{GS} = -10\ V$	f = 1 MHz
8		$C_{sg(off)}$	Source Gate OFF Capacitance			35			35			35			
9		$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate plus Source Gate ON Capacitance			160			160			160		$V_{DS} = V_{GS} = 0\ V$	
10		$t_{d(on)}$	Turn On Delay Time		15			15			15		ns	Switching Time Test Conditions J105 J106 J107 V_{DD} 1.5 V 1.5 V 1.5 V $V_{GS(off)}$ -12 V -7 V -5 V R_L 50 Ω 50 Ω 50 Ω	
11		t_r	Rise Time		20			20			20				
12		$t_{d(off)}$	Turn Off Delay Time		15			15			15				
13		t_f	Fall Time		20			20			20				

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ⩽ 3%.

NVA

Siliconix

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Choppers**
- **Commutators**
- **Low Noise Audio Amplifiers**

Performance Curves NIP
See Section 4

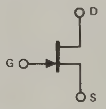
BENEFITS

- Low Cost
- Automated Insertion Package
- Low Insertion Loss
  $r_{DS(on)} < 8\ \Omega$ (J108)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Fast Switching
  $t_{d(on)} + t_r = 5$ ns Typical
- Low Noise
  $\overline{e_n} = 6\ \text{nV}/\sqrt{\text{Hz}}$ at 10 Hz, Typ (J110)

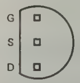
ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . –25V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . 300°C

TO-92
See Section 6



Plastic



Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J108			J109			J110			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			–3			–3			–3	nA	$V_{DS} = 0\ V, V_{GS} = -15\ V$	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–3		–10	–2		–6	–0.5		–4	V	$V_{DS} = 5\ V, I_D = 1\ \mu A$	
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25			–25			–25				$V_{DS} = 0\ V, I_G = -1\ \mu A$	
4		I_{DSS}	Drain Saturation Current (Note 2)	80			40			10			mA	$V_{DS} = 15\ V, V_{GS} = 0\ V$	
5		$I_{D(off)}$	Drain Cutoff Current (Note 1)			3			3			3	nA	$V_{DS} = 5\ V, V_{GS} = -10\ V$	
6		$r_{DS(on)}$	Drain-Source ON Resistance			8			12			18	Ω	$V_{DS} \leq 0.1\ V, V_{GS} = 0\ V$	
7	DYNAMIC	$C_{dg(off)}$	Drain-Gate OFF Capacitance			15			15			15	pF	$V_{DS} = 0\ V, V_{GS} = -10\ V$	f = 1 MHz
8		$C_{sg(off)}$	Source-Gate OFF Capacitance			15			15			15			
9		$C_{dg(on)} + C_{sg(on)}$	Drain-Gate Plus Source-Gate ON Capacitance			85			85			85		$V_{DS} = V_{GS} = 0$	
10		$t_{d(on)}$	Turn ON Delay Time		4			4			4		ns	Switching Time Test Conditions J108 J109 J110 V_{DD} 1.5 V 1.5 V 1.5 V $V_{GS(off)}$ –12 V –7 V –5 V R_L 150 Ω 150 Ω 150 Ω	
11		t_r	Rise Time		1			1			1				
12		$t_{d(off)}$	Turn OFF Delay Time		6			6			6				
13		t_f	Fall Time		30			30			30				

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse Test duration 300 μs; duty cycle ≤ 3%.

NIP

n-channel FETs *designed for . . .*

- **Analog Switches**
- **Choppers**
- **Commutators**

Siliconix

Performance Curves NCA
See Section 4

BENEFITS

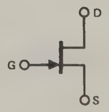
- Low Cost
- Automated Insertion Package
- Low Insertion Loss
  $r_{DS(on)} < 30\ \Omega$ (J111)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Fast Switching
  $t_{d(on)} + t_r = 13$ ns Typical
- Short Sample and Hold Aperture Time
  $C_{gd(off)} < 5$ pF
  $C_{gs(off)} < 5$ pF

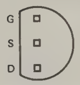
ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	–35V
Gate Current	50 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	–55 to 135°C
Storage Temperature Range	–55 to 150°C
Lead Temperature Range (1/16″ from case for 10 seconds)	300°C

Plastic

TO-92
See Section 6





Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J111 Min	J111 Typ	J111 Max	J112 Min	J112 Typ	J112 Max	J113 Min	J113 Typ	J113 Max	UNIT	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			–1			–1			–1	nA	$V_{DS} = 0$ V, $V_{GS} = -15$ V	
2		$V_{GS(off)}$	Gate Source Cutoff Voltage	–3		–10	–1		–5			–3	V	$V_{DS} = 5$ V, $I_D = 1\ \mu A$	
3		BV_{GSS}	Gate Source Breakdown Voltage	35			–35			–35				$V_{DS} = 0$ V, $I_G = -1\ \mu A$	
4		I_{DSS}	Drain Saturation Current (Note 2)	20			5			2			mA	$V_{DS} = 15$ V, $V_{GS} = 0$ V	
5		$I_{D(off)}$	Drain Cutoff Current (Note 1)			–1			–1			–1	nA	$V_{DS} = 5$ V, $V_{GS} = -10$ V	
6		$r_{DS(on)}$	Drain Source ON Resistance			30			50			100	Ω	$V_{DS} = 0.1$ V, $V_{GS} = 0$ V	
7	DYNAMIC	$C_{dg(off)}$	Drain Gate OFF Capacitance			5			5			5	pF	$V_{DS} = 0$ V, $V_{GS} = -10$ V	f = 1 MHz
8		$C_{sg(off)}$	Source Gate OFF Capacitance			5			5			5			
9		$C_{dg(on)} + C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance			28			28			28		$V_{DS} = V_{GS} = 0$	
10		$t_{d(on)}$	Turn On Delay Time		7			7			7		ns	Switching Time Test Conditions J111 / J112 / J113 V_{DD}: 10 V / 10 V / 10 V $V_{GS(off)}$: –12 V / –7 V / –5 V R_L: 800 Ω / 1,600 Ω / 3,200 Ω	
11		t_r	Rise Time		6			6			6				
12		$t_{d(off)}$	Turn Off Delay Time		20			20			20				
13		t_f	Fall Time		15			15			15				

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse Test duration 300 μs; duty cycle $\leqslant$ 3%.

NCA

n-channel JFETs
designed for . . .

- **Analog Switches**
- **Choppers**
- **Commutators**

Siliconix

Performance Curves NCA
See Section 4

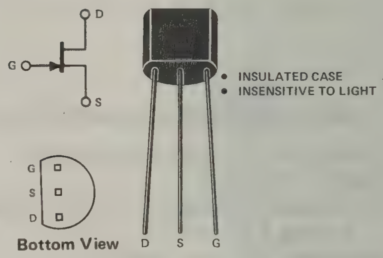
BENEFITS

- Low Insertion Loss
  $r_{DS(on)} < 30\ \Omega$ (J111A)
- High Off-Isolation
  $I_{D(off)} < 200$ pA
- No Error or Offset Voltages Generated by Closed Switch
  Purely Resistive

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	−40 V
Gate Current	50 mA
Drain Current	400 mA
Total Device Dissipation (25°C Free Air Temperature)	350 mW
Power Derating (to +125°C)	3.5 mW/°C
Storage Temperature Range	−55 to +125°C
Operating Temperature Range	−55 to +125°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

TO-92
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J111A		J112A		J113A		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)		−200		−200		−200	pA	$V_{DS} = 0$, $V_{GS} = -15$ V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−5	−10	−2	−7	−1	−5	V	$V_{DS} = 5$ V, $I_D = 1\ \mu$A	
3		BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		−40			$V_{DS} = 0$, $I_G = -1\ \mu$A	
4		I_{DSS}	Saturation Drain Current (Note 2)	30		15		8		mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
5		$I_{D(off)}$	Drain Cutoff Current (Note 1)		200		200		200	pA	$V_{DS} = 5$ V, $V_{GS} = -10$ V	
6		$r_{DS(on)}$	Drain Source ON Resistance		30		50		80	Ω	$V_{DS} \leqslant 0.1$ V, $V_{GS} = 0$	
7	DYN	$C_{dg(off)}$	Drain Gate OFF Capacitance		5		5		5	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
8		$C_{sg(off)}$	Source-Gate OFF Capacitance		5		5		5			
9		$C_{dg(on)} + C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance		28		28		28		$V_{DS} = V_{GS} = 0$	

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ⩽ 3%.

NCA

Siliconix

p-channel JFETs *designed for . . .*

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves PSA
See Section 4

BENEFITS

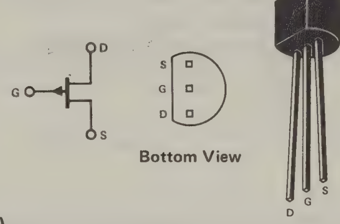
- Low Cost
- Simplifies Series-Shunt Switching when Combined with J113, its N-Channel Complement
- Low Insertion Loss
  - $r_{DS(on)} < 85\ \Omega$ (J174)
- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- Short Sample and Hold Aperture Time
  - $C_{sg(off)} < 5.5$ pF
  - $C_{dg(off)} < 5.5$ pF
- Fast Switching
  - $t_{d(on)} + t_r = 7$ ns Typical

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) 30V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . —55 to 135°C
Storage Temperature Range . . . . —55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . 300°C

TO-92
See Section 6

Plastic



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristics		J174			J175			J176			J177			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			1			1			1			1	nA	$V_{DS} = 0$, $V_{GS} = 20$ V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	5		10	3		6	1		4	0.8		2.25	V	$V_{DS} = -15$ V, $I_D = -10$ nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	30			30			30			30				$V_{DS} = 0$, $I_G = 1\ \mu A$	
4		I_{DSS}	Saturation Drain Current (Note 3)	-20		-125	-7		-70	-2		-35	-1.5		-20	mA	$V_{DS} = -15$ V, $V_{GS} = 0$	
5		$I_{D(off)}$	Drain Cutoff Current (Note 2)			-1			-1			-1			-1	nA	$V_{DS} = -15$ V, $V_{GS} = 10$ V	
6		$r_{DS(on)}$	Drain-Source ON Resistance			85			125			250			300	Ω	$V_{GS} = 0$, $V_{DS} = -0.1$ V	
7	DYNAMIC	$C_{dg(off)}$	Drain-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	$V_{DS} = 0$, $V_{GS} = 10$ V	f = 1 MHz
8		$C_{sg(off)}$	Source-Gate OFF Capacitance		5.5			5.5			5.5			5.5				
9		$C_{dg(on)} + C_{sg(on)}$	Drain-Gate Plus Source-Gate ON Capacitance		32			32			32			32			$V_{DS} = V_{GS} = 0$	
10		$t_{d(on)}$	Turn On Delay Time		2			5			15			20		ns	Switching Time Test Conditions J174 J175 J176 J177 V_{DD} -10 V -6 V -6 V -6 V $V_{GS(off)}$ 12 V 8 V 6 V 3 V R_L 560 Ω 1.2 KΩ 5.6 KΩ 10 KΩ $V_{GS(on)}$ 0 V 0 V 0 V 0 V	
11		t_r	Rise Time		5			10			20			25				
12		$t_{d(off)}$	Turn Off Delay Time		5			10			15			20				
13		t_f	Fall Time		10			20			20			25				

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 300 μs; duty cycle ⩽ 3%.

PSA

Siliconix

n-channel JFETs *designed for . . .*

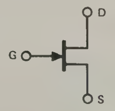
■ General Purpose Amplifiers

Performance Curves NPA
See Section 4

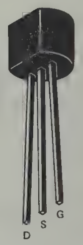
BENEFITS

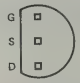
- High Input Impedance
  I_G = 35 pA Typical
- Good for Low Power Supply Operation
  $V_{GS(off)} < 1.5$ V (J201)

TO-92
See Section 6



Plastic





Bottom View

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . –40 V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J201			J202			J203			J204			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			-100			-100			-100			-100	pA	V_{DS} = 0, V_{GS} = -20 V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.3		-1.5	-0.8		-4.0	-2.0		-10.0	–0.3		-2.0	V	V_{DS} = 20 V, I_D = 10 nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40			-40			-40			-25				V_{DS} = 0, I_G = –1 μA	
4		I_{DSS}	Saturation Drain Current (Note 3)	0.2		1.0	0.9		4.5	4.0		20	0.2	1.2	3	mA	V_{DS} = 20 V, V_{GS} = 0	
5		I_G	Gate Current (Note 2)		-35			-35			-35			-35		pA	V_{DG} = 20 V, I_D = $I_{DSS(min)}$	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	500			1,000			1,500			500	1500		μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		1			3.5			10			2.5				
8		C_{iss}	Common-Source Input Capacitance		4			4			4			4		pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1			1			1			1				
10		$\overline{e}_n$	Equivalent Short-Circuit Input Noise Voltage		5			5			5			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

NPA

n-channel JFETs *designed for . . .*

Siliconix

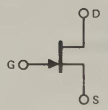
## ■ General Purpose Amplifiers

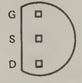
Performance Curves NZF
See Section 4

BENEFITS

- High Gain
  g_{fs} = 7000 μmho Minimum (J211, J212)
- High Input Impedance
  I_{GSS} = 100 pA Maximum
  C_{iss} = 5 pF Typical

TO-92
See Section 6





Bottom View

Plastic

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	−25 V
Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	−55 to 135°C
Storage Temperature Range	−55 to 150°C
Lead Temperature Range (1/16″ from case for 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J210			J211			J212			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			−100			−100			−100	pA	V_{DS} = 0, V_{GS} = −15 V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−1		−3	−2.5		−4.5	−4		−6	V	V_{DS} = 15 V, I_D = 1 nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	−25			−25			−25				V_{DS} = 0, I_G = −1 μA	
4		I_{DSS}	Saturation Drain Current (Note 2)	2		15	7		20	15		40	mA	V_{DS} = 15 V, V_{GS} = 0	
5		I_G	Gate Current (Note 1)		−10			−10			−10		pA	V_{DG} = 10 V, I_D = 1 mA	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	4,000		12,000	6,000		12,000	7,000		12,000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance			150			200			200			
8		C_{iss}	Common-Source Input Capacitance		4			4			4		pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1			1			1				
10		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$		f = 1 kHz

NZF

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.

n-channel JFETs designed for . . .

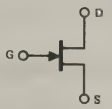
■ Audio and Sub-Audio Amplifiers

Performance Curves NPA
See Section 4

BENEFITS

- Ultra Low Noise
  $\overline{e}_n = 8\ nV/\sqrt{Hz}$ Typical at 10 Hz
  $\overline{e}_n = 2\ nV/\sqrt{Hz}$ Typical at 1 kHz

TO-92
See Section 6



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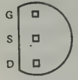


Bottom View

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	−40V
Gate Current	50 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	−55 to 135°C
Storage Temperature Range	−55 to 150°C
Lead Temperature Range (1/16″ from case for 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic				J230			J231			J232			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			-250			-250			-250	pA	$V_{DS} = 0$, $V_{GS} = -30$ V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5		-3	-1.5		-5	-3		-6	V	$V_{DS} = 20$ V, $I_D = 1\ \mu A$	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40			-40			-40				$V_{DS} = 0$, $I_G = -1\ \mu A$	
4		I_{DSS}	Saturation Drain Current (Note 3)	0.7		3	2		6	5		10	mA	$V_{DS} = 20$ V, $V_{GS} = 0$	
5		I_G	Gate Current (Note 2)		-10			-10			-10		pA	$V_{DG} = 10$ V, $I_D = 0.5$ mA	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	1,000		3,500	1,500		4,000	2,500		5,000	μmho	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		1.5			3			5				
8		C_{iss}	Common-Source Input Capacitance		12			12			12		pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		2			2			2				
10		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		8	30		8	30		8	30	$\frac{nV}{\sqrt{Hz}}$	$V_{DS} = 10$ V, $V_{GS} = 0$	f = 10 Hz
11					2			2			2				f = 1 kHz

NOTES:

1. Geometry is symmetrical. Unit may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

NPA

p-channel JFETs *designed for . . .*

Siliconix

■ General Purpose Amplifiers

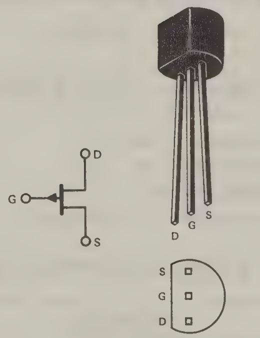
Performance Curves PSA
See Section 4

BENEFITS

- **Low Cost**
- **Automatic Insertion Package**
- **High Gain Amplifiers**
  g_{fs} = 14,000 μmho Typical (J271)
- **Low Noise**
  $\overline{e}_n$ = 6 nV/$\sqrt{\text{Hz}}$ at 1 kHz Typical

TO-92
See Section 6

Plastic



Bottom View

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate Source Voltage (Note 1) . . . . 30 V
Gate Current . . . . –50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . –55 to 135°C
Storage Temperature Range . . . . –55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J270			J271			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			200			200	pA	V_{DS} = 0, V_{GS} = 20 V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	0.5		2.0	1.5		4.5	V	V_{DS} = –15 V, I_D = –1 nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	30			30				V_{DS} = 0, I_G = 1 μA	
4		I_{DSS}	Saturation Drain Current (Note 3)	–2		–15	–6		–50	mA	V_{DS} = –15 V, V_{GS} = 0	
5		I_G	Gate Current (Note 2)		15			60		pA	V_{DG} = –15 V, I_D = $I_{DSS(min)}$	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	6,000		15,000	8,000		18,000	μmho	V_{DS} = –15 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance			200			500			
8		C_{iss}	Common-Source Input Capacitance		32			32		pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		4			4				
10		e_n	Equivalent Short-Circuit Input Noise Voltage		6			6		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = –10 V, I_D = $I_{DSS(min)}$	f = 1 kHz

NOTES:

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

PSA

n-channel JFETs designed for . . .

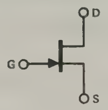
- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

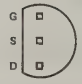
Performance Curves NZF
See Section 4

BENEFITS

- High Power Gain
  20–23 dB Typical at 100 MHz, Common-Source
  17.5–20.5 dB Typical at 100 MHz, Common-Gate
- Low Noise Figure
  1.3 dB Typical at 100 MHz
- High Dynamic Range
  Greater than 100 dB

TO-92
See Section 6





Bottom View

Plastic

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . –25 V
Gate Current . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . –55 to 135°C
Storage Temperature Range . . . . –55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–0.5	nA	V_{GS} = –15 V, V_{DS} = 0	
2					–0.1	μA		T_A = 125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25		V	I_G = –1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage (Note 1)	–1.5	–7.0		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1, 2)	4	45	mA	V_{DS} = 10 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	4500	9000	μmho	V_{DS} = 10 V, I_D = 5 mA, f = 1 kHz	
7		g_{os}	Common-Source Output Conductance		200			
8		C_{rss}	Common-Source Reverse Transfer Capacitance		1.7	pF	V_{DG} = 10 V, I_D = 5 mA, f = 1 MHz	
9		C_{iss}	Common-Source Input Capacitance		5.5			

Characteristic		J300A		J300B		J300C		J300D		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
I_{DSS} (Note 2)	Saturation Drain Current	4	9	7	15	12	25	21	45	mA	V_{DS} = 10V V_{GS} = 0V
$V_{GS(off)}$	Gate Source Cutoff Voltage	–1.5	–3.0	–2.0	–4.0	–2.5	–5.0	–3.5	–7.0	V	V_{DS} = 10V I_D = 1 nA

NOTES:
1. I_{DSS} and $V_{GSS(off)}$ are selected into 5 ranges and labeled according to above table.
2. Pulse test PW ≤ 300 μs, duty cycle ≤ 3%.

NZF

n-channel JFETs *designed for . . .*

- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

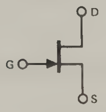
Siliconix

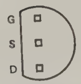
Performance Curves NH
See Section 4

BENEFITS

- Characterized for Operation at 100 and 400 MHz
- Low Noise
  NF = 1.7 dB Typical at 100 MHz

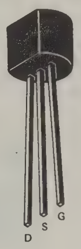
TO-92
See Section 6





Bottom View

Plastic



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . -30 V
Gate Current . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . −55 to 135°C
Storage Temperature Range. . . . . −55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J304			J305			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-100			-100	pA	V_{DS} = 0, V_{GS} = -20 V	
2		$V_{GS(off)}$	Gate Source Cutoff Voltage	-2		-6	-0.5		-3	V	V_{DS} = 15 V, I_D = 1 nA	
3		BV_{GSS}	Gate Source Breakdown Voltage	-30			-30				V_{DS} = 0, I_G = -1 μA	
4		I_{DSS}	Saturation Drain Current (Note 2)	5		15	1		8	mA	V_{DS} = 15 V, V_{GS} = 0	
5	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	4,500		7,500	3,000			μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
6		g_{os}	Common-Source Output Transconductance			50			50			
7		C_{iss}	Common-Source Input Capacitance		3.5			3.5		pF		f = 1 MHz
8		C_{rss}	Common-Source Reverse Transfer Capacitance		0.85			0.85				
9		C_{oss}	Common-Source Output Capacitance		1.0			1.0				
10	HIGH FREQUENCY	g_{fs}	Common-Source Forward Transconductance					3,000		μmho	V_{DS} = 15 V, V_{GS} = 0	f = 100 MHz
11					4,200							f = 400 MHz
12		g_{oss}	Common-Source Output Conductance		60			60				f = 100 MHz
13					80							f = 400 MHz
14		b_{oss}	Common-Source Output Susceptance		800			800				f = 100 MHz
15					3,600							f = 400 MHz
16		g_{iss}	Common-Source Input Conductance		80			80				f = 100 MHz
17					800							f = 400 MHz
18		b_{iss}	Common-Source Input Susceptance		2,000			2,000				f = 100 MHz
19					7,500							f = 400 MHz
20		G_{ps}	Common-Source Power Gain		20					dB	V_{DS} = 15 V, I_D = 5 mA	f = 100 MHz
21					11							f = 400 MHz
22		NF	Noise Figure (Single Sideband)		1.7						V_{DS} = 15 V, I_D = 5 mA, R_G = 1 KΩ	f = 100 MHz
23					3.8							f = 400 MHz

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.

NH

J308 J309 J310

n-channel JFETs *designed for . . .*

Siliconix

- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

ABSOLUTE MAXIMUM RATINGS (25°C)

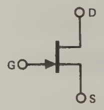
Drain-Gate Voltage . . . . .25 V
Source-Gate Voltage . . . . .25 V
Forward Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
  (Derate 3.27 mW/°C). . . . . .360 mW
Operating Temperature Range. . . . .−55 to 135°C
Storage Temperature Range. . . . .−55 to 150°C
Lead Temperature Range
  (1/16″ from case for 10 seconds) . . . . .300°C

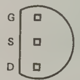
Performance Curves NZA
See Section 4

BENEFITS

- Industry Standard Part
  In Low Cost Plastic Package
- High Power Gain
  11 dB Typical at 450 MHz
  Common-Gate
- Low Noise
  2.7 dB Typical at 450 MHz
- Wide Dynamic Range
  Greater than 100 dB
- Easily Matches to 75 Ω Input

TO-92
See Section 6





Bottom View

Plastic

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J308			J309			J310			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−25			−25			−25			V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current			−1.0			−1.0			−1.0	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	
3						−1.0			−1.0			−1.0	µA		T = +125°C
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−1.0		−6.5	−1.0		−4.0	−2.0		−6.5	V	$V_{DS} = 10$ V, $I_D = 1$ nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	$V_{DS} = 10$ V, $V_{GS} = 0$	
6		$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	$V_{DS} = 0$, $I_G = 1$ mA	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	8,000	17,000		10,000	17,000		8,000	17,000		µmhos	$V_{DS} = 10$ V, $I_D = 10$ mA	f = 1 kHz
8		g_{os}	Common-Source Output Conductance			250			250			250			
9		g_{fg}	Common-Gate Forward Transconductance		13,000			13,000			12,000				
10		g_{og}	Common-Gate Output Conductance		150			100			150				
11		C_{gd}	Gate-Drain Capacitance		1.8	2.5		1.8	2.5		1.8	2.5	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
12		C_{gs}	Gate-Source Capacitance		4.3	5.0		4.3	5.0		4.3	5.0			
13		$\overline{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	$V_{DS} = 10$ V, $I_D = 10$ mA	f = 100 Hz
14	HI FREQ	$Re(y_{fs})$	Common-Source Forward Transconductance		12			12			12		mmho	$V_{DS} = 10$ V, $I_D = 10$ mA	f = 105 MHz
15		$Re(y_{ig})$	Common-Gate Input Conductance		14			14			14				
16		$Re(y_{is})$	Common-Source Input Conductance		0.4			0.4			0.4				
17		$Re(y_{os})$	Common-Source Output Conductance		0.15			0.15			0.15				
18		G_{pg}	Common-Gate Power Gain at Noise Match		16			16			16		dB		
19		NF	Noise Figure		1.5			1.5			1.5				
20		G_{pg}	Common-Gate Power Gain at Noise Match		11			11			11				f = 450 MHz
21		NF	Noise Figure		2.7			2.7			2.7				

NOTE:
1. Pulse test PW 300 µs, duty cycle ≤ 3%.

NZA

n-channel JFETs current regulator diodes

Siliconix

designed for . . .

- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Linear Ramp and Staircase Generator**

Performance Curves NCL
See Section 4

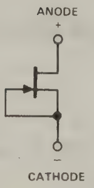
BENEFITS

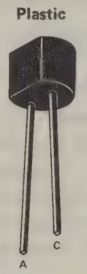
- Low Cost
- Simple Two Lead Current Source
- Simplifies Floating Current Sources No Power Supplies Required
- Good Operating Current Tolerance ±20%

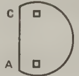
ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage . . . . 50 V
Forward Current . . . . 20 mA
Reverse Current . . . . 50 mA
Total Device Dissipation at 25°C Ambient
  (Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . −55 to 135°C
Storage Temperature Range . . . . −55 to 150°C
Lead Temperature Range
  (1/16" from case for 10 seconds) . . . . 300°C

TO-92 (MODIFIED)
See Section 6







Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

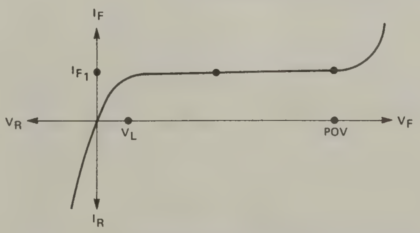
			Characteristic		J500	J501	J502	J503	J504	J505	Unit	Test Conditions
1	STATIC	I_{FI}	Forward Current (Note 1)	Min	0.192	0.264	0.344	0.448	0.600	0.800	mA	V_F = 25 V
2				Nominal	0.240	0.330	0.430	0.560	0.750	1.000		
3				Max	0.288	0.396	0.516	0.672	0.900	1.200		
4		POV	Peak Operating Voltage (Notes 1 and 2)	Min	50	50	50	50	50	50	V	$I_F = 1.1\ I_{FI}$ (Max)
5		V_L	Limiting Voltage (Note 3)	Max	1.2	1.3	1.5	1.7	1.9	2.1		$I_F = 0.9\ I_{FI}$ (Min)
6				Typ	0.8	0.9	1.1	1.2	1.4	1.5		
7	DYN	Z_{FI}	Small-Signal Dynamic Impedance (Note 1)	Min	4.0	2.2	1.5	1.2	0.8	0.5	MΩ	V_F = 25 V, f = 1 kHz
8				Typ	8.0	6.0	4.4	3.4	2.5	1.9		
9		C_F	Anode-Cathode Capacitance	Typ	2	2	2	2	2	2	pF	V_F = 25 V, f = 1 MHz

NCL

NOTES:

1. Pulse test duration = 2 ms.
2. Maximum V_F where $I_F < 1.1\ I_{FI(Max)}$ is guaranteed.
3. Minimum V_F required to insure $I_F > 0.9\ I_{FI(Min)}$.

Current-Limiter Diode
V-I Characteristic



Siliconix

n-channel JFETs current regulator diodes

designed for . . .

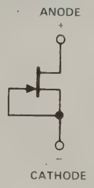
- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Linear Ramp and Staircase Generator**

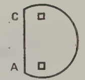
Performance Curves NCL
See Section 4

BENEFITS

- Low Cost
- Simple Two Lead Current Source
- Simplifies Floating Current Sources No Power Supplies Required
- Good Operating Current Tolerance ±20%

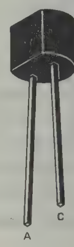
TO-92 (MODIFIED)
See Section 6





Bottom View

Plastic



ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage. . . . . .50 V
Forward Current . . . . 20 mA
Reverse Current. . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . .300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

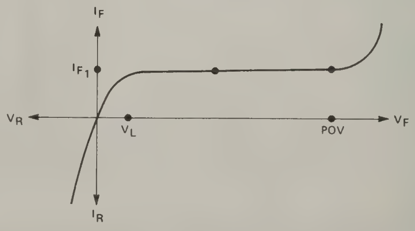
		Characteristic			J506	J507	J508	J509	J510	J511	Unit	Test Conditions
1	STATIC	I_{FI}	Forward Current (Note 1)	Min	1.120	1.440	1.9	2.4	2.9	3.8	mA	V_F = 25 V
2				Nominal	1.400	1.800	2.4	3.0	3.6	4.7		
3				Max	1.680	2.160	2.9	3.6	4.3	5.6		
4		POV	Peak Operating Voltage (Notes 1 and 2)	Min	50	50	50	50	50	50	V	$I_F = 1.1\ I_{FI}$ (Max)
5		V_L	Limiting Voltage (Note 3)	Max	2.5	2.8	3.1	3.5	3.9	4.2		$I_F = 0.9\ I_{FI}$ (Min)
6				Typ	1.8	2.0	2.2	2.5	2.8	3.0		
7	DYN	Z_{FI}	Small-Signal Dynamic Impedance (Note 1)	Min	0.33	0.2	0.2	0.15	0.15	0.12	MΩ	V_F = 25 V, f = 1 kHz
8				Typ	1.4	1.0	0.70	0.60	0.50	0.30		
9		C_F	Anode-Cathode Capacitance	Typ	2	2	2	2	2	2	pF	V_F = 25 V, f = 1 MHz

NOTES:

1. Pulse test duration = 2 ms.
2. Maximum V_F where $I_F < 1.1\ I_{FI(Max)}$ is guaranteed.
3. Minimum V_F required to insure $I_F > 0.9\ I_{FI(Min)}$.

NCL

Current-Limiter Diode
V-I Characteristic



Siliconix

n-channel JFETs current regulator diodes

designed for . . .

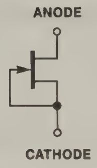
- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Linear Ramp and Staircase Generator**

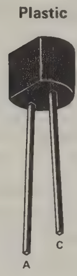
Performance Curves NKL, VRMA
See Section 4

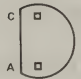
BENEFITS

- Low Cost
- Simple Two Lead Current Source
- Simplifies Floating Current Sources No Power Supplies Required

TO-92 (MODIFIED)
See Section 6







Bottom View

ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage	100V
Forward Current	20 mA
Reverse Current	50 mA
Total Device Dissipation (25°C Free Air Temperature)	350 mW
Power Derating (to +125°C)	3.27 mW/°C
Storage Temperature Range	−55 to 135°C
Operating Temperature Range	−55 to 135°C
Lead Temperature Range (1/16″ from case for 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic				Min	Typical	Max	Unit	Test Conditions
1	STATIC	I_{F1}	Forward Current (Note 1)			770	μA	$V_F = 100$ V
2				250		700		$V_F = 25$ V
3				200		—		$V_F = 1.0$ V
4		POV	Peak Operating Voltage (Notes 1 and 2)	100			V	$I_F = 1{\bullet}d\ I_{FI}$ (Max)
5 6		V_L	Limiting Voltage (Note 3)		1.1	1.5		$I_F = 0.9\ I_{FI}$ (Min)
7 8	DYN	Z_{F1}	Small-Signal Dynamic Impedance (Note 1)	1.0	4.4		MΩ	$V_F = 25$ V, f = 1 kHz
9		C_F	Anode-Cathode Capacitance		2		pF	$V_F = 25$ V, f = 1 MHz

NKL, VRMA

NOTES:

1. Pulse test duration = 2 ms.
2. Maximum V_F where $I_F < 1.1\ I_{F1(Max)}$ is guaranteed.
3. Minimum V_F required to insure $I_F > 0.9\ I_{F1(Min)}$.

J553 J554 J555 J556 J557

current regulator diodes designed for . . .

Siliconix

- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Low Voltage References**

Performance Curves NCL
See Section 4

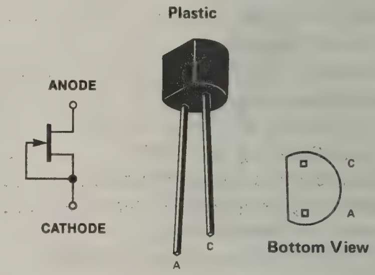
BENEFITS

- Simple Two Lead Current Source
- In Low Cost Plastic Package
- Simplifies Floating Current Sources No Power Supplies Required

ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage	50 V
Forward Current	20 mA
Reverse Current	50 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	−55 to 135°C
Storage Temperature Range	−55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C

TO-92 (MODIFIED)
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Regulator Current			Limiting Voltage		Peak op Volt	Dynamic Impedance	Knee Impedance
	V_F=25V			I_F=0.8 $I_{FI(min)}$ I_{FF} 1.1				
PART NUMBER	I_F NOM	I_F MIN	I_F MAX	V_L	V_L	V_{OP}	'ZD	'ZK
	Nominal mA	Min mA	Max mA	Max Volts	Typical	I_{FI} (Max) Min Volts	Typical Megohms	Typical Megohms
J553	0.5	0.18	0.75	1.3	0.75	50	10	2
J554	1.0	0.6	1.6	1.75	0.55	50	1	1
J555	2.0	1.4	2.6	2.15	0.75	50	.88	0.25
J556	3.0	2.4	3.8	2.6	0.75	50	.6	0.14
J557	4.5	3.6	5.3	3.0	1.5	50	.48	0.09

NOTES:

1. Pulse test—steady state currents may vary.
2. Pulse test—steady state impedance may vary.
3. Min V_F required to insure I_F>0.8 I_{F1} (min).
4. Max V_F where $I_F < 1.1$ $I_{F1(max)}$ is guaranteed.

NCL

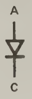
low-leakage pico-amp diodes *designed for . . .*

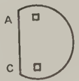
- **High Impedance Diode Switching**
- **High Dynamic Range Log Amps**
- **High Isolation Protection Circuits**

BENEFITS

- Low Cost

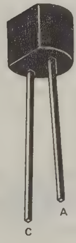
TO-92 (MODIFIED)
See Section 6





Bottom View

Plastic



ABSOLUTE MAXIMUM RATINGS (25°C)

Forward Current . . . . 10 mA
Total Device Dissipation . . . . 360 mW
Storage Temperature Range. . . . . –65°C to +135°C
Lead Temperature
(1/16″ from case for 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C)

			Characteristic		Min	Typ	Max	Unit	Test Conditions
1	STATIC	I_R	Reverse Current (Note 1)	JPAD5			–5	pA	$V_R = -20$ V
				JPAD10			–10		
				JPAD20			–20		
				JPAD50			–50		
				JPAD100			–100		
				JPAD200			–200		
				JPAD500			–500		
2		BV_R	Breakdown Voltage (Reverse)		–35	–80		V	$I_R = -1\ \mu A$
3		V_F	Forward Voltage Drop			0.8	1.5	V	$I_F = 5$ mA
4	DYN	C_R	Capacitance			1.5	2.0	pF	$V_R = -5$ V, f = 1 MHz

NOTE:
1. The JPAD type number denotes its maximum reverse current value in pico amps. Devices with I_R values intermediate to those shown are also available on request.

Siliconix

high voltage protection diode

designed for. . .

- **High Impedance Diode Switching**
- **High Dynamic Range Log Amps**
- **High Isolation Protection Circuits**

Performance Curves VRMA
See Section 4

BENEFITS

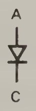
- Offers High Voltage Protection
- Broad Current Range

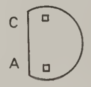
ABSOLUTE MAXIMUM RATINGS (25°C)

Anode to Cathode Voltage

JR135V	135 V
JR170V	170 V
JR200V	200 V
JR220V	220 V
JR240V	240 V
Forward Diode Current I_F	20 mA
Reverse Diode Current I_F	50 mA
Power Dissipation P_D (Derate 3.27 mW/°C)	360 mW
Storage Temperature T_{STG}	−55°C to 150°C
Operating Temperature T_{OP}	−55°C to 135°C

TO-92 (MODIFIED)
See Section 6





Bottom View

Plastic

ELECTRICAL CHARACTERISTICS (25°C)

		Characteristic		Min	Typ	Max	Unit	Test Conditions
1	P_{OV}	Peak Operating Voltage[1]	JR135V	135			V	$I_F = 1\,mA$
			JR170V	170				
			JR200V	200				
			JR220V	220				
			JR240V	240				
2	$I_F{}^1$	Forward Current		200			µA	$V_F = 2V$
	$I_F{}^2$			200		770		$V_F = 100V$
3	V_L	Limiting Current				0.9	V	$I = 0.8\,I_F{}^1$
4	Z_D	Dynamic Impedance			2		MΩ	$V_F = 25V$
5	$\Delta I_F/\Delta T$	I_F Temp Coefficient			+0.6		%/°C	$V_F = 2\text{–}100V$ $T_A = -20$ to $+85°C$

NOTE:
1. Pulse test duration 2 ms.

VRMA

enhancement-type n-channel MOSFET designed for . . .

Siliconix

- **General Purpose Amplifiers**
- **Analog Switches**
- **Digital Switching**

Performance Curves
MBN See Section 4

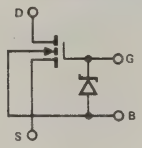
BENEFITS

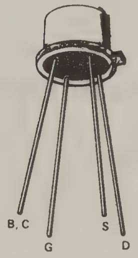
- Low Insertion Loss
  $R_{DS(on)}$ = 100 Ω Maximum
- Rugged
  Zener Diode Input Protection

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage	30 V
Gate-to-Source Voltage	30 V
Gate-to-Drain Voltage	30 V
Drain Current	50 mA
Gate Zener Current	±0.1 mA
Storage Temperature	-65 to 150°C
Operating Junction Temperature	−55 to +125°C
Total Device Dissipation (Derate 2.25 mW/°C to 125°C)	225 mW

TO-72
See Section 6





M116

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

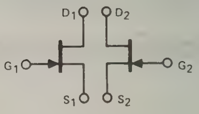
		Characteristic		M116 Min	M116 Max	Unit	Test Condition	
1	STATIC	I_{GSS}	Gate-Body Leakage		100	pA	V_{GS} = 20 V, V_{DS} = V_{BS} = 0	
2		$V_{GS(th)}$	Gate Threshold Voltage	1	5	V	V_{GS} = V_{DS}, I_D = 10 μA, V_{BS} = 0	
3		BV_{DSS}	Drain-Source Breakdown Voltage	30			I_D = 1 μA, V_{GS} = V_{BS} = 0	
4		BV_{SDS}	Source-Drain Breakdown Voltage	30			I_S = 1 μA, V_{GD} = V_{BD} = 0	
5		BV_{GBS}	Gate-Body Breakdown Voltage	30	60		I_G = 10 μA, V_{SB} = V_{DB} = 0	
6		$I_{D(off)}$	Drain Cutoff Current		10	nA	V_{DS} = 20 V, V_{GS} = V_{BS} = 0	
7		$I_{S(off)}$	Source Cutoff Current		10		V_{SD} = 20 V, V_{GD} = V_{BD} = 0	
8		$r_{DS(on)}$	Drain Source ON Resistance		100	Ω	V_{GS} = 20 V, I_D = 100 μA, V_{BS} = 0	
9					200		V_{GS} = 10 V, I_D = 100 μA, V_{BS} = 0	
10	DYN	C_{iss}	Input Capacitance		10	pF	V_{GB} = 0, V_{DB} = 10 V, V_{BS} = 0	f = 1 MHz
11		C_{gs}	Gate-Source Capacitance		2.5		V_{GB} = V_{DB} = 0 Body Guarded	
12		C_{gd}	Gate-Drain Capacitance		2.5			
13		C_{db}	Drain-Body Capacitance		7		V_{GB} = 0, V_{DB} = 10 V	

MBN

Siliconix

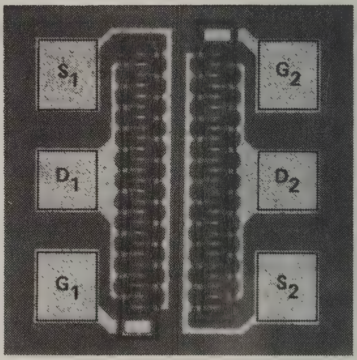
monolithic dual n-channel JFET Chips *designed for . . .*

- **Hybrid Circuits**
- **Wideband Differential Amplifiers**
- **VHF/UHF Amplifiers**



BENEFITS

- High Gain through 100 MHz
  $g_{fs} > 4500\ \mu$mho
- Low Insertion Loss
- Tight Tracking



ABSOLUTE MAXIMUM RATINGS (25° C)

Gate-Drain or Gate Source Voltage	–25 V
Gate Current	50 mA

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		M440CHP			M441CHP			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-500			-500	pA	$V_{DS} = 0$, $V_{GS} = -15$ V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1		-6	-1		-6	V	$V_{DS} = 10$ V, $I_D = 1$ nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25				$V_{DS} = 0$, $I_G = -1\ \mu$A	
4		I_{DSS}	Saturation Drain Current (Note 2)	6		30	6		30	mA	$V_{DS} = 10$ V, $V_{GS} = 0$	
5		I_G	Gate Current (Note 1)			-500			-500	pA	$V_{DG} = 10$ V, $I_D = 5$ mA	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4,500		9,000	4,500		9,000	μmho	$V_{DG} = 10$ V, $I_D = 5$ mA	f = 1 kHz
7		g_{os}	Common-Source Output Conductance			200			200			
8		C_{iss}	Common-Source Input Capacitance		5.0			5.0		pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			1.2				
10	MAT	$\lvert V_{GS1} - V_{GS2}\rvert$	Differential Gate-Source Voltage			10			20	mV	$V_{DG} = 10$ V, $I_D = 5$ mA	

NNZ

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μsec; duty cycle ⩽ 3%.

monolithic dual n-channel JFETs chips

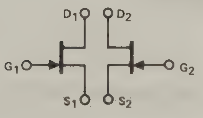
designed for . . .

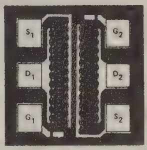
Siliconix

- **Hybrid Circuits**
- **Wideband Differential Amplifiers**
- **VHF/UHF Amplifiers**

BENEFITS

- High Gain through 100 MHz
  $g_{fs} > 5000\ \mu\text{mho}$
- Low Insertion Loss
- Tight Tracking





2

ABSOLUTE MAXIMUM RATINGS (25° C)

Gate-Drain or Gate Source Voltage .... –25 V
Gate Current .... 50 mA

*ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)

			Characteristic	Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -15 V, V_{DS} = 0	
2					-250	nA		T_A = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-5		V_{DS} = 10 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.3	-4		V_{DG} = 10 V, I_D = 5 mA	
6		I_G	Gate Operating Current		-100	pA		
					-100	nA		T_A = 125°C
7		I_{DSS}	Saturation Drain Current (Note 1)	7	40	mA	V_{DS} = 10 V, V_{GS} = 0 V	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	5000	10,000	µmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
9		g_{fs}	Common-Source Forward Transconductance	5000	10,000			f = 100 MHz
10		g_{os}	Common-Source Output Conductance		100			f = 1 kHz
11		g_{os}	Common-Source Output Conductance		150			f = 100 MHz
12		C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
14		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
15		NF	Spot Noise Figure		1	dB		f = 10 kHz R_G = 100K

			Characteristic	M5911CHP		M5912CHP		Unit	Test Conditions	
				Min	Max	Min	Max			
16	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		20		20	nA	V_{DG} = 10 V, I_D = 5 mA	T_A = 125°C
17		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	–	V_{DS} = 10 V, V_{GS} = 0	
18		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		10		15	mV	V_{DG} = 10 V, I_D = 5 mA	
19		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3) (Guarantee-no test)		20		40	µV/°C		T_A = 25°C T_B = 125°C
20					20		40			T_A = -55°C T_B = 25°C
21		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 2)	0.95	1	0.95	1	–		f = 1 kHz

NNZ

*JEDEC registered data.

NOTES:
1. Pulsewidth ⩽ 300 µs, duty cycle ⩽ 3%.
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.

enhancement-type p-channel MOSFET designed for . . .

Siliconix

Performance Curves MRA
See Section 4

- **High-Input Impedance Amplifiers**

  Smoke Detectors
  Electrometers
  pH Meters

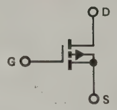
BENEFITS

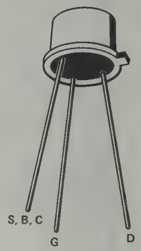
- High Input Impedance
  I_{GSS} = 30 Femto Amp Typical
- High Gain
  g_{fs} = 1000 μmho Minimum

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Voltage	25 V
Gate-Source Voltage	±10 V
Drain Current	30 mA
Total Device Dissipation at (Or Below) T_A = 25°C (Derate 3 mW/°C to +150°C)	375 mW
Operating Junction Temperature	–55 to +150°C
Storage Temperature	–65 to +200°C
Lead Temperature (1/16″ from case for 10 seconds)	265°C

TO-18
See Section 6





ELECTRICAL CHARACTERISTICS (25°C)

		Characteristic		Min	Max	Unit	Test Conditions
1	STATIC	I_{GSS}	Gate-Source Leakage Current		–1.0	pA	V_{GS} = –10 V, V_{DS} = 0
2		BV_{DSS}	Drain-Source Breakdown Voltage	–25		V	I_D = –10 μA, V_{GS} = 0
3		V_{GS}	Gate-Source Voltage	–2.0	–6.0	V	V_{DS} = –10 V, I_D = –10 μA
4		I_{DSS}	Drain Cutoff Current		–20	nA	V_{DS} = –10 V, V_{GS} = 0
5		$I_{D(on)}$	ON Drain Current	–3.0		mA	V_{DS} = –10 V, V_{GS} = –10 V
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000		μmhos	V_{DS} = –10 V, I_D = –2 mA, f = 1 kHz
7		C_{iss}	Common-Source Input Capacitance		6.0	pF	V_{DS} = –10 V, V_{GS} = –10 V, f = 1 MHz
8		C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		

MRA

Siliconix

n-channel JFET *designed for . . .*

- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

Performance Curves NH
See Section 4

BENEFITS

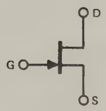
- Low Cost
- Automatic Insertion Package

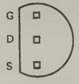
ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . .25 V
Source-Gate Voltage . . . . .25 V
Drain-Source Voltage. . . . . .25 V
Forward Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . .360 mW
Operating Temperature Range. . . . .–55 to 135°C
Storage Temperature Range. . . . .–55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . .300°C

TO-92
See Section 6

Plastic





Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–2.0	nA	V_{GS} = –15 V, V_{DS} = 0	
2					–2.0	μA		T_A = +100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25		V	I_G = –10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		–8.0		V_{DS} = 15 V, I_D = 2 nA	
5		I_{DSS}	Saturation Drain Current	2.0	20	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6		V_{GS}	Gate-Source Voltage	–0.5	–7.5	V	V_{DS} = 15 V, I_D = 200 μA	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2000	7500	μmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		$Re(y_{fs})$	Common-Source Forward Transconductance	1600				f = 100 MHz
9		$Re(y_{os})$	Common-Source Output Conductance		200			
10		$Re(y_{is})$	Common-Source Input Conductance		800			
11		C_{iss}	Common-Source Input Capacitance		7.0	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		3.0			

NOTE:
1. Pulse test PW = 300 μs; duty cycle ⩽ 3%.

NH

n-channel JFET
designed for . . .

Siliconix

- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

Performance Curves NH
See Section 4

BENEFITS

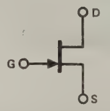
- Low Cost
- Automatic Insertion Package

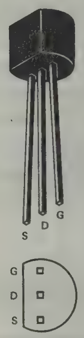
ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . .25 V
Source-Gate Voltage . . . . .25 V
Drain-Source Voltage. . . . . .25 V
Forward Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . .300°C

TO-92
See Section 6

Plastic





Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–1.0	nA	V_{GS} = –15 V, V_{DS} = 0	
2					–1.0	μA		T_A = +100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25		V	I_G = –10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.5	–8.0		V_{DS} = 15 V, I_D = 10 μA	
5		I_{DSS}	Saturation Drain Current	1.5	24	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2000	7500	μmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		75			
8		$Re(y_{fs})$	Common-Source Forward Transconductance	1600				f = 100 MHz
9		$Re(y_{os})$	Common-Source Output Conductance		200			
10		$Re(y_{is})$	Common-Source Input Conductance		800			
11		C_{iss}	Common-Source Input Capacitance		6.5	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		2.5			
13		NF	Noise Figure		2.5	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1M Ω	f = 1 kHz
14					3.0		V_{DS} = 15 V, V_{GS} = 0, R_G = 1K Ω	f = 100 MHz

NOTE:
1. Pulse test, pulse width = 300 μs, duty cycle ⩽ 3%.

NH

n-channel JFET designed for . . .

■ General Purpose Amplifiers

■ Analog Switches

Siliconix

Performance Curves NRL, NPA
See Section 4

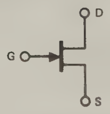
BENEFITS

- Low Cost
- Automatic Insertion Package

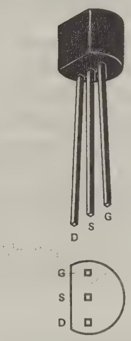
ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	25 V
Source-Gate Voltage	25 V
Drain-Source Voltage	25 V
Forward Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	–55 to 135°C
Storage Temperature Range	–55 to 150°C
Lead Temperature Range (1/16″ from case for 10 seconds)	300°C

TO-92
See Section 6



Plastic



Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–0.01	–1.0	nA	V_{GS} = –15 V, V_{DS} = 0	
2		BV_{GSS}	Gate-Source Breakdown Voltage	–25	–60		V	I_G = –10 μA, V_{DS} = 0	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.2		–8.0		V_{DS} = 15 V, I_D = 10 μA	
4		I_{DSS}	Saturation Drain Current	0.5		24	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
5	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	800		6000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
6		g_{os}	Common-Source Output Conductance		10	75			
7		C_{iss}	Common-Source Input Capacitance		4.5	7.0	pF		f = 1 MHz
8		C_{rss}	Common-Source Reverse Transfer Capacitance		1.0	3.0			
9		NF	Noise Figure		0.04	2.5	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1M Ω	f = 1 kHz

NRL, NPA

NOTE:
1. Pulse test PW ≤ 630 ms, duty cycle ≤ 10%.

Siliconix

n-channel JFET *designed for . . .*

- **General Purpose Amplifiers**
- **Analog Switches**

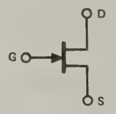
Performance Curves NRL, NPA
See Section 4

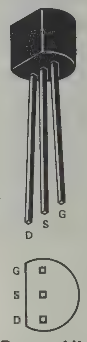
BENEFITS

- Low Cost
- Automatic Insertion Package

TO-92
See Section 6

Plastic





Bottom View

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	20V
Source-Gate Voltage	20V
Drain-Source Voltage	20V
Forward Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	–55 to 135°C
Storage Temperature Range	–55 to 150°C
Lead Temperature Range (1/16″ from case for 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate-Reverse Current		–.01	–100	nA	V_{GS} = –10 V, V_{DS} = 0	
2		BV_{GSS}	Gate-Source Breakdown Voltage	–20			V	I_G = –10 μA, V_{DS} = 0	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.5		–10.0		V_{DS} = 10 V, I_D = 1 μA	
4		I_{DSS}	Saturation Drain Current	0.5		20	mA	V_{DS} = 10 V, V_{GS} = 0 (Note 1)	
5	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	500			μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
6		g_{os}	Common-Source Output Conductance		10				
7		C_{iss}	Common-Source Input Capacitance		4.5		pF		f = 1 MHz
8		C_{rss}	Common-Source Reverse Transfer Capacitance		1.0				

NRL, NPA

NOTE:
1. Pulse test PW ⩽ 630 msec, duty cycle ⩽ 10%.

n-channel JFET *designed for . . .*

Siliconix

- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

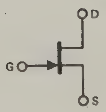
Performance Curves NH
See Section 4

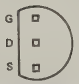
BENEFITS

- Low Cost
- Automatic Insertion Package

TO-92
See Section 6

Plastic





Bottom View

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	25 V
Source-Gate Voltage	25 V
Drain-Source Voltage	25 V
Forward Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	−55 to 135°C
Storage Temperature Range	−55 to 150°C
Lead Temperature Range (1/16″ from case for 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		−0.01	−100	nA	$V_{GS} = -10$ V, $V_{DS} = 0$	
2		BV_{GSS}	Gate-Source Breakdown Voltage	−25			V	$I_G = -10\ \mu$A, $V_{DS} = 0$	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5		−10.0		$V_{DS} = 10$ V, $I_D = 1\ \mu$A	
4		I_{DSS}	Saturation Drain Current	1		25	mA	$V_{DS} = 10$ V, $V_{GS} = 0$, (Note 1)	
5		g_{fs}	Common-Source Forward Transconductance	1000		7500	μmho	$V_{DS} = 10$ V, $V_{GS} = 0$	f = 1 kHz
6	DYN	$Re(y_{fs})$	Common-Source Forward Transconductance	800					f = 100 MHz
7		C_{iss}	Common-Source Input Capacitance		3.5		pF		f = 1 MHz
8		C_{rss}	Common-Source Reverse Transfer Capacitance		0.85				

NH

NOTE:
1. Pulse test PW = 300 μs, duty cycle ⩽ 3%.

p-channel JFETs *designed for . . .*

Siliconix

Performance Curves PSA
See Section 4

- **Analog Switches**
- **Choppers**
- **Commutators**

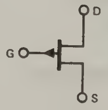
BENEFITS

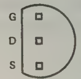
- Low Insertion Loss
  $r_{DS(on)}$ = 75 Ω Maximum (P1086)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) 30V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . −55 to 135°C
Storage Temperature Range . . . . −55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . 300°C

TO-92
See Section 6





Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		P1086		P1087		Unit	Test Conditions	
				Min	Max	Min	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30		30		V	$I_G = 1\ \mu A$, $V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current		2		2	nA	$V_{GS} = 15$ V, $V_{DS} = 0$	
3		$I_{D(off)}$	Drain Cutoff Current		−10		−10		$V_{DS} = -15$ V, $V_{GS} = 12$ V (P1086) $V_{GS} = 7$ V (P1087)	
4					−0.5		−0.5	μA		$T_A = 85°C$
5		I_{DGO}	Drain Reverse Current		2		2	nA	$V_{DG} = -15$ V, $I_S = 0$	
					0.1		0.1	μA		$T_A = 85°C$
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage		10		5	V	$V_{DS} = -15$ V, $I_D = -1\ \mu A$	
7		I_{DSS}	Saturation Drain Current	−10		−5		mA	$V_{DS} = -20$ V, $V_{GS} = 0$	
8		$V_{DS(on)}$	Drain-Source ON Voltage		−0.5		−0.5	V	$V_{GS} = 0$, $I_D = -6$ mA (P1086), $I_D = -3$ mA (P1087)	
9		$r_{DS(on)}$	Static Drain-Source ON Resistance		75		150	Ω	$I_D = -1$ mA, $V_{GS} = 0$	
10	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		75		150	Ω	$I_D = 0$, $V_{GS} = 0$	f = 1 kHz
11		C_{iss}	Common-Source Input Capacitance		45		45	pF	$V_{DS} = -15$ V, $V_{GS} = 0$	f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		10		10		$V_{DS} = 0$, $V_{GS} = 12$ V (P1086) $V_{GS} = 7$ V (P1087)	
13	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	$V_{DD} = -6$ V, $V_{GS(on)} = 0$	
14		t_r	Rise Time		20		75		$V_{GS(off)}$ $I_{D(on)}$ R_L	
15		$t_{d(off)}$	Turn-OFF Delay Time		15		25		P1086 12 V −6 mA 910 Ω	
16		t_f	Fall Time		50		100		P1087 7 V −3 mA 1.8K Ω	

NOTE:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

PSA

PAD1 PAD2 PAD5 PAD10 PAD20 PAD50 PAD100
PLASTIC EQUIVALENT JPAD5 SERIES

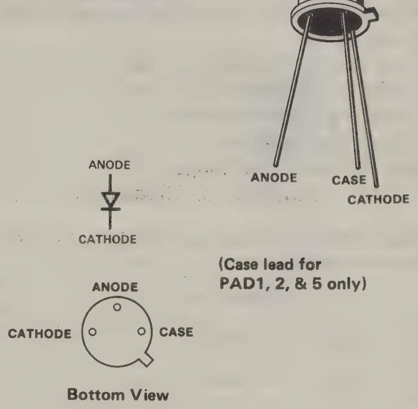
low-leakage pico-amp diodes *designed for . . .*

- **Clipping Circuits**
- **Diode Switching**
- **High Impedance Protection Circuits**

BENEFITS

- Very High Off-Isolation
  1 pA Max (PAD1)

TO-18 (MODIFIED)
See Section 6



(Case lead for PAD1, 2, & 5 only)

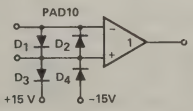
Bottom View

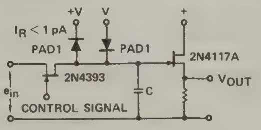
ABSOLUTE MAXIMUM RATINGS (25°C)

Forward Current	50 mA
Total Device Dissipation	300 mW
Storage Temperature Range	−55°C to +125°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_R	Reverse Current			-1	pA	$V_R = -20$ V	PAD1
2						-2			2
3						-5			5
4						-10			PAD10
5						-20			20
6						-50			50
7						-100			PAD100
8		BV_R	Breakdown Voltage (Reverse)	-45		-120	V	$I_R = -1\ \mu A$	PAD1, 2, 5
9				-35					PAD10, 20, 50, 100
10		V_F	Forward Voltage Drop		0.8	1.5		$I_F = 5$ mA	PAD1, 2, 5, 10, 20, 50, 100
11	DYN	C_R	Capacitance			0.8	pF	$V_R = -5$ V, f = 1 MHz	PAD1, 2, 5
12						2			PAD10, 20, 50, 100





APPLICATION

Operational Amplifier Protection. Input Differential Voltage limited to 0.8 V (typ) by PADS D_1 and D_2 Common mode input voltage limited by PADS D_3 and D_4 to ±15 V.

Typical sample and hold circuit with clipping. PAD diodes reduce offset voltages fed capacitively from the FET switch gate.

n-channel JFETs *designed for . . .*

Siliconix

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Performance Curves NCA
See Section 4

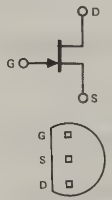
BENEFITS

- Low Insertion Loss
  High Accuracy in Test Systems
  $r_{DS(on)} < 30\ \Omega$ (PN4091)
- High Off-Isolation
  $I_{D(off)} < 200$ pA
- High Speed
  $t_{rise} < 10$ ns (PN4091)
- Short Sample and Hold Aperture Time
  $C_{rss} < 5$ pF

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	–55 to 135°C
Storage Temperature Range	–55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C

TO-92
See Section 6



Bottom View

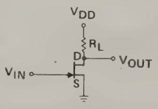
Plastic

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	PN4091		PN4092		PN4093		Unit	Test Conditions		
				Min	Max	Min	Max	Min	Max				
1	S T A T I C	BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$		
2		I_{DGO}	Drain Reverse Current		200		200		200	pA	$V_{GS} = -20$ V, $I_S = 0$		
3					400		400		400	nA			150°C
4		$I_{D(off)}$	Drain Cutoff Current						200	pA	$V_{DS} = 20$ V	$V_{GS} = -6$ V	
5									400	nA			150°C
6							200			pA		$V_{GS} = -8$ V	
7							400			nA			150°C
8					200					pA		$V_{GS} = -12$ V	
9					400					nA			150°C
10		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-5	-10	-2	-7	-1	-5	V	$V_{DS} = 20$ V, $I_D = 1$ nA		
11		I_{DSS}	Saturation Drain Current (Note 1)	30		15		8		mA	$V_{DS} = 20$ V, $V_{GS} = 0$		
12		$V_{DS(on)}$	Drain-Source ON Voltage						0.2	V	$V_{GS} = 0$	$I_D = 2.5$ mA	
13							0.2					$I_D = 4$ mA	
14					0.2							$I_D = 6.6$ mA	
15		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		50		80	Ω	$V_{GS} = 0$, $I_D = 1$ mA		
16	D Y N	$r_{ds(on)}$	Drain-Source ON Resistance		30		50		80	Ω	$V_{GS} = 0$, $I_D = 0$		f = 1 kHz
17		C_{iss}	Common-Source Input Capacitance		16		16		16	pF	$V_{DS} = 20$ V, $V_{GS} = 0$		f = 1 MHz
18		C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5		$V_{DS} = 0$, $V_{GS} = -20$ V		
19	S W	$t_{d(on)}$	Turn-ON Delay Time		15		15		20	ns	$V_{DD} = 3$ V, $V_{GS(on)} = 0$		
20		t_r	Rise Time		10		20		40		$I_{D(on)}$ $V_{GS(off)}$ R_L PN4091 6.6 mA -12 V 425 Ω PN4092 4 -8 700 PN4093 2.5 -6 1120		
21		t_{off}	Turn-OFF Time		40		60		80				

NCA

NOTE:
1. Pulsewidth = 300 μs, duty cycle ⩽ 3%.



INPUT PULSE
RISE TIME < 1 ns
FALL TIME < 1 ns
PULSE WIDTH 1 μs
PULSE DUTY CYCLE ⩽ 10%
PULSE GENERATOR IMPEDANCE 50Ω

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.7 pF

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NT
See Section 4

- **Ultra-High Input Impedance Amplifiers**

Electrometers
pH Meters
Smoke Detectors

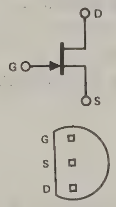
BENEFITS

- Low Power
  $I_{DSS} < 90\ \mu A$ (PN4117)
- Minimum Circuit Loading
  $I_{GSS} < 1$ pA (PN4117A Series)

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . -40 V
Gate Current . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . 300°C

TO-92
See Section 6



Bottom View

Plastic

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		PN4117 PN4117A			PN4118 PN4118A			PN4119 PN4119A			PN4120 PN4120A			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current PN4117 Series Only			-10			-10			-10			-20	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
2						-25			-25			-25			-50	nA		100°C
3		I_{GSS}	Gate Reverse Current PN4117A Series Only		-1			-1			-1			-5		pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
4						-2.5			-2.5			-2.5			-10	nA		100°C
5		BV_{GSS}	Gate-Source Breakdown Voltage	-40			-40			-40					-40	V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.6		-1.8	-1		-3	-2		-6	-0.6		3		$V_{DS} = 10$ V, $I_D = 1$ nA	
7		I_{DSS}	Saturation Drain Current (Note 2)	0.03		0.09	0.08		0.24	0.20		0.60	0.03		0.3	mA	$V_{DS} = 10$ V, $V_{GS} = 0$	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	70		210	80		250	100		330	70		300	μmho	$V_{DS} = 10$ V, $V_{GS} = 0$	f = 1 kHz
9		g_{os}	Common-Source Output Conductance			3			5			10			20			
10		C_{iss}	Common-Source Input Capacitance			3			3			3			3	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance			1.5			1.5			1.5			1.5			

NT

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. This parameter is measured during a 2 ms interval 100 ms after power is applied.

n-channel JFETs designed for . . .

Siliconix

Performance Curves NPA, NH
See Section 4

■ General Purpose Amplifiers

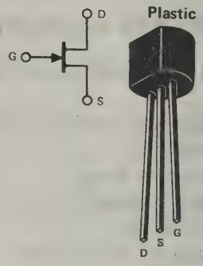
BENEFITS

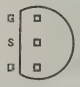
- Low Cost
- High Input Impedance
  I_G = 35 pA Typically
- Low Noise
  $\overline{e}_n$ = 5 nV/$\sqrt{Hz}$ Typically @ 1 kHz

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . –30V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Ambient.
  (Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
  (1/16″ from case for 10 seconds) . . . . 300°C

TO-92
See Section 6





Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		PN4302 Min	PN4302 Max	PN4303 Min	PN4303 Max	PN4304 Min	PN4304 Max	Unit	Test Conditons	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)		1		–1		–1	nA	V_{GS} = –10 V, V_{DS} = 0	
2					0.1		–0.1		–0.1	µA		T_A = 85°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–30		–30		–30		V	I_G = –1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		–4.0		–6.0		–10		V_{DS} = 20 V, I_D = 10 nA	
5		I_{DSS}	Saturation Drain Current (Note 3)	0.5	5.0	4.0	10	0.5	15	mA	V_{DS} = 20 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	1000		2000		1000		µmho		f = 1 kHz
7		g_{os}	Common-Source Output Conductance		50		50		50			
8		C_{rss}	Common-Source Reverse Transfer Capacitance		3		3		3	pF		f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		6		6		6			
10		C_{DG}	Drain-Gate Capacitance		2		2		2		V_{DG} = 10 V, I_S = 0	f = 140 kHz
11		NF	Noise Figure		2.0		2.0		3.0	dB	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz, R_{gen} = 1.0M Ω
12		$\lvert y_{fs}\rvert$	Common-Source Short Circuit Forward Transadmittance (Note 3)	700		1400		700		µmho	V_{DS} = 20 V, V_{GS} = 0	f = 10 MHz

NPA, NH

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

n-channel JFETs designed for . . .

PN4391 PN4392 PN4393

Siliconix

- **Analog Switches**
- **Commutators**
- **Choppers**

Performance Curves NCA
See Section 4

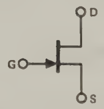
BENEFITS

- Low Insertion Loss
- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- Low Cost

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage	−40 V
Forward Gate Current	50 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	−55 to 135°C
Storage Temperature Range	−55 to 150°C
Lead Temperature Range (1/16″ from case for 10 seconds)	300°C

TO-92
See Section 6



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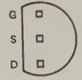


Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	PN4391		PN4392		PN4393		Unit	Test Conditions		
				Min	Max	Min	Max	Min	Max				
1	STATIC	I_{GSS}	Gate Reverse Current		−1.0		−1.0		−1.0	nA	V_{GS} = −20 V, V_{DS} = 0		
2					−200		−200		−200				100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		−40		V	I_G = −1 μA, V_{DS} = 0		
4		$I_{D(off)}$	Drain Cutoff Current						1.0	nA	V_{DS} = 20 V	V_{GS} = −5 V	
5									200				100°C
6							1.0					V_{GS} = −7 V	
7							200						100°C
8					1.0							V_{GS} = −12 V	
9					200								100°C
10		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−4	−10	−2	−5	−0.5	−3	V	V_{DS} = 20 V, I_D = 1 nA		
11		I_{DSS}	Saturation Drain Current (Note 1)	50	150	25	100	5	60	mA	V_{DS} = 20 V, V_{GS} = 0		
12		$V_{DS(on)}$	Drain-Source ON Voltage						0.4	V	V_{GS} = 0	I_D = 3 mA	
13							0.4					I_D = 6 mA	
14					0.4							I_D = 12 mA	
15		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 1 mA		
16		$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, V_{DS} = 0		f = 1 kHz
17	DYN	C_{iss}	Common-Source Input Capacitance		16		16		16	pF	V_{DS} = 20 V, V_{GS} = 0		f = 1 MHz
18		C_{rss}	Common-Source Reverse Transfer Capacitance						5		V_{DS} = 0	V_{GS} = −5 V	
19							5					V_{GS} = −7V	
20					5							V_{GS} = −12 V	
21		$t_{d(on)}$	Turn-ON Delay Time		15		15		15	ns	V_{DD} = 10 V, $V_{GS(on)}$ = 0 $I_{D(on)}$ $V_{GS(off)}$ R_L PN4391 12 mA −12 V 800 Ω PN4392 6 −7 1.6K PN4393 3 −5 3.2K		
22	SW	t_r	Rise Time		5		5		5				
23		$t_{d(off)}$	Turn-OFF Delay Time		20		35		50				
24		t_f	Fall Time		15		20		30				

NCA

NOTE:
1. Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%.

n-channel JFETs
designed for . . .

Siliconix

- **VHF Amplifiers**
- **Mixers**

Performance Curves NH
See Section 4

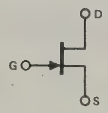
BENEFITS

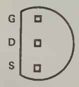
- Low Noise
  NF = 3 dB Typical at 400 MHz
- Wide Band
  High g_{fs}/C_{iss} Ratio

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . –30V
Gate Current . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . –55 to 135°C
Storage Temperature Range . . . . –55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . 300°C

TO-92
See Section 6





Bottom View

Plastic

			Characteristic	Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		1.0	nA	V_{GS} = –15 V, V_{DS} = 0 V	
2								
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		V	I_G = –1 μA, V_{DS} = 0 V	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-6		V_{DS} = 15 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	5	15	mA	V_{DS} = 15 V, V_{GS} = 0 V	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4500	7500	μmho		f = 1 kHz
7		g_{os}	Common-Source Output Conductance		50			
8		C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	pF		f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		4			
10		C_{oss}	Common-Source Output Capacitance		2			

			Characteristic	100 MHz		400 MHz		Unit	Test Conditions
				Min	Max	Min	Max		
11	HIGH FREQUENCY	g_{iss}	Common-Source Input Conductance		100		1000	μmho	V_{DS} = 15 V, V_{GS} = 0 V
12		b_{iss}	Common-Source Input Susceptance		2500		10,000		
13		g_{oss}	Common-Source Output Conductance		75		100		
14		b_{oss}	Common-Source Output Susceptance		1000		4000		
15		g_{fs}	Common-Source Forward Transconductance			4000			
16		G_{ps}	Common-Source Power Gain	18		10		dB	V_{DS} = 15 V, I_D = 5 mA
17		NF	Noise Figure		2		4		V_{DS} = 15 V, I_D = 5 mA, R_G = 1K Ω

NH

NOTES:
1. Pulse test duration = 300 μs.

n-channel JFET *designed for . . .*

Siliconix

■ Low and Medium Frequency Amplifiers

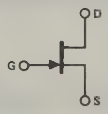
BENEFITS

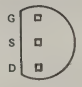
- Low Cost

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . –25V
Gate Current (FWD) . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . 300°C

TO-92
See Section 6





Bottom View

Plastic

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions		
1	STATIC	I_{GSS}	Gate Reverse Current		–10	nA	V_{GS} = –15 V, V_{DS} = 0		
2					–0.6	μA			T_A = 85°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25		V	I_G = –10 μA, V_{DS} = 0		
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.4	–8.0		V_{DS} = 15 V, I_D = 1 μA		
5		V_{GS}	Gate-Source Voltage		–7.5		V_{DS} = 15 V, I_D = 100 μA		
6		I_{DSS}	Saturation Drain Current	1.0	40	mA	V_{DS} = 15 V, V_{GS} = 0		
7	DYNAMIC	$r_{ds(on)}$	Drain-Source ON Resistance		500	Ω	V_{GS} = 0, I_D = 0		f = 1 kHz
8		g_{fs}	Common-Source Forward Transconductance	2000	9000	μmho	V_{DS} = 15 V, V_{GS} = 0		
9		g_{os}	Common-Source Output Conductance		200				
10		g_{fs}	Common-Source Forward Transconductance	1800					f = 1 MHz
11		C_{iss}	Common-Source Input Capacitance		20	pF			
12		C_{rss}	Common-Source Reverse Transfer Capacitance		5.0				
13		NF	Common-Source Spot Noise Figure		3.0	dB	V_{DS} = 15 V, I_D = 1 mA	R_G = 150k Ω	f = 1 kHz NBW = 150 Hz
14		$\overline{e}_N$	Equivalent Short Circuit Input Noise Voltage		50	$\frac{nV}{\sqrt{Hz}}$			

*JEDEC registered data

n-channel DMOS FETs

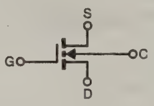
Designed for Military and Industrial Applications . . .

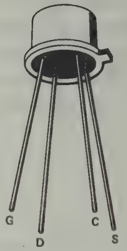
- **High-Speed Switching**
- **Analog Switch**
- **Multiplexer**
- **Digital Switch**
- **A to D Converters**
- **D to A Converters**
- **Choppers**
- **Sample and Hold**

BENEFITS

- Ultra low feedback capacitance (0.30pF)
- High switching speeds (<1ns)
- Gate can accept ±40V

TO-72
See Section 6





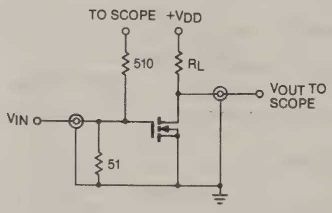
ABSOLUTE MAXIMUM RATINGS (°C)

Drain Current 50mA
Total Device Dissipation at 25°C
Case Temperature 1.2W
Storage Temperature Range . . . . −65° to +200°C
Lead Temperature (1/16″ from case for 10 sec.) . . . . . . 300°C
Operating Temperature Range . . . . −55° to +150°C

PARAMETER		SD210	SD212	SD214	UNIT
V_{DS}	Drain-to-source	+30	+10	+20	Vdc
V_{SD}	Source-to-drain*	+10	+10	+20	Vdc
V_{DB}	Drain-to-substrate	+30	+15	+25	Vdc
V_{SB}	Source-to-substrate	+15	+15	+25	Vdc
V_{GS}	Gate-to-source	±40	±40	±40	Vdc
V_{GB}	Gate-to-substrate	±40	±40	±40	Vdc
V_{GD}	Gate-to-drain	±40	±40	±40	Vdc

TEST CONDITIONS

Switching

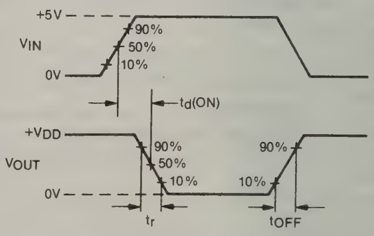


Input pulse: t_d, $t_r < 1$ns
Pulse width = 100ns
Rep rate = 1MHz

SAMPLING SCOPE

$t_r < 360$ps
$R_{IN} = 1M\Omega$
$C_{IN} = 2.0$pF

Typical Switching Waveform



SWITCHING CHARACTERISTICS

		t_d(ON) (ns)		t_r(ns)		t_{OFF}(ns)	
V_{DD}	R_L	Typ	Max	Typ	Max	Typ	Max
5	680	0.6	1.0	0.7	1.0	9.0	*
10	680	0.7		0.8		9.0	*
15	1k	0.9		1.0		14.0	*

*t_{OFF} is dependent on R_L and C_L and does not depend on the device characteristics.

DC ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified.)

		PARAMETER		TEST CONDITIONS	SD210			SD212			SD214			UNIT
					Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	S T A T I C	**Breakdown voltage**												V
1		BV_{DS}	Drain-to-source	$V_{GS} = V_{BS} = 0V$, $I_D = 10\mu A$	30	35								
				$V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	10	25		10	25		20	25		
2		BV_{SD}	Source-to-drain	$V_{GD} = V_{BD} = -5V$ $I_D = 10nA$	10			10			20			
3		BV_{DB}	Drain-to-substrate	$V_{GB} = 0V$, source OPEN $I_D = 10nA$	15			15			25			
4		BV_{SB}	Source-to-substrate	$V_{GB} = 0V$, drain OPEN $I_S = 10\mu A$	15			15			25			
		Leakage current												nA
5		I_{DS} (OFF)	Drain-to-source	$V_{GS} = V_{BS} = -5V$										
				$V_{DS} = +10V$		1	10		1	10				
				$V_{DS} = +20V$								1	10	
6		I_{SD} (OFF)	Source-to-drain	$V_{GD} = V_{BD} = -5V$										
				$V_{SD} = +10V$		1	10		1	10				
				$V_{SD} = +20V$								1	10	
7		I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$ $V_{GB} = \pm 40V$			0.1			0.1			0.1	
8		V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$ $V_{SB} = 0V$	0.5	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
9		r_{DS} (ON)	Drain-to-source resistance	$I_D = 1.0mA$, $V_{SB} = 0$										Ω
				$V_{GS} = +5V$		50	70		50	70		50	70	
				$V_{GS} = +10V$		30	45		30	45		30	45	
				$V_{GS} = +15V$		23			23			23		
				$V_{GS} = +20V$		19			19			19		
				$V_{GS} = +25V$		17			17			17		

AC ELECTRICAL CHARACTERISTICS

		PARAMETER		TEST CONDITIONS	SD210			SD212			SD214			UNIT
					Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
10	D Y N A M I C	gfs	Forward trans-conductance	$V_{DS} = 10V$, $V_{SB} = 0V$ $I_D = 20mA$, $f = 1kHz$	10	15		10	15		10	15		mmhos
		Small Signal Capacitances (See capacitance model)		$V_{DS} = 10V$, $f = 1MHz$ $V_{GS} = V_{BS} = -15V$										pF
11		$C_{(GS+GD+GB)}$	Gate node			2.4	3.5		2.4	3.5		2.4	3.5	
12		$C_{(GD+DB)}$	Drain node			1.3	1.5		1.3	1.5		1.3	1.5	
13		$C_{(GS+SB)}$	Source node			3.5	4.0		3.5	4.0		3.5	4.0	
14		C_{DG}	Reverse transfer			0.3	0.5		0.3	0.5		0.3	0.5	

SD211DE SD213DE SD215DE

n-channel DMOS FETs

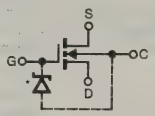
Designed for Military and Industrial Applications . . .

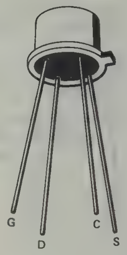
- **High-Speed Switching**
- **Analog Switch**
- **Multiplexer**
- **Digital Switch**
- **A to D Converters**
- **D to A Converters**
- **Choppers**
- **Sample and Hold**

BENEFITS

- Ultra low feedback capacitance (0.30pF)
- High switching speeds (<1ns)
- Diode protected gate

TO-72
See Section 6





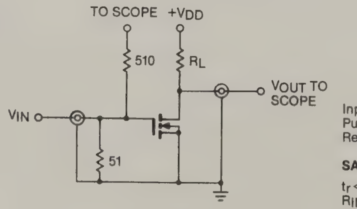
ABSOLUTE MAXIMUM RATINGS (°C)

Drain Current 50mA
Total Device Dissipation at 25°C
Case Temperature 1.2W
Storage Temperature Range . . . . −65° to +200°C
Lead Temperature (1/16″ from case for 10 sec.) . . . . . . 300°C
Operating Temperature Range . . . . −55° to +150°C

PARAMETER		SD211	SD213	SD215	UNIT
V_{DS}	Drain-to-source	+30	+10	+20	Vdc
V_{SD}	Source-to-drain*	+10	+10	+20	Vdc
V_{DB}	Drain-to-substrate	+30	+15	+25	Vdc
V_{SB}	Source-to-substrate	+15	+15	+25	Vdc
V_{GS}	Gate-to-source	−15 +25	−15 +25	−25 +30	Vdc
V_{GB}	Gate-to-substrate	−0.3 +25	−0.3 +25	−0.3 +30	Vdc
V_{GD}	Gate-to-drain	−30 +25	−15 +25	−25 +30	Vdc

TEST CONDITIONS

Switching

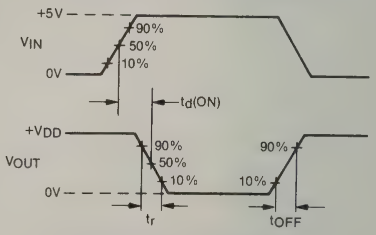


Input pulse: t_d, $t_r < 1$ns
Pulse width = 100ns
Rep rate = 1MHz

SAMPLING SCOPE

$t_r < 360$ps
$R_{IN} = 1M\Omega$
$C_{IN} = 2.0$pF

Typical Switching Waveform



SWITCHING CHARACTERISTICS

		t_d(ON) (ns)		t_r(ns)		t_{OFF}(ns)	
V_{DD}	R_L	Typ	Max	Typ	Max	Typ	Max
5	680	0.6	1.0	0.7	1.0	9.0	*
10	680	0.7		0.8		9.0	*
15	1k	0.9		1.0		14.0	*

*t_{OFF} is dependent on R_L and C_L and does not depend on the device characteristics.

DC ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified.)

		PARAMETER		TEST CONDITIONS	SD211			SD213			SD215			UNIT
					Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	STATIC	**Breakdown voltage**												
1		BV_{DS}	Drain-to-source	$V_{GS} = V_{BS} = 0V$, $I_D = 10\mu A$	30	35								V
				$V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	10	25		10	25		20	25		
2		BV_{SD}	Source-to-drain	$V_{GD} = V_{BD} = -5V$ $I_D = 10nA$	10			10			20			
3		BV_{DB}	Drain-to-substrate	$V_{GB} = 0V$, source OPEN $I_D = 10nA$	15			15			25			
4		BV_{SB}	Source-to-substrate	$V_{GB} = 0V$, drain OPEN $I_S = 10\mu A$	15			15			25			
		Leakage current												
5		I_{DS} (OFF)	Drain-to-source	$V_{GS} = V_{BS} = -5V$										nA
				$V_{DS} = +10V$		1	10		1	10				
				$V_{DS} = +20V$								1	10	
6		I_{SD} (OFF)	Source-to-drain	$V_{GD} = V_{BD} = -5V$										
				$V_{SD} = +10V$		1	10		1	10				
				$V_{SD} = +20V$								1	10	
7		I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$										μA
				$V_{GB} = +25V$			10			10				
				$V_{GB} = +30V$									10	
8		V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$ $V_{SB} = 0V$	0.5	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
9		r_{DS} (ON)	Drain-to-source resistance	$I_D = 1.0mA$, $V_{SB} = 0$										Ω
				$V_{GS} = +5V$		50	70		50	70		50	70	
				$V_{GS} = +10V$		30	45		30	45		30	45	
				$V_{GS} = +15V$		23			23			23		
				$V_{GS} = +20V$		19			19			19		
				$V_{GS} = +25V$								17		

AC ELECTRICAL CHARACTERISTICS

		PARAMETER		TEST CONDITIONS	SD211			SD213			SD215			UNIT
					Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
10	DYNAMIC	gfs	Forward trans-conductance	$V_{DS} = 10V$, $V_{SB} = 0V$ $I_D = 20mA$, $f = 1kHz$	10	15		10	15		10	15		mmhos
		Small Signal Capacitances (See capacitance model)		$V_{DS} = 10V$, $f = 1MHz$ $V_{GS} = V_{BS} = -15V$										pF
11		$C_{(GS+GD+GB)}$	Gate node			2.4	3.5		2.4	3.5		2.4	3.5	
12		$C_{(GD+DB)}$	Drain node			1.3	1.5		1.3	1.5		1.3	1.5	
13		$C_{(GS+SB)}$	Source node			3.5	4.0		3.5	4.0		3.5	4.0	
14		C_{DG}	Reverse transfer			0.3	0.5		0.3	0.5		0.3	0.5	

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**

Siliconix

Performance Curves NCA
See Section 4

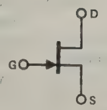
BENEFITS

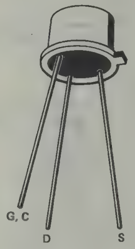
- Low Insertion Loss
  $r_{DS(on)} < 50\ \Omega$ (U202)
- Good Off-Isolation
  $I_{D(off)} < 1$ nA

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . -30 V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Derate 10 mW/°C) . . . . 1.8 W
Storage Temperature Range . . . . -65 to +200°C
Lead Temperature
(1/16″ from case for 10 seconds) . . . . 300°C

TO-18
See Section 6





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U200		U201		U202		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-1		-1		-1	nA	V_{GS} = -20 V, V_{DS} = 0	
2					-1		-1		-1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-3	-1.5	-5	-3.5	-10		V_{DS} = 20 V, I_D = 10 nA	
5		$I_{D(off)}$	Drain Cutoff Current		1		1		1	nA	V_{DS} = 10 V, V_{GS} = -12 V	
					1		1		1	μA		150°C
6		I_{DSS}	Saturation Drain Current (Note 1)	3	25	15	75	30	150	mA	V_{DS} = 20 V, V_{GS} = 0	
7	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		150		75		50	ohm	V_{GS} = 0, I_D = 0	f = 1 kHz
8		C_{iss}	Common-Source Input Capacitance (Note 1)		30		30		30	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		8		8		8		V_{DS} = 0, V_{GS} = -12 V	

NOTE:
1. Pulse test required, pulsewidth = 300 μsec, duty cycle ⩽ 3%.

NCA

Siliconix

monolithic dual n-channel JFETs *designed for . . .*

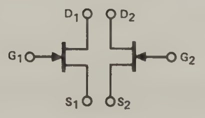
■ Differential Amplifiers

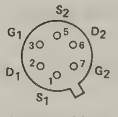
Performance Curves NQP
See Section 4

BENEFITS

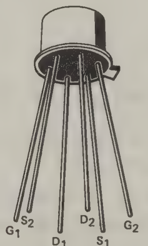
- Good Matching Characteristics

TO-71
See Section 6





Bottom View



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . -50 V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C
(Derate 1.7 mW/°C to 200°C) . . . . 300 mW
Storage Temperature Range . . . . -65 to +200°C
Lead Temperature
(1/16″ from case for 10 seconds) . . . . .300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-500	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-4.5		V_{DS} = 20 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.3	-4.0		V_{DG} = 20 V, I_D = 200 μA	
6		I_G	Gate Operating Current		-50	pA		
					-250	nA		125°C
7		I_{DSS}	Saturation Drain Current (Note 1)	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	5000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
				1000				f = 100 MHz
9		g_{fs}	Common-Source Forward Transconductance (Note 1)	600	1600		V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
10		g_{os}	Common-Source Output Conductance		35		V_{DS} = 20 V, V_{GS} = 0	
11		g_{os}	Common-Source Output Conductance		10		V_{DG} = 20 V, I_D = 200 μA	
12		C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		2			
14		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		80	$\frac{nV}{\sqrt{Hz}}$		f = 100 Hz

		Characteristic		U231 Max	U232 Max	U233 Max	U234 Max	U235 Max	Unit	Test Conditions	
15	MATCHING	$\|I_{G1}-I_{G2}\|$	Differential Gate Current	10	10	10	10	10	nA	V_{DG} = 20 V, I_D = 200 μA	125°C
16		$\frac{(I_{DSS1}-I_{DSS2})}{I_{DSS1}}$	Saturation Drain Current Match (Note 1)	5	5	5	10	15	%	V_{DS} = 20 V, V_{GS} = 0	
17		$\|V_{GS1}-V_{GS2}\|$	Differential Gate-Source Voltage	5	10	15	20	25	mV	V_{DG} = 20 V, I_D = 200 μA	
18		$\frac{\Delta\|V_{GS1}-V_{GS2}\|}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 2)	10	25	50	75	100	μV/°C		T_A = 25°C T_B = 125°C
19				10	25	50	75	100			T_A = -55°C T_B = 25°C
20		$\frac{(g_{fs1}-g_{fs2})}{g_{fs1}}$	Transconductance Match (Note 1)	3	5	5	10	15	%		f = 1 kHz
21		$\|g_{os1}-g_{os2}\|$	Differential Output Conductance	5	5	5	5	5	μmho		

NOTES:
1. Pulse test required, pulsewidth = 300 μs, duty cycle ⩽ 3%.
2. Measured at end points, T_A and T_B.

NQP

U257

matched dual n-channel JFET *designed for . . .*

Siliconix

- **Wideband Differential Amplifiers**

Performance Curves NZF-D, NNZ
See Section 4

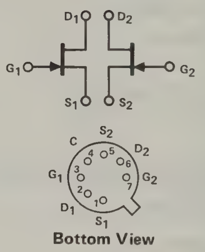
BENEFITS

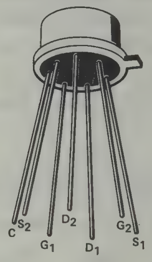
- **High Gain through 100 MHz g_{fs} = 4500 μmho Minimum**
- **Matching Characteristics Specified**

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . –25 V
Gate Current . . . . 50 mA
Device Dissipation (Each Side), T_A = 85°C
(Derate 3.85 mW/°C) . . . . 250 mW
Total Device Dissipation, T_A = 85°C
(Derate 7.7 mW/°C) . . . . 500 mW
Storage Temperature Range . . . . –65 to + 200°C
Lead Temperature
(1/16″ from case for 10 seconds) . . . . .300°C

TO-78
See Section 6





ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	S T A T I C	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -15 V, V_{DS} = 0	
2					-250	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-5		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	5	40	mA	V_{DS} = 10 V, V_{GS} = 0	
6	D Y N A M I C	g_{fs}	Common-Source Forward Transconductance	4500	10,000	μmho	V_{DS} = 10 V, I_D = 5 mA	f = 1 kHz
7		g_{fs}	Common-Source Forward Transconductance	4500	10,000		V_{DG} = 10 V, I_D = 5 mA	f = 100 MHz
8		g_{os}	Common-Source Output Conductance		200		V_{DS} = 10 V, I_D = 5 mA	f = 1 kHz
9		g_{os}	Common-Source Output Conductance		200		V_{DG} = 10 V, I_D = 5 mA	f = 100 MHz
10		C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
12		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		30	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
13	M A T C H I N G	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.85	1		V_{DS} = 10 V, V_{GS} = 0	
14		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		100	mV	V_{DG} = 10 V, I_D = 5 mA	
15		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 2)	0.85	1			f = 1 kHz
16		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		20	μmho		

NOTES:
1. Pulse test required, pulse width = 300 μs, duty cycle ⩽ 30%.
2. Assumes smaller value in numerator.

NZF-D, NNZ

n-channel JFETs *designed for . . .*

Siliconix

- **Analog Switches**
- **Commutators**
- **Choppers**

Performance Curves NVA
See Section 4

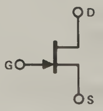
BENEFITS

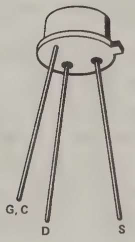
- **Ultra-Low Insertion Loss** $r_{DS(on)} < 3.0\,\Omega$ **(U290)**
- **High Off-Isolation** $I_{D(off)} < 1$ **nA**

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage	–30 V
Gate Current	100 mA
Drain Current	1.5 A
Total Device Dissipation at 25°C Free-Air Temperature (Note 1)	500 mW
Storage Temperature Range	–65 to +200°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

TO-52
See Section 6





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U290		U291		Unit	Test Conditions	
				Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-1		-1	nA	V_{GS} = –15 V, V_{DS} = 0	
2					-1		-1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		V	I_G = –1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-1.5	-4.5		V_{DS} = 15 V, I_D = 3 nA	
5		$I_{D(off)}$	Drain Cutoff Current		1		1	nA	V_{DS} = 5 V, V_{GS} = –10 V	
6					1		1	μA		150°C
7		$V_{DS(on)}$	Drain-Source ON Voltage		3.0		70	mV	V_{GS} = 0, I_D = 10 mA	
8		I_{DSS}	Saturation Drain Current (Note 2)	500		200		mA	V_{DS} = 10 V, V_{GS} = 0	
9		$r_{DS(on)}$	Static Drain-Source ON Resistance	1.0	3.0	2	7	Ω	V_{GS} = 0 V, I_D = 10 mA	
10	DYNAMIC	$r_{ds(on)}$	Drain-Source ON Resistance	1.0	3.0	2	7	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
11		C_{SGO}	Source-Gate OFF Capacitance		30		30	pF	V_{SG} = 15 V, I_D = 0	f = 1 MHz
12		C_{DGO}	Drain-Gate OFF Capacitance		30		30		V_{DG} = 15 V, I_S = 0	
13		$C_{SG}+C_{DG}$	Source Gate Plus Drain Gate On Capacitance		160		160		V_{DS} = 0, V_{GS} = 0	
14	SW	$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	V_{DD} = 1.5 V, $I_{D(on)}$ = 30 mA, R_L = 50 Ω, $V_{GS(on)}$ = 0 V, $V_{GS(off)}$ = –12 V (U290) $V_{GS(off)}$ = – 7 V (U291)	
15		t_r	Rise Time		20		20			
16		$t_{d(off)}$	Turn-OFF Delay Time		15		15			
17		t_f	Fall Time		20		20			

NVA

NOTES:

1. Derate linearly at the rate of 4.0 mW/°C.
2. Pulse test required pulsewidth 300 μs, duty cycle ≤ 3%.

Siliconix

p-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**

Performance Curves PSA
See Section 4

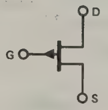
BENEFITS

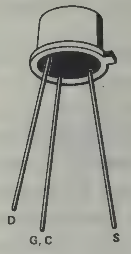
- Low Insertion Loss
  $r_{DS(on)} < 85\ \Omega$ (U304)
- High Off-Isolation
  $I_{D(off)} < 500$ pA

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage (Note 1)	30 V
Gate Current	50 mA
Total Device Dissipation, Free-Air (Derate 2.8 mW/°C)	350 mW
Storage Temperature Range	–65 to +200°C
Lead Temperature (1/16″ from case for 60 seconds)	300°C

TO-18
See Section 6





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U304 Min	U304 Max	U305 Min	U305 Max	U306 Min	U306 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		500		500		500	pA	$V_{GS} = 20$ V, $V_{DS} = 0$	
2					1.0		1.0		1.0	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	$I_G = 1\ \mu A$, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	5	10	3	6	1	4		$V_{DS} = -15$ V, $I_D = -1\ \mu A$	
5		$V_{DS(on)}$	Drain-Source ON Voltage		-1.3		-0.8		-0.6		$V_{GS} = 0$, $I_D = -15$ mA (U304), $I_D = -7$ mA (U305), $I_D = -3$ mA (U306)	
6		I_{DSS}	Saturation Drain Current (Note 2)	-30	-90	-15	-60	-5	-25	mA	$V_{DS} = -15$ V, $V_{GS} = 0$	
7		$I_{D(off)}$	Drain Cutoff Current		-500		-500		-500	pA	$V_{DS} = -15$ V, $V_{GS} = 12$ V (U304), $V_{GS} = 7$ V (U305), $V_{GS} = 5$ V (U306)	
8					-1.0		-1.0		-1.0	μA		150°C
9		$r_{DS(on)}$	Static Drain-Source ON Resistance		85		110		175	Ω	$V_{GS} = 0$ V, $I_D = -1$ mA	
10	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		85		110		175	Ω	$V_{GS} = 0$ V, $I_D = 0$	f = 1 kHz
11		C_{iss}	Common-Source Input Capacitance		27		27		27	pF	$V_{DS} = -15$ V, $V_{GS} = 0$	f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		7		7		7		$V_{DS} = 0$, $V_{GS} = 12$ V (U304) $V_{GS} = 7$ V (U305), $V_{GS} = 5$ V (U306)	
13	SWITCH	$t_{d(on)}$	Turn–ON Delay Time		20		25		25	ns		
14		t_r	Rise Time		15		25		35			
15		$t_{d(off)}$	Turn–OFF Delay Time		10		15		20			
16		t_f	Fall Time		25		40		60			

	U304	U305	U306
V_{DD}	–10 V	–6 V	–6 V
$V_{GS(off)}$	12 V	7 V	5 V
R_L	580 Ω	743 Ω	1800 Ω
$V_{GS(on)}$	0	0	0
$I_{D(on)}$	–15 mA	–7 mA	–3 mA

NOTES:
1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
2. Pulse test pulsewidth = 300 μs, duty cycle ⩽ 3%.

PSA

n-channel JFETs *designed for . . .*

Siliconix

- VHF Amplifiers
- Front End High Sensitivity Amplifiers
- Oscillators
- Mixers

U308 U309 U310
PLASTIC EQUIVALENT J308 SERIES

Performance Curves NZA
See Section 4

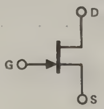
BENEFITS

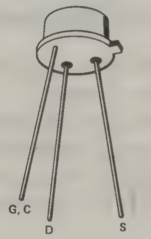
- Industry Standard
- High Power Gain
  16 dB at 105 MHz, Common-Gate
  11 dB at 450 MHz, Common-Gate
- Low Noise
  2.7 dB Noise Figure at 450 MHz
- Wide Dynamic Range
  Greater than 100 dB
- 75 Ω Input Match Common Gate

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . –25 V
Gate Current . . . . 20 mA
Total Power Dissipation at T_A = 25°C . . . . 500 mW
Power Derating to 150°C . . . . 4.0 mW/°C
Storage Temperature Range . . . . –65 to +200°C
Lead Temperature
(1/16″ from case for 10 seconds) . . . . 300°C

TO-52
See Section 6





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U308			U309			U310			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current			–150			–150			–150	pA	V_{GS} = –15 V, V_{DS} = 0	
2						–150			–150			–150	nA		T_A = 125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25			–25			–25			V	I_G = –1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–1.0		–6.0	–1.0		–4.0	–2.5		–6.0		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	V_{DS} = 10 V, V_{GS} = 0	
6		$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	I_G = 10 mA, V_{DS} = 0	
7	DYNAMIC	g_{fg}	Common-Gate Forward Transconductance (Note 1)	10	17		10	17		10	17		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
8		g_{og}	Common-Gate Output Conductance			250			250			250	μmho		
9		C_{gd}	Drain-Gate Capacitance			2.5			2.5			2.5	pF	V_{GS} = –10 V, V_{DS} = 10 V	f = 1 MHz
10		C_{gs}	Gate-Source Capacitance			5.0			5.0			5.0			
11		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, I_D = 10 mA	f = 100 Hz
12	HI FREQ	g_{fg}	Common-Gate Forward Transconductance		15			15			15		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
13					14			14			14				f = 450 MHz
14		g_{og}	Common-Gate Output Conductance		0.18			0.18			0.18				f = 105 MHz
15					0.32			0.32			0.32				f = 450 MHz
16		G_{pg}	Common-Gate Power Gain (Note 2)	14	16		14	16		14	16		dB		f = 105 MHz
17				10	11		10	11		10	11				f = 450 MHz
18		NF	Noise Figure		1.5	2.0		1.5	2.0		1.5	2.0			f = 105 MHz
19					2.7	3.5		2.7	3.5		2.7	3.5			f = 450 MHz

NOTES:
1. Pulse test duration = 2 ms.
2. Gain (G_{pg}) measured at optimum input noise match.

NZA

U311

PREFERRED PART U310

Siliconix

n-channel JFET *designed for . . .*

- **VHF Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NZA
See Section 4

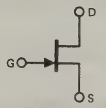
BENEFITS

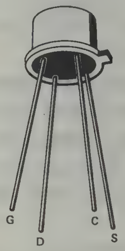
- High Power Gain
  - 16 dB Typ @ 105 MHz, Common-Gate
  - 11 dB Typ @ 450 MHz, Common-Gate
- Low Noise Figure
  - 1.5 dB Typ @ 105 MHz
  - 2.7 dB Typ @ 450 MHz
- Wide Dynamic Range—Greater than 100 dB

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	–25 V
Gate Current	10 mA
Total Device Dissipation (Derate 1.7 mW/°C)	300 mW
Storage Temperature Range	–65 to +200°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

TO-72
See Section 6





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	Min	Max	Typ	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-150		pA	V_{GS} = -15 V, V_{DS} = 0	
2					-150		nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			V	I_G = -1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-6			V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	20	60		mA	V_{DS} = 10 V, V_{GS} = 0	
6		$V_{GS(f)}$	Gate-Source Forward Voltage		1		V	I_G = 1 mA, V_{DS} = 0	
7	DYN	g_{fg}	Common-Gate Forward Transconductance (Note 1)	10,000		17,000	µmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
8		g_{og}	Common-Gate Output Conductance		250				
9		C_{gd}	Gate-Drain Capacitance		2.5		pF	V_{DG} = 10 V, I_D = 5 mA	f = 1 MHz
10		C_{gs}	Gate-Source Capacitance		5.0				

NOTE:
1. Pulse test duration = 2 ms.

NZA

Siliconix

n-channel JFETs designed for . . .

- **VHF Buffer Amplifiers**
- **IF Amplifiers**

Performance Curves NIP
See Section 5

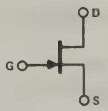
BENEFITS

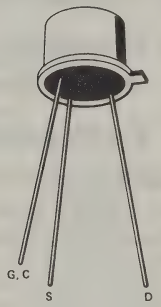
- High Gain
  g_{fs} = 120,000 μmho Typical
- Wide Dynamic Range
- Low Intermodulation Distortion

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	−25 V
Gate Current	100 mA
Total Device Dissipation (25°C Case Temperature)	3 W
Power Derating (to 150°C)	24 mW/°C
Storage Temperature Range	−55 to +150°C
Operating Temperature Range	−55 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-39
See Section 6





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Characteristic			U320			U321			U322			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-3			-3			-3	nA	V_{GS} = -15 V, V_{DS} = 0 V	
2						-0.5			-0.5			-0.5	μA		T = 100°C
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-2		-10	-1		-4	-3		-10	V	V_{DS} = 5 V, I_D = 1 mA	
4		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25				I_G = -1 μA, V_{DS} = 0 V	
5		I_{DSS}	Saturation Drain Current (Note 2)	100		500	80		250	200		700	mA	V_{DS} = 15 V, V_{GS} = 0 V	
6		$V_{GS(f)}$	Gate-Source Forward Voltage			1			1			1	V	I_G = 1 mA, V_{DS} = 0 V	
7		$r_{DS(on)}$	Drain-Source ON Resistance			10			11			8	Ω	V_{GS} = 0 V, I_D = 10 mA	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	75	120	200	75	120	200	75	130	200	mmhos	V_{DS} = 15 V, V_{GS} = 0 V	f = 1 kHz
9		C_{iss}	Common-Source Input Capacitance			30			30			30	pF	V_{GS} = -10 V, V_{DS} = 0 V	f = 1 MHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance			15			15			15			
11		C_{gs}	Gate-Source Capacitance		12			12			12			V_{GS} = -10 V, I_D = 0	
12		C_{gd}	Gate-Drain Capacitance		12			12			12			V_{GD} = -10 V, I_S = 0	
13		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		2			2			2		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 5 V, I_D = 10 mA	f = 1 kHz
14	HIGH FREQ	g_{fg}	Common Gate Forward Transconductance		55			55			55		mmho	V_{DG} = 20 V, I_D = 25 mA	f = 50 MHz
15		g_{ig}	Common-Gate Input Conductance		56			56			56				
16		g_{og}	Common-Gate Output Conductance		0.5			0.5			0.5				
17		G_{PS}	Power Gain (Note 3)		9			9			9		dB		
18		F_t	Gain-Bandwidth (Note 4)		400			400			400		MHz	V_{DS} = 15 V, V_{GS} = 0 V	
19		NF	Noise Figure (Note 3)		2.5			2.5			2.5		dB	V_{DG} = 20 V, I_D = 25 mA	f = 30 MHz

NOTES:

NIP

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.
3. Noise figure (SSB) and power gain measured in circuit shown in Figure 1.
4. Computed as g_{fs}/C_{rss}.

U401 U402 U403 U404 U405 U406

Siliconix

monolithic dual n-channel JFETs *designed for . . .*

- Low Noise FET Input Amplifiers
- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Comparators

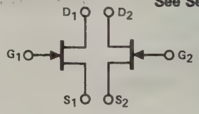
ABSOLUTE MAXIMUM RATINGS (25°C)

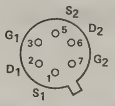
Gate-Drain or Gate-Source Voltage	50 V
Forward Gate Current	10 mA
Device Dissipation (each side)	
@ $T_A = 85°C$ derate 2.6 mW/°C	300 mW
Total Device Dissipation	
@ $T_A = 85°C$ (derate 5 mW/°C)	500 mW
Storage Temperature Range	−65 to 200°C

Performance Curves NNR See Section 4

BENEFITS

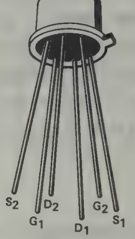
- Minimum System Error and Calibration
  - 5 mV Offset Maximum (U401)
  - 95 dB Minimum CMRR (U401-04)
- Low Drift with Temperature
  - 10 µV/°C Maximum (U401, 02)
- Operates from Low Power Supply Voltages
  - $V_{GS(off)} < 2.5$ V
- Simplifies Amplifier Design
  - Output Conductance < 2 µmho
- Low Noise
  - $\overline{e}_n = 6\ nV/\sqrt{Hz}$ at 10 Hz Typical





Bottom View

TO-71
See Section 6



ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

		Characteristic		U401		U402		U403		U404		U405		U406		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−50		−50		−50		−50		−50		−50		V	$V_{DS} = 0$, $I_G = -1\ \mu A$	
2		I_{GSS}	Gate Reverse Current (Note 1)		−25		−25		−25		−25		−25		−25	pA	$V_{DS} = 0$, $V_{GS} = -30$ V	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	V	$V_{DS} = 15$ V, $I_D = 1$ nA	
4		$V_{GS(on)}$	Gate-Source Voltage (on)		−2.3		−2.3		−2.3		−2.3		−2.3		−2.3		$V_{DG} = 15$ V, $I_D = 200\ \mu A$	
5		I_{DSS}	Saturation Drain Current (Note 2)	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	mA	$V_{DS} = 10$ V, $V_{GS} = 0$	
6		I_G	Gate Current (Note 1)		−15		−15		−15		−15		−15		−15	pA	$V_{DG} = 15$ V, $I_D = 200\ \mu A$	
7					−10		−10		−10		−10		−10		−10	nA		$T_A = 125°C$
8		BV_{G1-G2}	Gate-Gate Breakdown Voltage	±50		±50		±50		±50		±50		±50		V	$V_{DS} = 0$, $V_{GS} = 0$, $I_G = \pm 1\ \mu A$	
9	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	µmho	$V_{DS} = 10$ V, $V_{GS} = 0$	f = 1 kHz
10		g_{os}	Common-Source Output Conductance		20		20		20		20		20		20			
11		g_{fs}	Common-Source Forward Transconductance	1000	2000	1000	2000	1000	2000	1000	2000	1000	2000	1000	2000		$V_{DG} = 15$ V, $I_D = 200\ \mu A$	f = 1 kHz
12		g_{os}	Common-Source Output Conductance		2.0		2.0		2.0		2.0		2.0		2.0			
13		C_{iss}	Common-Source Input Capacitance		8.0		8.0		8.0		8.0		8.0		8.0	pF		f = 1 MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance		3.0		3.0		3.0		3.0		3.0		3.0			
15		$\overline{e}_N$	Equivalent Short-Circuit Input Noise Voltage		20		20		20		20		20		20	$\frac{nV}{\sqrt{Hz}}$	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 10 Hz
16	MATCHING	CMRR	Common-Mode Rejection Ratio (Note 3)	95		95		95		95		90				dB	V_{DG} = 10 to 20 V, $I_D = 200\ \mu A$	
17		$\|V_{GS1} - V_{GS2}\|$	Differential Gate-Source Voltage		5		10		10		15		20		40	mV	$V_{DG} = 10$ V, $I_D = 200\ \mu A$	
18		$\frac{\Delta\|V_{GS1} - V_{GS2}\|}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 4).		10		10		25		25		40		80	µV/°C	$V_{DG} = 10$ V, $I_D = 200\ \mu A$	$T_A = -55°C$, $T_B = +25°C$ $T_C = +125°C$

NOTES:

1. Approximately doubles for every 10°C increase in T_A. 2. Pulse test duration = 300 µs; duty cycle ≤ 3%. 3. $CMRR = 20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta|V_{GS1}-V_{GS2}|}\right]$, $\Delta V_{DD} = 10$ V.
4. Measured at end points, T_A, T_B and T_C.

NNR

monolithic dual n-channel JFETs

Siliconix

designed for . . .

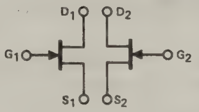
- **FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

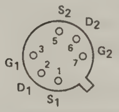
Performance Curves NQP
See Section 4

BENEFITS

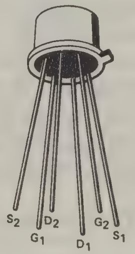
- Low Cost
- Minimum System Error and Calibration
  10 mV Offset Maximum (U410)
  70 dB Minimum CMRR (U410)
- Low Drift with Temperature
  10 μV/°C Maximum (U410)
- Simplifies Amplifier Design
  Low Output Conductance

TO-71
See Section 6





Bottom View



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-To-Gate Voltage . . . . ±40 V
Gate-Drain or Gate-Source Voltage . . . . –40 V
Gate Current . . . . 50 mA
Total Package Dissipation (25°C Free-Air) . . . . 375 mW
Power Derating . . . . 3.0 mW/°C
Storage Temperature Range . . . . –65 to +150°C
Lead Temperature (1/16″ from case for 10 seconds) . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic				U410			U411			U412			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-200			-200			-200	pA	V_{DS} = 0, V_{GS} = -30 V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5		-3.5	-0.5		-3.5	-0.5		-3.5	V	V_{DS} = 20 V, I_D = 1 nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40			-40			-40				V_{DS} = 0 V, I_G = -1 μA	
4		I_{DSS}	Saturation Drain Current (Note 2)	0.5		5.0	0.5		5.0	0.5		5.0	mA	V_{DS} = 20 V, V_{GS} = 0 V	
5		I_G	Gate Current (Note 1)			-200			-200			-200	pA	V_{DG} = 20 V, I_D = 200 μA	
6		V_{GS}	Gate-Source Voltage	-0.2		-3.0	-0.2		-3.0	-0.2		-3.0	V		
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000		4,000	1,000		4,000	1,000		4,000	μmho	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
8				600		1,200	600		1,200	600		1,200		V_{DG} = 20 V, I_D = 200 μA	
9		g_{os}	Common-Source Output Conductance			20			20			20		V_{DS} = 20 V, V_{GS} = 0 V	
10						5			5			5		V_{DG} = 20 V, I_D = 200 μA	
11		C_{iss}	Common-Source Input Capacitance		4.5			4.5			4.5		pF	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			1.2			1.2				
13		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage			50			50			50	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 20 V, I_D = 200 μA	f = 100 Hz
14	MATCHING	$\|V_{GS1}-V_{GS2}\|$	Differential Gate-Source Voltage			10			20			40	mV	V_{DG} = 20 V, I_D = 200 μA	
15		$\frac{\Delta\|V_{GS1}-V_{GS2}\|}{\Delta T}$	Gate-Source Differential Drift (Note 3)			10			25			80	μV/°C	V_{DG} = 20 V, I_D = 200 μA T_A = 25°C to T_B = 85°C	
16		CMRR	Common-Mode Rejection Ratio (Note 4)		80			80			70		dB	V_{DD} = 10 V to V_{DD} = 20 V I_D = 200 μA	

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μsec; duty cycle ≤ 3%.
3. Measured at end points, T_A and T_B.
4. CMRR = $20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta|V_{GS1}-V_{GS2}|}\right]$, ΔV_{DD} = 10 V.

NQP

monolithic dual n-channel JFETs *designed for . . .*

- ■ **Very High Input Impedance Differential Amplifiers**
  Electrometers
- ■ **Impedance Converters**

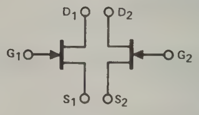
Siliconix

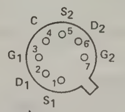
Performance Curves NNT
See Section 4

BENEFITS

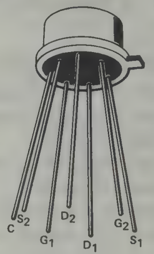
- High Input Impedance
  I_G = 0.25 pA Maximum (U421-3)
- High Gain g_{fs} = 120 µmho Minimum @ I_D = 30 µA (U421-6)
- Low Power Supply Operation
  $V_{GS(off)}$ = 2 V Maximum (U421-3)
- Minimum System Error and Calibration
  10 mV Maximum Offset
  90 dB Minimum CMRR (U421, U424)

TO-78
See Section 6





Bottom View



ABSOLUTE MAXIMUM RATINGS (25° C)

Gate-to-Gate Voltage .... ±40 V
Gate-Drain or Gate-Source Voltage .... –40 V
Gate Current .... 10 mA
Device Dissipation (Each Side), T_A = 25°C
(Derate 3.2 mW/°C to 150°C) .... 400 mW
Total Device Dissipation, T_A = 25°C
(Derate 6.0 mW/°C to 150°C) .... 750 mW
Storage Temperature Range .... –65°C to +150°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U421-3			U424-6			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–40	–60		–40	–60		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2		BV_{G1G2}	Gate-Gate Breakdown Voltage	±40			±40				$I_G = -1\ \mu A$, $I_D = 0$, $I_S = 0$	
3		I_{GSS}	Gate Reverse Current (Note 1)			1.0			3.0	pA	T = +25°C	$V_{GS} = -20$ V, $V_{DS} = 0$
						1.0			3.0	nA	T = +125°C	
4		I_G	Gate Operating Current (Note 1)			.25			0.5	pA	T = +25°C	$V_{DG} = 10$ V, $I_D = 30\ \mu A$
						250			500		T = +125°C	
5		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.4		–2.0	–0.4		–3.0	V	$V_{DS} = 10$ V, $I_D = 1$ nA	
6		V_{GS}	Gate-Source Voltage			–1.8			–2.9		$V_{DG} = 10$ V, $I_D = 30\ \mu A$	
7		I_{DSS}	Saturation Drain Current	60		1000	60		1800	µA	$V_{DS} = 10$ V, $V_{GS} = 0$	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	300		1500	300		1500	µ℧	$V_{DS} = 10$ V, $V_{GS} = 0$	f = 1 kHz
9		g_{os}	Common-Source Output Conductance			5.0			5.0			
10		C_{iss}	Common-Source Input Capacitance			3.0			3.0	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance			1.5			1.5			
12		g_{fs}	Common-Source Forward Transconductance	120		350	120		350	µ℧	$V_{DG} = 10$ V, $I_D = 30\ \mu A$	f = 1 kHz
13		g_{os}	Common-Source Output Conductance			3.0			3.0			
14		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20	70		20	70	nV/√Hz		f = 10 Hz
					10			10				f = 1 kHz
15		NF	Noise Figure			1.0			1.0	dB	f = 10 Hz	$R_G = 10\text{M}\ \Omega$

		Characteristic		U421, 4			U422, 5			U423,6			Unit	Test Conditions
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
16	MATCH	$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage			10			15			25	mV	$V_{DG} = 10$ V, $I_D = 30\ \mu A$
17		$\frac{\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Differential Gate-Source Voltage Change With Temperature (Note 2)			10			25			40	µV/°C	$V_{DG} = 10$ V, $I_D = 30\ \mu A$, $T_A = -55°C$, $T_B = 25°C$, $T_C = 125°C$
18		CMRR	Common Mode Rejection Ratio (Note 3)	90	95		80	90		80	90		dB	$I_D = 30\ \mu A$, V_{DG} = 10 to 20 V

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Measured at end points T_A, T_B and T_C.
3. CMRR = $20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta \lvert V_{GS1} - V_{GS2} \rvert}\right]$, $\Delta V_{DD} = 10$ V.
4. Case lead not connected.

NNT

monolithic dual n-channel JFETs *designed for . . .*

- **Very High Input Impedance Differential Amplifiers**
  - **Electrometers**
- **Impedance Converters**

Performance Curves NNT
See Section 4

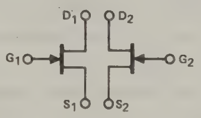
BENEFITS

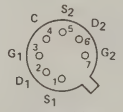
- **High Input Impedance** I_G **= 5 pA (U427)**
- **High Gain** g_{fs} **= 120 µmho Minimum @** I_D **= 30 µA**
- **Low Power Supply Operation** $V_{GS(off)}$ **= 2 V Maximum (U427)**
- **Minimum System Error and Calibration 25 mV Maximum Offset**

ABSOLUTE MAXIMUM RATINGS (25°C)

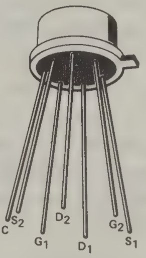
Gate-to-Gate Voltage	±40 V
Gate-Drain or Gate-Source Voltage	–40 V
Gate Current	10 mA
Device Dissipation (Each Side), T_A = 25°C (Derate 3.2 mW/°C to 150°C)	400 mW
Total Device Dissipation, T_A = 25°C (Derate 6.0 mW/°C to 150°C)	750 mW
Storage Temperature Range	–65 to +150°C

TO-78
See Section 6





Bottom View



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U427 Min	U427 Typ	U427 Max	U428 Min	U428 Typ	U428 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–40	–60		–40	–60		V	I_G = –1 µA, V_{DS} = 0	
2		BV_{G1G2}	Gate-Gate Breakdown Voltage	±40			±40				I_G = –1 µA, I_D = 0, I_S = 0	
3		I_{GSS}	Gate Reverse Current (Note 1)			5			10	pA	T = +25°C	V_{GS} = –20 V, V_{DS} = 0
						5			10	nA	T = +125°C	
4		I_G	Gate Operating Current (Note 1)			3			5	pA	T = +25°C	V_{DG} = 10 V, I_D = 30 µA
						3			5	nA	T = +125°C	
5		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.4		–2.0	–0.4		–3.0	V	V_{DS} = 10 V, I_D = 1 nA	
6		V_{GS}	Gate-Source Voltage			–1.8			–2.9		V_{DG} = 10 V, I_D = 30 µA	
7		I_{DSS}	Saturation Drain Current	60		1000	60		1800	µA	V_{DS} = 10 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	300		800	300		1500	µ℧	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
9		g_{os}	Common-Source Output Conductance			3.0			5.0			
10		C_{iss}	Common-Source Input Capacitance			3.0			3.0	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance			1.5			1.5			
12		g_{fs}	Common-Source Forward Transconductance	120		350	120		350	µ℧	V_{DG} = 10 V, I_D = 30 µA	f = 1 kHz
13		g_{os}	Common-Source Output Conductance			0.5			1.0			
14		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		20	50		20	70	nV/√Hz		f = 10 Hz
					10			10				f = 1 kHz
15		NF	Noise Figure			1.0			1.0	dB	f = 10 Hz	R_G = 10M Ω
16	MATCH	$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage			25			40	mV	V_{DG} = 10 V, I_D = 30 µA	
17		$\frac{\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Differential Gate-Source Voltage Change With Temperature (Note 2)			40			80	µV/°C	V_{DG} = 10 V, I_D = 30 µA, T_A = –55°C, T_B = 25°C, T_C = 125°C	
18		CMRR	Common Mode Rejection Ratio (Note 3)		90			90		dB	I_D = 30 µA, V_{DG} = 10 to 20 V	

NOTES.

1. Approximately doubles for every 10°C increase in T_A.
2. Measured at end points T_A, T_B and T_C.
3. $\text{CMRR} = 20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta \lvert V_{GS1}-V_{GS2} \rvert}\right]$ ΔV_{DD} = 10 V.
4. Case lead not connected.

NNT

Siliconix

matched dual n-channel JFETs *designed for . . .*

- **Balanced Mixers**
- **Differential Amplifiers**

Performance Curves NZA
See Section 4

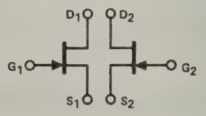
BENEFITS

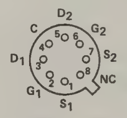
- Low Noise Figure
- Low IMD-
  30 dBm Intercept Point

ABSOLUTE MAXIMUM RATINGS (25°C)

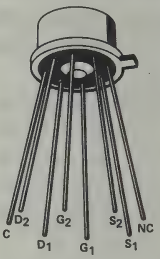
Gate-Drain or Gate-Source Voltage . . . . –25 V
Gate Current . . . . 10 mA
Total Continuous Power Dissipation at
(or Below) 25°C Free Air Temperature
Derate 4 mW/°C to 150°C. 500 mW
Continuous Device Dissipation (Each Side) at
(or Below) 25°C Free Air Temperature
Derate 2.4 mW/°C to 150°C . . . . 300 mW
Storage Temperature Range . . . . –65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . 300°C

TO-99/TO-78
See Section 6





Bottom View



ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)

	Characteristic			U430			U431			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current			-150			-150	pA	V_{GS} = –15 V, V_{DS} = 0 V	
2						-150			-150	nA		T = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			V	I_G = -1 μA, V_{DS} = 0 V	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0		-4.0	-2.0		-6.0		V_{DS} = 10 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0		V_{DS} = 0 V, I_G = 10 mA	
6		I_{DSS}	Saturation Drain Current (Note 4)	12		30	24		60	mA	V_{DS} = 10 V, V_{GS} = 0 V	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	10	17		10	17		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
8		g_{os}	Common-Source Output Conductance			250			250	μmho		
9		C_{gs}	Gate-Source Capacitance			5.0			5.0	pF	V_{GS} = -10 V, V_{DS} = 0 V	f = 1 MHz
10		C_{gd}	Drain Gate Capacitance			2.5			2.5			
11		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, I_D = 10 mA	f = 100 Hz
12	HI FREQ	g_{fs}	Common-Source Forward Transconductance		12			12		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 100 MHz
13		g_{os}	Common-Source Output Conductance		0.15			0.15				
14		g_{ig}	Power-Match Source Admittance		12			12				
15		G_c	Conversion Gain (See Note 1)		3.0			3.0		dB	V_{DS} = 20 V, V_{GS} = 1/2 $V_{GS(off)}$	
16		IMD	Intercept Point (See Notes 1 and 2)		+30			+30		dBm		
17	MATCH	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 3)	0.9		1.0	0.9		1.0		V_{DS} = 10 V	V_G = 0 V
18		$\frac{V_{GS(off)1}}{V_{GS(off)2}}$	Gate-Source Cutoff Voltage Ratio (Note 3)	0.9		1.0	0.9		1.0			I_D = 1 nA
19		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 3)	0.9		1.0	0.9		1.0			I_D = 10 mA

NOTES:

1. VHF single-balanced mixer drain load impedance 2k Ω.
2. 2-tone 3rd-order IMD.
3. Assumes smaller value in numerator.
4. Pulse test pulsewidth = 300 μs, duty cycle ⩽ 3%.

NZA

matched dual n-channel JFETs *designed for . . .*

Siliconix

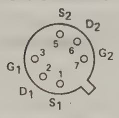
■ VHF/UHF Amplifiers

Performance Curves NZF, NNZ
See Section 4

BENEFITS

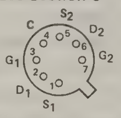
- High Gain
  g_{fs} = 4500 μmho Minimum
- Dual Version of J300 with Matched Gate-to-Source Voltage

TO-71
See Section 6

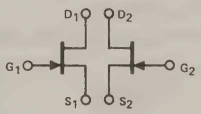


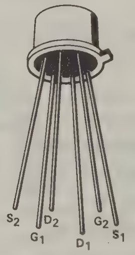
Bottom View

TO-78
See Section 6

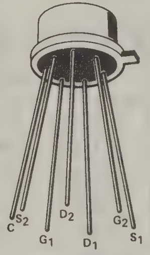


Bottom View





TO-71 = U440, U441



TO-78 = U443, U444

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-To-Gate Voltage .... ±50 V
Gate-Drain or Gate-Source Voltage .... -25 V
Gate Current .... 50 mA
Total Package Dissipation
(25°C Free-Air Temperature) .... 350 mW
Power Derating .... 2.8 mW/°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature
(1/16″ from case for 10 seconds) .... 300°C)

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U440/U443			U441/U444			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-500			-500	pA	$V_{DS} = 0$, $V_{GS} = -15$ V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1		-6	-1		-6	V	$V_{DS} = 10$ V, $I_D = 1$ nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25				$V_{DS} = 0$, $I_G = -1$ μA	
4		I_{DSS}	Saturation Drain Current (Note 2)	6		30	6		30	mA	$V_{DS} = 10$ V, $V_{GS} = 0$	
5		I_G	Gate Current (Note 1)			-500			-500	pA	$V_{DG} = 10$ V, $I_D = 5$ mA	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4,500		9,000	4,500		9,000	μmho	$V_{DG} = 10$ V, $I_D = 5$ mA	f = 1 kHz
7		g_{os}	Common-Source Output Conductance			200			200			
8		C_{iss}	Common-Source Input Capacitance		3.5			3.5		pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		0.8			0.8				
10	MAT	$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage			10			20	mV	$V_{DG} = 10$ V, $I_D = 5$ mA	

NZF, NNZ

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μsec; duty cycle ⩽ 3%.

n-channel JFETs *designed for . . .*

Siliconix

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves NCA
See Section 4

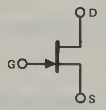
BENEFITS

- Low Insertion Loss
  $r_{DS(on)} < 30\ \Omega$ (U1897)
- No Error or Offset Voltage Generated by Closed Switch
  Purely Resistive

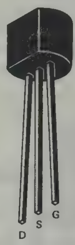
ABSOLUTE MAXIMUM RATINGS (25°C)

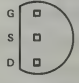
Gate-Drain or Gate-Source Voltage . . . . –40V
Gate Current . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . –55 to 135°C
Storage Temperature Range . . . . –55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . 300°C

TO-92
See Section 6



Plastic





Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U1897		U1898		U1899		Unit	Test Conditions
				Min	Max	Min	Max	Min	Max		
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–40		–40		–40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$
2		BV_{DGO}	Drain-Gate Breakdown Voltage	40		40		40			$I_G = -1\ \mu A$, $I_S = 0$
3		BV_{SGO}	Source-Gate Breakdown Voltage	40		40		40			$I_G = -1\ \mu A$, $I_D = 0$
4		I_{GSS}	Gate Reverse Current		–400		–400		–400	pA	$V_{GS} = -20$ V, $V_{DS} = 0$
5		I_{DGO}	Drain-Gate Leakage Current		200		200		200		$V_{DG} = 20$ V, $I_S = 0$
6		I_{SGO}	Source-Gate Leakage Current		200		200		200		$V_{SG} = 20$ V, $I_D = 0$
7		$I_{D(off)}$	Drain Cutoff Current		200		200		200		$V_{DS} = 20$ V, $V_{GS} = -12$ V (U1897) $V_{GS} = -8$ V (U1898) $V_{GS} = -6$ V (U1899)
8					10		10		10	nA	$T_A = 85°C$
9		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–5.0	–10	–2.0	–7.0	–1.0	–5.0	V	$V_{DS} = 20$ V, $I_D = 1$ nA
10		I_{DSS}	Saturation Drain Current (Note 1)	30		15		8.0		mA	$V_{DS} = 20$ V, $V_{GS} = 0$
11		$V_{DS(on)}$	Drain-Source ON Voltage		0.2		0.2		0.2	V	$V_{GS} = 0$, $I_D = 6.6$ mA (U1897) $I_D = 4.0$ mA (U1898), $I_D = 2.5$ mA (U1899)
12		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		50		80	Ω	$I_D = 1$ mA, $V_{GS} = 0$
13	DYNAMIC	C_{DG}	Drain-Gate Capacitance		5		5		5	pF	$V_{DG} = 20$ V, $I_S = 0$; f = 1 MHz
14		C_{SG}	Source-Gate Capacitance		5		5		5		$V_{SG} = 20$ V, $I_D = 0$
15		C_{iss}	Common-Source Input Capacitance		16		16		16		$V_{DS} = 20$ V, $V_{GS} = 0$
16		C_{rss}	Common-Source Reverse Transfer Capacitance		3.5		3.5		3.5		
17		$t_{d(on)}$	Turn ON Delay Time		15		15		20	ns	Switching Time Test Conditions
18		t_r	Rise Time		10		20		40		
19		t_{off}	Turn-OFF Time		40		60		80		

Switching Time Test Conditions

	U1897	U1898	U1899
V_{DD}	3 V	3 V	3 V
$V_{GS(on)}$	0	0	0
$V_{GS(off)}$	–12 V	–8 V	–6 V
R_L	430 Ω	700 Ω	1100 Ω
$I_{D(on)}$	6.6 mA	4 mA	2.5 mA

NOTE:
1. Pulse test pulsewidth = 300 μs; duty cycle ≤ 3%.

NCA

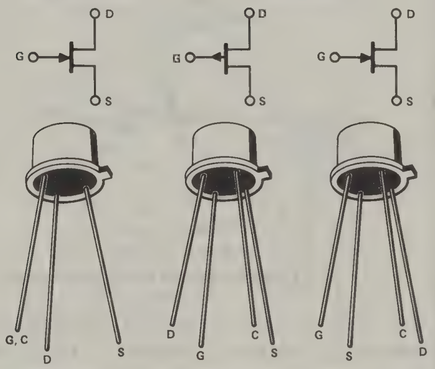
voltage-controlled resistor FETs *designed for . . .*

Siliconix

- **Small Signal Attenuators**
- **Filters**
- **Amplifier Gain Control**
- **Oscillator Amplitude Control**

Performance Curves NCA, NPA, NT, PSA See Section 4

TO-18 (MODIFIED) See Section 6 **TO-72 (MODIFIED) See Section 6**



VCR2N VCR4N **VCR3P VCR5P** **VCR7N**

ABSOLUTE MAXIMUM RATING (25°C)

Gate-Drain or Gate-Source Voltage . . . . 15 V
Gate Current . . . . 10 mA
Total Device Dissipation at T_A = 25°C
(Derate at 2.0 mW/°C to 175°C) . . . . 300 mW
Storage Temperature Range . . . . −55 to +175°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

N-Channel VCR FETs

		Characteristic		VCR2N		VCR4N		VCR7N		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-5		-0.2		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0	
2		BV_{GSS}	Gate-Source Breakdown Voltage	-15		-15		-15		V	I_G = -1 μA, V_{DS} = 0	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-3.5	-7	-3.5	-7	-2.5	-5		I_D = 1 μA, V_{DS} = 10 V	
4		$r_{ds(on)}$	Drain Source ON Resistance	20	60	200	600	4,000	8,000	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	DY	C_{dgo}	Drain-Gate Capacitance		7.5		3		1.5	pF	V_{GD} = -10 V, I_S = 0	f = 1 MHz
6		C_{sgo}	Source-Gate Capacitance		7.5		3		1.5		V_{GS} = -10 V, I_D = 0	

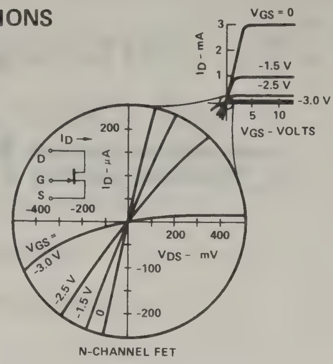
NCA NPA NT

P-Channel VCR FETs

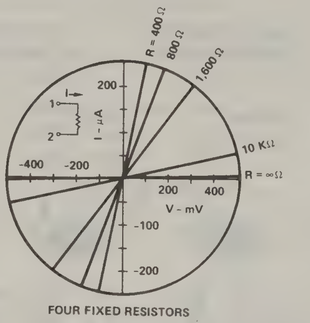
				VCR3P				
1	STATIC	I_{GSS}	Gate Reverse Current		20	nA	V_{GS} = 15 V, V_{DS} = 0	
2		BV_{GSS}	Gate-Source Breakdown Voltage	15		V	I_G = 1 μA, V_{DS} = 0	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	3.5	7		I_D = -1 μA, V_{DS} = -10 V	
4		$r_{ds(on)}$	Drain-Source ON Resistance	70	200	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	DY	C_{dgo}	Drain-Gate Capacitance		25	pF	V_{GD} = 10 V, I_S = 0	f = 1 MHz
6		C_{sgo}	Source-Gate Capacitance		15		V_{GS} = 10 V, I_D = 0	

PSA

APPLICATIONS



N-Channel JFET Output Characteristic Enlarged Around V_{DS} = 0
Figure 1



V-I Characteristic of Four Fixed Resistors
Figure 2

The VCR FET has an a-c drain-source resistance, evaluated around V_{DS} = 0, that is controlled by d-c bias voltage V_{GS} applied to the high-impedance gate terminal. Minimum r_{ds} occurs when V_{GS} = 0 and, as V_{GS} approaches the pinch-off voltage, r_{ds} rapidly increases. Comparing Fig. 1 and 2, for $V_{DS} < \pm 0.1$ volt and V_{GS} = constant, the VCR FET has a bilateral characteristic with no offset voltage, just like a fixed resistor. However, when $V_{DS} > \pm 0.1$ volts, the VCR FET characteristic has noticeable curvature.

This series of junction FETs is intended for applications where the drain-source voltage is a low-level a-c signal with no d-c component. Thus the FET operating point will swing symmetrically around V_{DS} = 0. In the first quadrant, signal distortion depends on what extent the FET output characteristic deviates from a straight line or linear relation. Besides the linearity problem in the third quadrant, when V_{GS} is near zero and $v_{ds} > 0.5$ volt rms, the gate-channel junction will become forward biased and cause additional curvature in the characteristic. Also, whenever the gate becomes forward biased due to any combination of V_{GS} and v_{ds}, it ceases to be a high-impedance control terminal for the VCR.

Fig. 3 presents a normalized plot of r_{DS} versus normalized V_{GS} where $V_{GS(off)}$ is defined as that value of V_{GS} at I_D/I_{DSS} = 0.001. The dynamic range of r_{DS} is shown as greater than 100:1. For best control of r_{DS} the normalized V_{GS} should lie between 0 and 0.8 $V_{GS(off)}$ because as V_{GS} approaches $V_{GS(off)}$, r_{DS} increases very rapidly so that r_{ds} control becomes very critical and unit-to-unit matching is almost impossible. In Fig. 4, $r_{ds(on)}$ (drain-source resistance at $V_{DS} = V_{GS} = 0$) varies as an inverse function of $V_{GS(off)}$. In Fig. 5 r_{ds} has a typical 0.7%/°C temperature coefficient for P-channels which decreases as V_{GS} approaches the zero t.c. point. N-channel devices have a typical 0.3%/°C t.c. Specific bias voltage to set operation at the zero t.c. point varies, as does $V_{GS(off)}$, from device to device.*

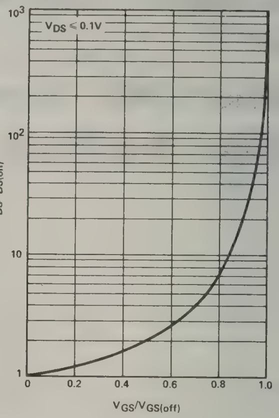


Fig. 3

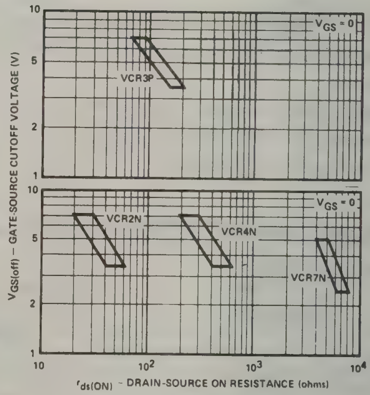


Fig. 4

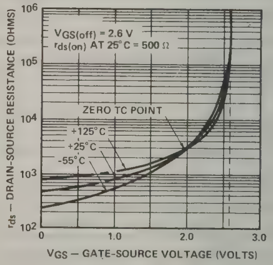


Fig. 5

For further information on using FETs as voltage-variable resistors, consult Siliconix Application Note AN73-1.

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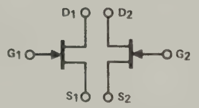
* L. Evans; "Biasing FETs for Zero DC Drift"; Electro Technology, August 1964.

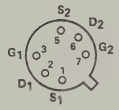
voltage-controlled resistor FETs *designed for . . .*

Siliconix

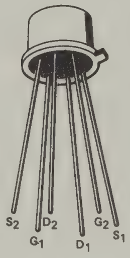
- **Small Signal Attenuators**
- **Filters**
- **Amplifier Gain Control**
- **Oscillator Amplitude Control**

TO-71
See Section 6





Bottom View



ABSOLUTE MAXIMUM RATING (25°C)

Gate-Drain or Gate-Source Voltage . . . . 25 V
Gate Current . . . . 10 mA
Total Device Dissipation at T_A = 25°C
(Derate at 2.0 mW/°C to 175°C) . . . . 300 mW
Storage Temperature Range . . . . −55 to +175°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Characteristic		VCR11N		Unit	Test Conditions	
			Min	Max			
1	I_{GSS}	Gate Reverse Current		-0.2	nA	V_{GS} = -15 V, V_{DS} = 0	
2	BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
3	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-8	-12		I_D = 1 μA, V_{DS} = 10 V	
4	$r_{ds(on)}$	Drain Source ON Resistance	100	200	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	C_{dgo}	Drain-Gate Capacitance		8	pF	V_{GD} = -10 V, I_S = 0	f = 1 MHz
6	C_{sgo}	Source-Gate Capacitance		8		V_{GS} = -10 V, I_D = 0	
7	$r_{DS}min / r_{DS}max$		.95	1	Ω	V_{DS} = 100 mV	r_{DS1} = 200Ω
			.95	1		$V_{GS1} = V_{GS2}$	r_{DS1} = 2kΩ

Note

1 V_{GS1} + Control Voltage necessary to force r_{DS}, to 200Ω or 2KΩ.

NSH*

*Contact factory for geometry information.

Introduction 1
Data Sheets 2
Selector Guides 3
Geometry 4
Application Notes 5
Appendices 6
Other Products 7
Worldwide Sales Offices 8

Tips on Selecting the Right FET for Your Application

The "Product Specification," a short form version of technical data, will provide you direct reference to Siliconix part numbers and a condensed version of technical specifications

IF YOU ARE NOT FAMILIAR WITH THE FET PARAMETERS YOU NEED:

1. Turn to page 3-4, "How to Choose the Correct FET for Your Application." Using this guide, determine the important FET parameters.
2. Next, turn to page 3-6, "JFET Geometry Selector Guide." Using this guide, choose the appropriate geometry.
3. Once you have chosen a geometry, turn to "Geometry Characteristics," section 4 of the catalog. Here you make the choice of a suitable part number.
4. Now that you have the part number, you will find complete electrical specifications of these products in the "Data Sheets," section 2 of the catalog.

IF YOU ARE FAMILIAR WITH THE PARAMETERS YOU NEED:

1. Turn to the "Product Specifications," pages 3-9 through 3-18 to determine the proper part number(s).
2. Double-check your choices against the data sheets, and select the part most suited for your application.

FET Application Selection Preferences

Additional Information

POPULAR PRODUCT TYPES	2N4117-9 2N4117A-19A PN4117-20, A	2N4338-41, J201-4 J304-5, 2N4867-9A, J230-2	2N4416, PN4416	2N3821-2, 2N4221-2 2N5457-9	U308-10, J308-10	J300, J210-2	J105-7, U290-1	2N5432-4 J108-10	2N4856-61, 2N4391-3 J111-13, PN4391-3	3N163, 4, MFE823	U421-U428
PROCESS DESIGNATION	**NT**	**NPA**	**NH**	**NRL**	**NZA**	**NZF**	**NVA**	**NIP**	**NCA**	**MRA**	**NNT**
Low Current Amplifier	P	S		S						P	P
Low Freq Amplifier ≤ 100 Hz		S		S						P	
High Freq Amplifier > 100 MHz			P		P	P					
HF ≥ 400 MHz Prime					P	S					
General Purpose Amplifier		P	P	P					P		
Low Noise Amp (10 Hz e_n)		P	S	S				S	P		
Low Noise Amp > 50 MHz			P	S	P	P					
High Frequency Mixer			P		P	P					
Dual Diff Pair											P
AGC Amplifier			P	P		P					
Electrometer Preamp	P										P
Microvolt Amplifier	P										P
Low Leakage Diode	P	S									
Low Leakage Dual Diode											P
Smoke Detector Input	P									P	
Battery Operated Amp < 1.5V	P	P									P
Diff/Single Ended Inp. Stag.											P
High Slew Rate Diff Amp											
Active Filter		S	P	P							
Oscillator		S	P	P	P	P					
Voltage Controlled Resistor		S	P	P					P		
Hybrid Chips	P	P	P	P					P		P
Analog/Digital Switch			S				P	P	P	S	
Multiplexing			P	S			S	S	P		
Choppers							P	P	P		
Reed Relay Replacement							P	P			
Sub pA Dual Diff Pair											P
Sample Hold			P	S					P		S
Buffer Interface to CMOS											
Matched Switch											
Current Limiter									P		
Current Source	S	S		LV							LV
High Voltage Protection Diode											

P = PRIME CHOICE
S = SECONDARY (ALTERNATIVE) CHOICE
LV = LIMITED VALUE

SMALL SIGNAL FET Application Selection Preferences

(Cont'd)

2N5196-9, 2N5515-24, 2N5545-7, 2N39548, U231-5	U401-6	2N5911-12, U440-1 U443-4	2N5902-9	2N5564-6, DN5564-6	2N5018-21, 2N5114-6 J174-7, VCR 3P	J500-J511	CRR0240-CRR0560 J553-7, J9100	CRR0800-CRR1250 CR068-CR150	CRR1450-CRR4300 CR160-CR470	SD210-SD215DE	JR135V-JR240V	M5911CHP-12CHP, M440CHP, M441CHP	M116
NQP	**NNR**	**NZFD**	**NTD**	**NCA-D**	**PSA**	**NCL**	**NKL**	**NKM**	**NKO**	**DMCB**	**VRMA**	**NNZ**	**MBN**
P	P		S										
P	P				S								
		P								P		P	
										P			
					P					S			
P	P			P									
		P		P								P	
P	P	P	S	S								P	
S	S		S										
P	P		S										
S			S										
P	P	P		P								P	
		P		P								P	
	P				P								
P	P		LV		P	P	P	P	P				
	S			S	P					P			P
					P					P			P
				P	P					P			P
										P			
			S										
S	S		S		P								S
					P								
S	P	S		P								S	
					P	P	P	P	P				
						P	P	P	P				
											P		

Small Signal FET Application/ Parameter Importance Guide

KEY PARAMETERS	BV_{GSS} (POV)	I_{GSS} (I_G)	I_D (off)	V_{GS1-2}/ V_{GS} (temp)	V_{GS} (off)	r_{DS}	I_{DSS}	g_{fso} (g_{fs} @ I_D)	g_{os}	High frequency Y parameters/P Gain	e_n (NF)	C_{iss}/C_{rss}	t_{on}/t_{off}
LIMIT	Min.	Max.	Max.	Max.	Min. Max.	Max.	Min. Max.	Min.	Max.	Min. Max.	Max.	Max.	Max.
Low Current Amplifier	*	*			/*		*	*	D		?	?	
Low Freq Amplifier ≤ 100 Hz	*	*			/*		*	*	D		?		
High Freq Amplifier > 100 MHz	*	*		/*		*	*	D	G		*		
HF ≥ 400 MHz Prime	*	D			/*		*	*	?	G		*	
General Purpose Amplifier	*	*			/*		*	*	D		?		
Low Noise Amp (10 Hz e_n)	*	*			/*		*	*		G		*	
Low Noise Amp > 50 MHz	*	*			/*		*	*	?	G		*	
High Frequency Mixer	*	D			?/*		*	*	?	G		D	
Dual Diff Pair	*	(*)		*	/*		*/D	(*)	*		?	D	
AGC Amplifier	*	*			*/*		*	*	?			D	
Electrometer Preamp	*	(*)			/*		*	*	D		?	D	
Microvolt Amplifier	*	*			/*		*	*	*		*	D	
Low Leakage Diode	*	*										?	
Low Leakage Dual Diode	*	*										?	
Smoke Detector Input	*	*			*/*		*/	*	?				
Battery Operated Amp < 1.5V	*	*			/*		*	*	D			D	
Diff/Single Enced Inp. Stag.	*	(*)		*	/*		*	(*)	D			?	
High Slew Rate Diff Amp	*	(*)		*	/*		*/	(*)	*			*	
Active filter	*	*			/*		*	*	?			D	
Oscillator	*	*			/*		*	*	?			*	
Voltage Controled Resistor	?	D			*/*	*						D	
Hybrid Chips	Same as application area												
Analog/Digital Switch	*	*	*			*	*/					*	*
Multiplexing	*	*	*			*	*/					*	*
Choppers	*	*	*			*	*/					*	*
Reed Relay Replacement	*	*	*			*	*/					?	*
Sub pA Dual Diff Pair	*	(*)		*	/*		*/	(*)	*		?	D	
Sample Hold	*	*	*		/*	*	*/					*	
Buffer Interface to CMOS	*								?				
Matched Switch	*	*	*			*	*/					*	*
Current Limiter	*						*/*		*				
Current Source	*						*/*		*				
High Voltage Protection Diode	*						*/*		*				

* - Important FET Parameter - Required
? - Important for some applications
D - Desired "nominal" limit - rarely critical
G - Guaranteed by C_{iss}, C_{rss}, g_{fs}, and device design

*/ - Indicates "Max"
/* - Indicates "Min"
(*) - Indicates Parameter in Parenthesis

Application	Detail Application	Important FET Parameters Required	Major Tradeoffs	Unimportant FET Parameters
AMPLIFIER	Audio	Low noise ($\overline{e}_n$), g_{fs}/g_{os}	Voltage amplification factor μ $= g_{fs}/g_{os}$ $= \Delta V_{DS}/\Delta V_{GS}$ @ I_D = const	$R_{DS(on)}$ $V_{DS(on)}$ $I_{D(off)}$ Switching Times
	Buffer	Low I_G, high g_{fs}		
	Differential	Good matching V_{GS}, g_{fs}, I_{DSS}, I_G		
	High Input Impedance	Very low I_G (eg., MOSFET)		
	High Frequency	High g_{fs}/C_{iss} ratio, NF, RF parameters		
	FET Input Op Amp	Good matching V_{GS}, g_{fs}, I_{DSS}, I_G		
	Low Distortion	High $V_{GS(off)}$ compared to signal amplitude		
	Low Supply Voltage	Low $V_{GS(off)}$		
	Low Noise	Low $\overline{e}_n$, $\overline{i}_n$, low 1/f noise, low NF		
	Preamplifier	Operate near I_{DZO}, high g_{fs}/I_D ratio		
	Video	High g_{fs}/C_{iss} ratio, NF		
SWITCHES	Analog Gates	Fast switching time	$R_{DS(on)}$ vs Capacitance	g_{fs} g_{os} I_{DSS} max
	Choppers	$r_{DS}/I_{D(off)}$ switching efficiency		
	Commutators	Low C_{rss}		
	Digital	Fast switching time		
	Integrator Reset	Very low $R_{DS(on)}$, High I_{DSS}		
	Sample and Hold	Low C_{rss}		
CONSTANT CURRENT SOURCE	Current Limiting	Low g_{oss}, low $V_{GS(off)}$, high BV_{GSS}	I_{DSS} vs BV_{GSS}	g_{fs}, $R_{DS(on)}$, $I_{D(off)}$, $V_{DS(on)}$ switching times, RF parameters capacitance
	Reference Current Source			
	Biasing			
VOLTAGE CONTROLLED RESISTORS	Gain Control	High $V_{GS(off)}$ for wide dynamic range and low distortion		g_{fs}, BV_{GSS}, I_{DSS}
	Amplitude Stability			
	Attenuators			
MIXERS	VHF	RF parameters, NF, high g_{fs}/C_{iss} ratio, low C_{rss}		$r_{DS(on)}$ $V_{DS(on)}$ $I_{D(off)}$
	UHF			
	Double Balanced	Matching characteristics		
OSCILLATORS	Class A	Good g_{fs} at operating frequency	g_{fs} vs Capacitance	
	Class C	Low C_{iss} for VHF operation		

<table>
<tr><th>Basic Circuit*</th><th>Preferred Parts</th></tr>
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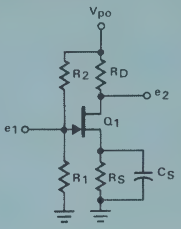

<table>
<tr><th>VDD (V)</th><th>RS Ω</th><th>R1 M℧</th><th>R2 M℧</th><th>CS NF</th><th>IDD mA</th><th>RD Ω</th><th>e0 (V)</th><th>AV</th></tr>
<tr><td rowspan="3">20</td><td>2K</td><td>4.7</td><td>11</td><td>100</td><td>5</td><td>1K</td><td>1.5</td><td>8-11</td></tr>
<tr><td>330</td><td>1</td><td>∞</td><td>100</td><td>8</td><td>820</td><td>1.5</td><td>9</td></tr>
<tr><td>330</td><td>1</td><td>∞</td><td>0</td><td>8</td><td>820</td><td>3</td><td>1.9</td></tr>
<tr><td rowspan="3">30</td><td>2K</td><td>4.7</td><td>11</td><td>100</td><td>6</td><td>2.7K</td><td>5</td><td>18-24</td></tr>
<tr><td>330</td><td>1</td><td>∞</td><td>100</td><td>8</td><td>1.5K</td><td>2.5</td><td>15</td></tr>
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<tr><td>VDD = 15
VSS = –15</td><td>4.7K</td><td>1</td><td colspan="2">Source Follower</td><td>5</td><td>0</td><td>11</td><td>0.97</td></tr>
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JFET Voltage Amplifier Stage Application Note: TA70-2
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J230-32
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J308-10
U308-10
U401-6
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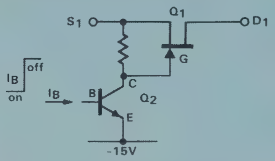

Shunt-Resistor Analog Switch Application Note: AN73-5
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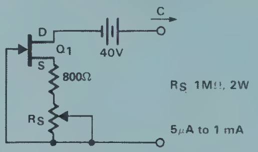

Equivalent Circuit of a JFET Current Limiter Application Note: DI71-1
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J552-7
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JR135V-240V</td></tr>
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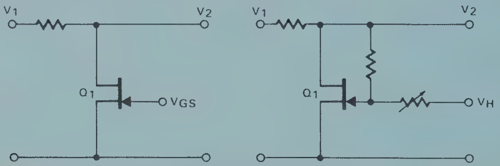

Distortion Free Voltage Controlled Attenuator (VCR) Application Note: AN73-1
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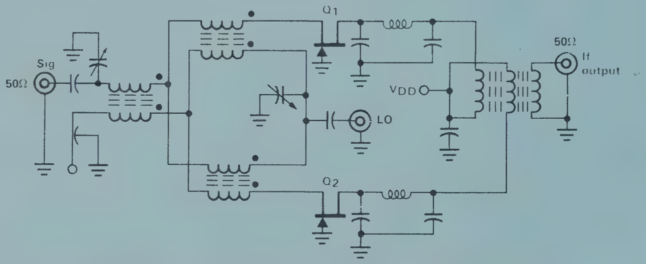

Single-Balanced VHF Balanced Mixer Application Note: AN72-1
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U308-10
J308-10
2N4416</td></tr>
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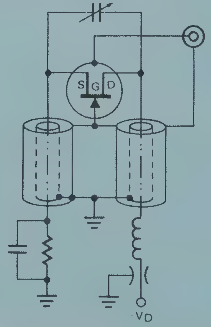

UHF Transmission Line Oscillator Application Note: DI73-2
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PN4416
U308-10
J308-10</td></tr>
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*for further details see Application Notes, Index 5

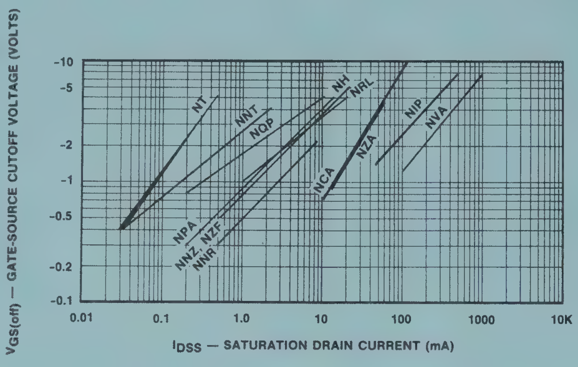
JFET Geometry Selector Guide

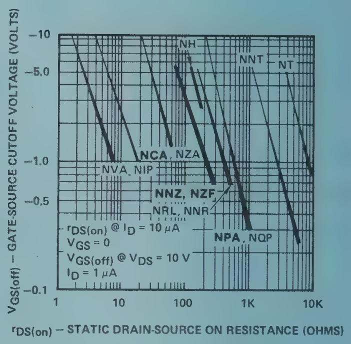
USEFUL JFET INFORMATION

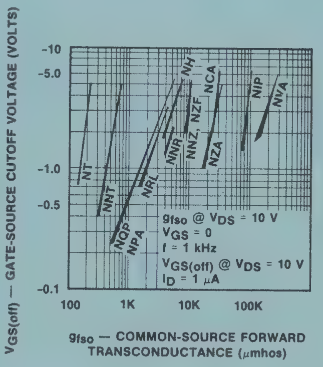
C_{iss}	=	$C_{qs} + C_{gd}$	Input Capacitance
C_{OSS}	=	$C_{ds} + C_{gs} + C_{bd}$	Output Capacitance
C_{RSS}	=	C_{qd}	Reverse Feedback Capacitance
I_{DZ}	=	$I_{DSS}\left(\frac{0.63}{V_{GS(off)}}\right)^2$	Variation of $I_{(zero\ tc)}$ with Gate Source Cutoff Voltage
g_{fso}	=	$K\frac{I_{DSS}}{V_{GS(off)}}$	Forward transconductance as a function of I_{DSS} and $V_{GS(off)}$ at zero gate-source voltage (K = 1.5 to 2.5; typically = 2 for N-channel junction FET)
g_{fs}	=	$g_{fso}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$	Variation of g_{fs} with gate bias
g_{fs}	=	$g_{fso}\sqrt{I_D/I_{DSS}}$	Variation of g_{fs} with drain current
$V_{GS(off)}$	=	$\frac{2\,I_{DSS}}{g_{fso}}$	Gate-Source cutoff voltage in terms of I_{DSS} and g_{fso}
V_{DS}	≈	$V_{GS(off)}\left(\frac{I_D}{I_{DSS}}\right)^{1/2}$	Drain voltage at which drain current saturates
r_{DS}	≃	$\frac{1}{g_{fs}}$	Reciprocal relationship between drain-source resistance and forward transconductance. Accurate when $V_{DS} < V_{GS(off)}$ i.e. in the triode region
r_{DS}	≃	$\frac{[V_{GS(off)}]^2}{KI_{DSS}\,[V_{GS(off)} - V_{GS}]}$	K = 1.5 to 2.5 Variation of drain resistance in the triode region
I_D	=	$I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$	Variation of drain current with gate-source voltage. The square law transfer characteristic.

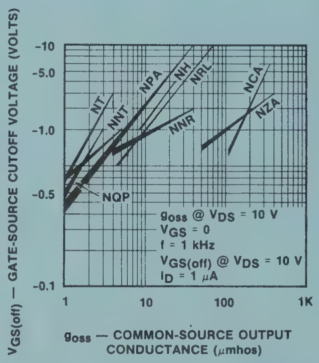
JFET Geometry Selector Guide (Cont'd)

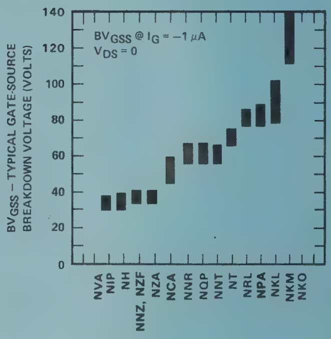
N-Channel JFETs

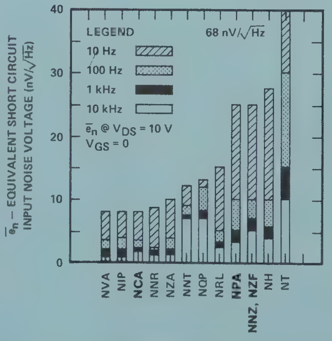


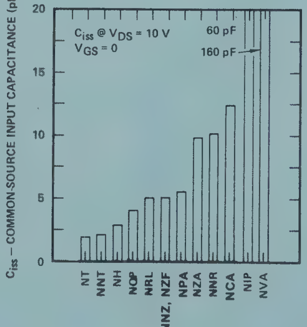


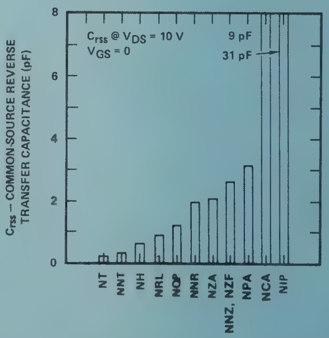






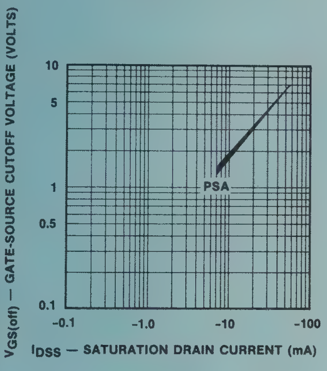


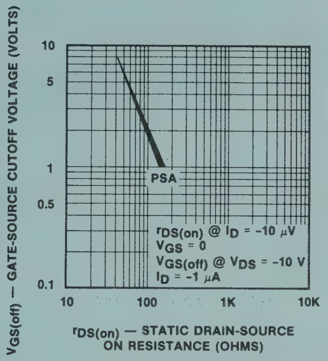


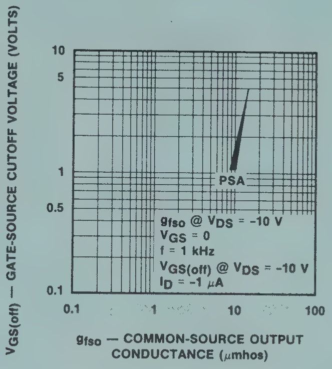


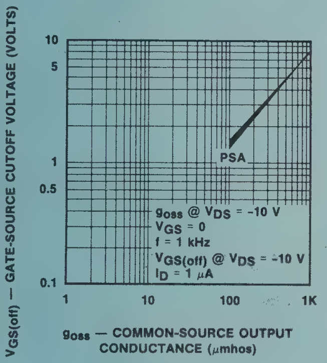
JFET Geometry Selector Guide (Cont'd)

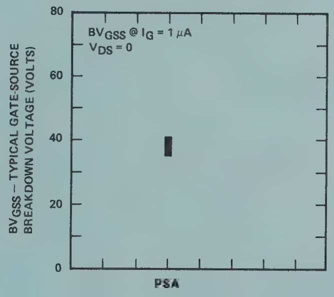
P-Channel JFETs

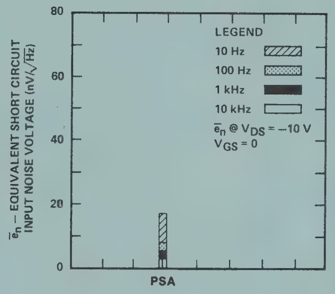


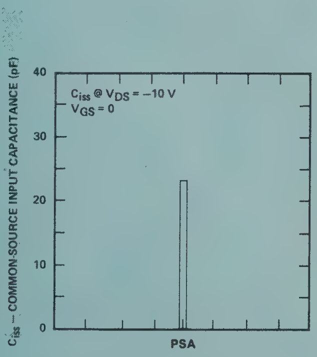


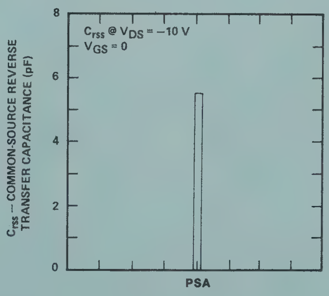












Product Specifications

N & P-Channel Single FETs

DEVICE	GEOMETRY (Section 4)	RESISTANCE Chnl Ω, Max.	RESISTANCE Gate Ω	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	INPUT CAPACITANCE (pF, MAX.)	TRANS-CONDUCTANCE gfs (μmhos) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	SATURATION CURRENT (mA) Max.	SATURATION CURRENT (mA) Min.	BREAKDOWN VOLTAGE (V, MAX.)	THRESHOLD VOLTAGE (V, MAX.)	LEAKAGE (nA, MAX.) Chnl	LEAKAGE (nA, MAX.) Gate	PACKAGE (TO-)	N or P	PART NUMBER
LOW LEAKAGE	NT	—	—	—	3	210	70	0.09	0.03	40	1.8	—	0.01	72	N	2N4117
	NT	—	—	—	3	210	70	0.09	0.03	40	1.8	—	0.001	72	N	2N4117A
	NT	—	—	—	3	250	80	0.24	0.08	40	3.0	—	0.01	72	N	2N4118
	NT	—	—	—	3	250	90	0.24	0.08	40	3.0	—	0.001	72	N	2N4118A
	NT	—	—	—	3	330	100	0.6	0.2	40	6.0	—	0.01	72	N	2N4119
	NT	—	—	—	3	330	100	0.6	0.2	40	6.0	—	0.001	72	N	2N4119A
	NT	3K	—	—	—	210	70	0.09	0.03		−40		0.01	92	N	PN4117
	NT	3K	—	—	—	210	70	0.09	0.03		−40		0.001	92	N	PN4117A
	NT	3K	—	—	—	250	80	0.24	0.08		−40		0.01	92	N	PN4118
	NT	3K	—	—	—	250	80	0.24	0.08		−40		0.001	92	N	PN4118A
	NT	3K	—	—	—	330	100	0.6	0.2		−40		0.01	92	N	PN4119
	NT	3K	—	—	—	330	100	0.6	0.2		−40		0.001	92	N	PN4119A
	NT	3K	—	—	—	330	100	0.6	0.2		−40		—	92	N	PN4120
	NT	3K	—	—	—	210	70	0.09	0.03		−40		0.005	72	N	FN4117
	NT	—	—	—	3	210	70	0.2	0.03	40	2.0		0.001	72	N	FN4117A
	NT	3K	—	—	—	250	80	0.24	0.08		−40		0.005	72	N	FN4118
	NT	—	—	—	3	250	80	0.4	0.08	40	2.0		0.001	72	N	FN4118A
	NT	3K	—	—	—	330	100	0.6	0.2		−40		0.005	72	N	FN4119
	NT	—	—	—	3	330	100	1.2	0.2	40	6.0		0.001	72	N	FN4119A
	NCA	14	60	—	—		—	100	25		40	0.1	0.1	18	N	FN4392
	NCA	14	100	—	—		—	60	5.0		40	0.1	0.1	18	N	FN4393
LOW NOISE	NRL	—	1M	2.5	6	4000	1000	3.0	0.5	30	4.0	—	0.1	72	N	2N4220A
	NRL	—	1M	2.5	6	5000	2000	6.0	2.0	30	6.0	—	0.1	72	N	2N4221A
	NRL	—	1M	2.5	6	6000	2500	15	5.0	30	8.0	—	0.1	72	N	2N4222
	NPA	—	1M	1.0	7	1800	600	0.6	0.2	50	1.0	—	0.1	18	N	2N4338
	NPA	—	1M	1.0	7	2400	800	1.5	0.5	50	1.8	—	0.1	18	N	2N4339
	NPA	—	1M	1.0	7	3000	1300	3.6	1.2	50	3.0	—	0.1	18	N	2N4340
	NPA	—	1M	1.0	7	4000	2000	9.0	3.0	50	6.0	—	0.1	18	N	2N4341
	NPA	—	—	20	25	2000	700	1.2	0.4	40	2.0	—	0.25	72	N	2N4867
	NPA	—	—	10	25	2000	700	1.2	0.4	40	2.0	—	0.25	72	N	2N4867A
	NPA	—	—	20	25	3000	1000	3.0	1.0	40	3.0	—	0.25	72	N	2N4868
	NPA	—	—	10	25	3000	1000	3.0	1.0	40	3.0	—	0.25	72	N	2N4868A
	NPA	—	—	20	25	4000	1300	7.5	2.5	40	5.0	—	0.25	72	N	2N4869
	NPA	—	—	10	25	4000	1300	7.5	2.5	40	5.0	—	0.25	72	N	2N4869A
	NPA	—	—	30	—	2500	1000	3.0	0.7	40	3.0	—	0.25	92	N	J230
	NPA	—	—	30	—	2500	1000	3.0	0.7	40	3.0	—	0.25	92	N	J230-18
	NPA	—	—	30	—	3000	1500	6.0	2.0	40	5.0	—	0.25	92	N	J231
	NPA	—	—	30	—	3000	1500	6.0	2.0	40	5.0	—	0.25	92	N	J231-18
	NPA	—	—	30	—	4000	2500	10	5.0	40	6.0	—	0.25	92	N	J232

Product Specifications (Cont'd)

N & P-Channel Single FETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)		THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS-CONDUCTANCE gfs (μmhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE		GEOMETRY (Section 4)	DEVICE
			Gate	Chnl			Min.	Max.	Min.	Max.			Gate Ω	Chnl Ω, Max.		
J232-18	N	92	0.25	—	6.0	40	5.0	10	2500	4000	—	30	—	—	NPA	RF AMPLIFIERS
J270-18	P	92	0.2	—	2.0	30	2.0	15	6000	15000	—	—	—	—	PSA	
2N3819	N	92	2.0	—	8.0	25	2.0	20	2000	6500	8.0	—	—	—	NRL	
2N3823	N	72	0.5	—	8.0	30	4.0	20	3500	6500	6	2.5	1K	—	NRL	
2N4223	N	72	0.25	—	8.0	30	3.0	18	3000	7000	6	5.0	1K	—	NRL	
2N4224	N	72	0.5	—	8.0	30	2.0	20	2000	7500	6	—	—	—	NRL	
2N4416	N	72	0.1	—	6.0	30	5.0	15	4500	7500	4	2.0	1K	—	NH	
2N4416A	N	72	0.1	—	6.0	35	5.0	15	4500	7500	4	2.0	1K	—	NH	
2N5078	N	72	0.25	—	8.0	30	4.0	25	4500	10000	6	3.0	1K	—	—	
2N5484	N	92	1.0	—	3.0	25	1.0	5.0	3000	6000	5	3.0	1K	—	NH	
2N5485	N	92	1.0	—	4.0	25	4.0	10	3500	7000	5	2.0	1K	—	NH	
2N5486	N	92	1.0	—	6.0	25	8.0	20	4000	8000	5	2.0	1K	—	NH	
2N5668	N	92	2.0	—	4.0	25	1.0	5.0	1500	6500	7	2.5	1K	—	NH	
2N5669	N	92	2.0	—	6.0	25	4.0	10	2000	6500	7	2.5	1K	—	NH	
2N5670	N	92	2.0	—	8.0	25	8.0	20	3000	7500	7.0	2.5	1K	—	NH	
J210	N	92	0.1	—	3.0	25	2.0	15	4000	12000	—	—	—	—	NZF	
J211	N	92	0.1	—	4.5	25	7.0	20	7000	12000	—	—	—	—	NZF	
J212	N	92	0.1	—	6.0	25	15	40	7000	12000	—	—	—	—	NZF	
J270	P	92	0.2	—	2.0	30	2.0	15	6000	15000	—	—	—	—	PSA	
J271	P	92	0.2	—	4.5	30	6.0	50	8000	18000	—	—	—	—	PSA	
J300	N	92	0.5	—	6.0	25	6.0	30	4500	9000	5.5	—	—	—	NZF	
J304	N	92	0.1	—	6.0	30	5.0	15	4500	7500	—	—	—	—	NH	
J305	N	92	0.1	—	3.0	30	1.0	8.0	3000	—	—	—	—	—	NH	
J308	N	92	1.0	—	6.5	25	12	60	8000	20000	7.5	—	—	—	NZA	
J309	N	92	1.0	—	4.0	25	12	30	10000	20000	7.5	—	—	—	NZA	
J310	N	92	1.0	—	6.5	25	24	60	8000	18000	7.5	—	—	—	NZA	
PN4416	N	92	1.0	—	6.0	30	5.0	15	4500	7500	4.0	2.0	1K	—	NH	
MPF102	N	92	2.0	—	7.5	25	2.0	20	2000	7500	7.0	—	—	—	NH	
MPF108	N	92	1.0	—	8.0	25	1.5	24	2000	7500	6.5	2.5	1M	—	NH	
MPF112	N	92	100	—	10	25	1.0	25	1000	7500	—	—	—	—	NH	
U308	N	52	0.15	—	6.0	25	12	60	10000	20000	7.5	—	—	—	NZA	
U309	N	52	0.15	—	4.0	25	12	30	10000	20000	7.5	—	—	—	NZA	
U310	N	52	0.15	—	6.0	25	24	60	10000	18000	7.5	—	—	—	NZA	
U311	N	72	0.15	—	6.0	25	20	60	10000	20000	7.5	—	—	—	NZA	
U312	N	52	0.1	—	6.0	25	10	30	6000	10000	5.0	—	—	—	NZF	

Product Specifications (Cont'd)

N & P-Channel Single FETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.) Gate	LEAKAGE (nA, MAX.) Chnl	THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA) Min.	SATURATION CURRENT (mA) Max.	TRANS-CONDUCTANCE gfs (µmhos) Min.	TRANS-CONDUCTANCE gfs (µmhos) Max.	INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE Gate Ω	RESISTANCE Chnl Ω, Max.	GEOMETRY (Section 4)	DEVICE
U1837	N	92	0.25	–	8.0	30	4.0	25	4500	10000	6.0	3.0	1K	–	NH	RF AMP
U1837-18	N	92	0.25	–	8.0	30	4.0	25	4500	10000	6.0	2.0	1K	–	NH	
2N3824	N	72	0.1	0.1	8.0	50	–	–	–	–	6.0	–	–	250	NCA	SWITCHES & CHOPPERS
2N3966	N	72	0.1	1.0	6.0	30	2.0	–	–	–	6.0	–	–	220	NCA	
2N3970	N	18	0.25	0.25	10	40	50	150	–	–	25	–	–	30	NCA	
2N3971	N	18	0.25	0.25	5.0	40	25	75	–	–	25	–	–	60	NCA	
2N3972	N	18	0.25	0.25	3.0	40	5.0	30	–	–	25	–	–	100	NCA	
2N4091	N	18	0.2	0.2	10	40	30	–	–	–	16	–	–	30	NCA	
2N4092	N	18	0.2	0.2	7.0	40	15	–	–	–	16	–	–	50	NCA	
2N4093	N	18	0.2	0.2	5.0	40	8.0	–	–	–	16	–	–	80	NCA	
2N4391	N	18	0.1	0.1	10	40	50	150	–	–	14	–	–	30	NCA	
2N4392*	N	18	0.1	0.1	5.0	40	25	75	–	–	14	–	–	60	NCA	
2N4393*	N	18	0.1	0.1	3.0	40	5.0	30	–	–	14	–	–	100	NCA	
2N4856	N	18	0.25	0.25	10	40	50	–	–	–	18	–	–	25	NCA	
2N4856A	N	18	0.25	0.25	10	40	50	–	–	–	10	–	–	25	NCA	
2N4857	N	18	0.25	0.25	6.0	40	20	100	–	–	18	–	–	40	NCA	
2N4857A	N	18	0.25	0.25	6.0	40	20	100	–	–	10	–	–	40	NCA	
2N4858	N	18	0.25	0.25	4.0	40	8.0	80	–	–	18	–	–	60	NCA	
2N4858A	N	18	0.25	0.25	4.0	40	8.0	80	–	–	10	–	–	60	NCA	
2N4859	N	18	0.25	0.25	10	30	50	–	–	–	18	–	–	25	NCA	
2N4859A	N	18	0.25	0.25	10	30	50	–	–	–	10	–	–	25	NCA	
2N4860	N	18	0.25	0.25	6.0	30	20	100	–	–	18	–	–	40	NCA	
2N4860A	N	18	0.25	0.25	6.0	30	20	100	–	–	10	–	–	40	NCA	
2N4861	N	18	0.25	0.25	4.0	30	8.0	80	–	–	18	–	–	60	NCA	
2N4861A	N	18	0.25	0.25	4.0	30	8.0	80	–	–	10	–	–	60	NCA	
2N5018	P	18	2.0	10.0	10	30	10	–	–	–	45	–	–	75	PSA	
2N5019	P	18	2.0	10.0	5.0	30	5.0	–	–	–	45	–	–	150	PSA	
2N5114	P	18	0.5	0.5	10	30	30	90	–	–	25	–	–	75	PSA	
2N5115	P	18	0.5	0.5	6.0	30	15	60	–	–	25	–	–	100	PSA	
2N5116	P	18	0.5	0.5	4.0	30	5.0	25	–	–	25	–	–	150	PSA	
2N5432	N	52	0.2	0.2	10	25	150	–	–	–	30	–	–	5.0	NIP	
2N5433	N	52	0.2	0.2	9.0	25	100	–	–	–	30	–	–	7.0	NIP	
2N5434	N	52	0.2	0.2	4.0	25	30	–	–	–	30	–	–	10	NIP	
2N5638	N	92	1.0	1.0	12	30	50	–	–	–	10	–	–	30	NCA	
2N5639	N	92	1.0	1.0	8.0	30	25	–	–	–	10	–	–	60	NCA	

*FN4392 and FN4393 available

Product Specifications (Cont'd)

N & P-Channel Single FETs

DEVICE SWITCHES & CHOPPERS

PART NUMBER	GEOMETRY (Section 4)	RESISTANCE		NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	INPUT CAPACITANCE (pF, MAX.)	TRANS-CONDUCTANCE gfs (μmhos)		SATURATION CURRENT (mA)		BREAKDOWN VOLTAGE (V, MAX.)	THRESHOLD VOLTAGE (V, MAX.)	LEAKAGE (nA, MAX.)		PACKAGE (TO-)	N or P
		Chnl Ω, Max.	Gate Ω			Max.	Min.	Max.	Min.			Chnl	Gate		
2N5640	NCA	100	—	—	10	—	—	—	5.0	30	6.0	1.0	1.0	92	N
2N5653	NCA	50	—	—	10	—	—	—	40	30	12	1.0	1.0	92	N
2N5654	NCA	100	—	—	10	—	—	—	15	30	8.0	1.0	1.0	92	N
J105	NVA	3.0	—	—	—	—	—	—	500	25	10.0	3.0	3.0	92	N
J105-18	NVA	3.0	—	—	—	—	—	—	500	25	10	3.0	3.0	92	N
J106	NVA	6.0	—	—	—	—	—	—	200	25	6.0	3.0	3.0	92	N
J106-18	NVA	6.0	—	—	—	—	—	—	200	25	6.0	3.0	3.0	92	N
J107	NVA	8.0	—	—	—	—	—	—	100	25	4.5	3.0	3.0	92	N
J107-18	NVA	8.0	—	—	—	—	—	—	100	25	4.5	3.0	3.0	92	N
J108	NIP	8.0	—	—	—	—	—	—	80	25	10	3.0	3.0	92	N
J108-18	NIP	8.0	—	—	—	—	—	—	80	25	10	3.0	3.0	92	N
J109	NIP	12	—	—	—	—	—	—	40	25	6.0	3.0	3.0	92	N
J109-18	NIP	12	—	—	—	—	—	—	40	25	6.0	3.0	3.0	92	N
J110	NIP	18	—	—	—	—	—	—	10	25	4.0	3.0	3.0	92	N
J110-18	NIP	18	—	—	—	—	—	—	10	25	4.0	3.0	3.0	92	N
J111	NCA	30	—	—	—	—	—	—	20	35	10	1.0	1.0	92	N
J111-18	NCA	30	—	—	—	—	—	—	20	35	10	1.0	1.0	92	N
J112	NCA	50	—	—	—	—	—	—	5.0	35	5.0	1.0	1.0	92	N
J112-18	NCA	50	—	—	—	—	—	—	5.0	35	5.0	1.0	1.0	92	N
J113	NCA	100	—	—	—	—	—	—	2.0	35	3.0	1.0	1.0	92	N
J113-18	NCA	100	—	—	—	—	—	—	2.0	35	3.0	1.0	1.0	92	N
J174	PSA	85	—	—	—	—	—	100	20	30	10	1.0	1.0	92	P
J174-18	PSA	85	—	—	—	—	—	100	20	30	10	1.0	1.0	92	P
J175	PSA	125	—	—	—	—	—	60	7.0	30	6.0	1.0	1.0	92	P
J175-18	PSA	125	—	—	—	—	—	60	7.0	30	6.0	1.0	1.0	92	P
J176	PSA	250	—	—	—	—	—	25	2.0	30	4.0	1.0	1.0	92	P
J176-18	PSA	250	—	—	—	—	—	25	2.0	30	4.0	1.0	1.0	92	P
J177	PSA	300	—	—	—	—	—	20	1.5	30	2.25	1.0	1.0	92	P
J177-18	PSA	300	—	—	—	—	—	20	1.5	30	2.25	1.0	1.0	92	P
PN4391	NCA	30	—	—	14	—	—	150	50	40	10	1.0	1.0	92	N
PN4391-18	NCA	30	—	—	14	—	—	150	50	40	10	1.0	1.0	92	N
PN4392	NCA	60	—	—	14	—	—	100	25	40	5.0	1.0	1.0	92	N
PN4392-18	NCA	60	—	—	14	—	—	100	25	40	5.0	1.0	1.0	92	N
PN4393	NCA	100	—	—	14	—	—	60	5.0	40	3.0	1.0	1.0	92	N
PN4393-18	NCA	100	—	—	14	—	—	60	5.0	40	3.0	1.0	1.0	92	N
P1086	PSA	75	—	—	45	—	—	—	10	30	10	10.0	2.0	92	P
P1086-18	PSA	75	—	—	45	—	—	—	10	30	10	10.0	2.0	92	P

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FET Product Specifications (Cont'd)

N & P-Channel Single FETs

DEVICE		SWITCHES & CHOPPERS																						GENERAL PURPOSE
GEOMETRY (Section 4)		PSA	PSA	DMCB-B	DMCB-A	DMCB-B	DMCB-A	DMCB-B	DMCB-A	NCA	NCA	NCA	NVA	NVA	PSA	PSA	PSA	NCA	NCA	NCA	NCA	NCA	NCA	
RESISTANCE	Chnl Ω, Max.	150	150	70	70	70	70	70	70	150	75	50	2.5	7.0	85	110	175	30	30	50	50	80	80	—
	Gate Ω	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	1M
NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	3
INPUT CAPACITANCE (pF, MAX.)		45	45	3.5	3.5	3.5	3.5	3.5	3.5	30	30	30	60	60	27	27	27	16	16	16	16	16	16	30
TRANS-CONDUCTANCE gfs (μmhos)	Max.	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Min.	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	2500
SATURATION CURRENT (mA)	Max.	—	—	—	—	—	—	—	—	25	75	150	—	—	90	60	25	—	—	—	—	—	—	10.0
	Min.	5.0	5.0	10	10	10	10	10	10	3.0	15	30	500	200	30	15	5.0	30	30	15	15	8.0	8.0	2.0
BREAKDOWN VOLTAGE (V, MAX.)		30	30	30	30	10	10	20	20	30	30	30	30	30	30	30	30	40	40	40	40	40	40	30
THRESHOLD VOLTAGE (V, MAX.)		5.0	5.0	2.0	2.0	2.0	2.0	2.0	2.0	3.0	5.0	10	10	4.5	10	6.0	4.0	10	10	7.0	7.0	5.0	5.0	4.0
LEAKAGE (nA, MAX.)	Chnl	10.0	10.0	100	100	100	100	100	100	1.0	1.0	1.0	1.0	1.0	0.5	0.5	0.5	0.2	0.2	0.2	0.2	0.2	0.2	—
	Gate	2.0	2.0	100	100	100	100	100	100	1.0	1.0	1.0	1.0	1.0	0.5	0.5	0.5	0.4	0.4	0.4	0.4	0.4	0.4	30
PACKAGE (TO-)		92	92	72	72	72	72	72	72	18	18	18	52	52	18	18	18	92	92	92	92	92	92	
N or P		P	P	N	N	N	N	N	N	N	N	N	N	N	P	P	P	N	N	N	N	N	N	P
PART NUMBER		P1087	P1087-18	SD210	SD211	SD212	SD213	SD214	SD215	U200	U201	U202	U290	U291	U304	U305	U306	U1897	U1897-18	U1898	U1898-18	U1899	U1899-18	2N2609

Product Specifications (Cont'd)

N & P-Channel Single FETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA; MAX.) Gate	LEAKAGE (nA; MAX.) Chnl	THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA) Min.	SATURATION CURRENT (mA) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	TRANS-CONDUCTANCE gfs (μmhos) Max.	INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE Gate Ω	RESISTANCE Chnl Ω, Max.	GEOMETRY (Section 4)	DEVICE
2N3821	N	72	0.1	–	4.0	50	0.5	2.5	1500	4500	6	200	–	–	NRL	GENERAL PURPOSE
2N3822	N	72	0.1	–	6.0	50	2.0	10	3000	6500	6	200	–	–	NRL	
2N4220	N	72	0.1	–	4.0	30	0.5	3.0	1000	4000	6	–	–	–	NRL	
2N4221	N	72	0.1	–	6.0	30	2.0	6.0	2000	5000	6	–	–	–	NRL	
2N4222	N	72	0.1	–	8.0	30	5.0	15	2500	6000	6	–	–	–	NRL	
2N5457	N	92	1.0	–	6.0	25	1.0	5.0	1000	5000	7	3.0	1M	–	NRL	
2N5458	N	92	1.0	–	7.0	25	2.0	9.0	1500	5500	7	3.0	1M	–	NRL	
2N5459	N	92	1.0	–	8.0	25	4.0	16	2000	6000	7	3.0	100M	–	NRL	
J201	N	92	0.1	–	1.5	40	0.2	1.0	500	–	5.0	–	–	–	NPA	
J201-18	N	92	0.1	–	1.5	40	0.2	1.00	500	–	5.0	–	–	–	NPA	
J202	N	92	0.1	–	4.0	40	0.9	4.5	1000	–	5.0	–	–	–	NPA	
J202-18	N	92	0.1	–	4.0	40	0.9	4.5	1000	–	5.0	–	–	–	NPA	
J203	N	92	0.1	–	10	40	4.0	20	1500	–	5.0	–	–	–	NPA	
J203-18	N	92	0.1	–	10	40	4.0	20	1500	–	5.0	–	–	–	NPA	
J204	N	92	0.1	–	2.0	25	1.2	3.0	–	–	5.0	–	–	–	NPA	
J204-18	N	92	0.1	–	2.0	25	1.2	3.0	–	–	5.0	–	–	–	NPA	
J270	P	92	0.2	–	4.5	30	6.0	50	8000	18000	–	–	–	–	PSA	
J271-18	P	92	0.2	–	4.5	30	6.0	50	8000	18000	–	–	–	–	PSA	
PN4302	N	92	1.0	–	4.0	30	0.5	5.0	1000	–	6	2.0	1M	–	NPA	
PN4302-18	N	92	1.0	–	4.0	30	0.5	5.0	1000	–	6.0	2.0	1M	–	NPA	
PN4303	N	92	1.0	–	6.0	30	4.0	10	2000	–	6	2.0	1M	–	NPA	
PN4303-18	N	92	1.0	–	6.0	30	4.0	10	2000	–	6.0	2.0	1M	–	NPA	
PN4304	N	92	1.0	–	10.0	30	0.5	15	1000	–	6	3.0	1M	–	NPA	
PN4304-18	N	92	1.0	–	10	30	0.5	15	1000	–	6.0	2.0	1M	–	NPA	
PN5163	N	92	10	–	8.0	25	1.0	40.0	2000	9000	20	50.0	–	–	–	
MPF109	N	92	1.0	–	8.0	25	0.5	24	800	6000	7.0	2.5	1M	–	NRL	
MPF111	N	92	100	–	10	20	0.5	20	500	–	–	–	–	–	NRL	

Product Specifications (Cont'd)

N-Channel Dual FETs

DEVICE	GEOMETRY (Section 4)	OUTPUT CONDUCTANCE gos (μmhos, MAX.)	THRESHOLD Temp Tracking μV/°C	THRESHOLD Static Match (mV, Max.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	INPUT CAPACITANCE (pF, MAX.)	TRANS-CONDUCTANCE gfs (μmhos) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	SATURATION CURRENT (mA) Max.	SATURATION CURRENT (mA) Min.	BREAKDOWN VOLTAGE (V, MAX.)	THRESHOLD VOLTAGE (V, MAX.)	LEAKAGE (nA, MAX.) Gate	PACKAGE (TO-)	N or P	PART NUMBER
LOW LEAKAGE	NQP	50	5.0	5.0	20	6.0	—	1000	7.0	0.7	50	4.0	0.025	71	N	2N5196
	NQP	50	10	5.0	20	6.0	—	1000	7.0	0.7	50	4.0	0.025	71	N	2N5197
	NQP	50	20	10	20	6.0	—	1000	7.0	0.7	50	4.0	0.025	71	N	2N5198
	NQP	50	40	15	20	6.0	—	1000	7.0	0.7	50	4.0	0.025	71	N	2N5199
	NQP	25	10	5.0	200	6.0	—	1500	8.0	0.5	50	4.5	0.1	71	N	2N5545
	NQP	25	20	10	200	6.0	—	1500	8.0	0.5	50	4.5	0.1	71	N	2N5546
	NQP	25	40	15	200	6.0	—	1500	8.0	0.5	50	4.5	0.1	71	N	2N5547
	NQP	1.0	5.0	5.0	0.2	3.0	—	70	0.5	0.03	40	4.5	0.005	78	N	2N5902
	NT	1.0	10	5.0	0.2	3.0	—	70	0.5	0.03	40	4.5	0.005	78	N	2N5903
	NT	1.0	20	10	0.2	3.0	—	70	0.5	0.03	40	4.5	0.005	78	N	2N5904
	NT	1.0	40	15	0.2	3.0	—	70	0.5	0.03	40	4.5	0.005	78	N	2N5905
	NT	1.0	5.0	5.0	0.1	3.0	—	70	0.5	0.03	40	4.5	0.002	78	N	2N5906
	NT	1.0	10	5.0	0.1	3.0	—	70	0.5	0.03	40	4.5	0.002	78	N	2N5907
	NT	1.0	20	10	0.1	3.0	—	70	0.5	0.03	40	4.5	0.002	78	N	2N5908
	NT	1.0	20	15	0.1	3.0	—	70	0.5	0.03	40	4.5	0.002	78	N	2N5909
	NNR	2.0	10	5.0	20	8.0	—	2000	10	0.5	50	2.5	0.025	71	N	U401
	NNR	2.0	10	10	20	8.0	—	2000	10	0.5	50	2.5	0.025	71	N	U402
	NNR	2.0	25	10	20	8.0	—	2000	10	0.5	50	2.5	0.025	71	N	U403
	NNR	2.0	25	15	20	8.0	—	2000	10	0.5	50	2.5	0.025	71	N	U404
	NNR	2.0	40	20	20	8.0	—	2000	10	0.5	50	2.5	0.025	71	N	U405
	NNR	2.0	80	40	20	8.0	—	2000	10	0.5	50	2.5	0.025	71	N	U406
	NNT	0.5	10	10	10	3.0	1500	300	1.0	0.06	40	2.0	0.001	78	N	U421
	NNT	0.5	25	15	10	3.0	1500	300	1.0	0.06	40	2.0	0.001	78	N	U422
	NNT	0.5	40	25	10	3.0	1500	300	1.0	0.06	40	2.0	0.001	78	N	U423
	NNT	1.0	10	10	10	3.0	1500	300	1.8	0.06	40	3.0	0.003	78	N	U424
	NNT	1.0	25	15	10	3.0	1500	300	1.8	0.06	40	3.0	0.003	78	N	U425
	NNT	1.0	40	25	10	3.0	1500	300	1.8	0.06	40	3.0	0.003	78	N	U426
	NNT	3.0	40	25	—	3.0	—	250	1.8	0.06	40	2.0	0.005	78	N	U427
	NNT	5.0	80	40	—	3.0	—	250	1.8	0.06	40	3.0	0.005	78	N	U428
LOW NOISE	NQP	1.0	5.0	5.0	30	25	—	1000	7.5	0.5	40	4.0	0.25	71	N	2N5515
	NQP	1.0	10	5.0	30	25	—	1000	7.5	0.5	40	4.0	0.25	71	N	2N5516
	NQP	1.0	20	10	30	25	—	1000	7.5	0.5	40	4.0	0.25	71	N	2N5517
	NQP	1.0	40	15	30	25	—	1000	7.5	0.5	40	4.0	0.25	71	N	2N5518
	NQP	1.0	80	15	30	25	—	1000	7.5	0.5	40	4.0	0.25	71	N	2N5519
	NQP	1.0	5.0	5.0	15	25	—	1000	7.5	0.5	40	4.0	0.25	71	N	2N5520
	NQP	1.0	10	5.0	15	25	—	1000	7.5	0.5	40	4.0	0.25	71	N	2N5521
	NQP	1.0	20	10	15	25	—	1000	7.5	0.5	40	4.0	0.25	71	N	2N5522
	NQP	1.0	40	15	15	25	—	1000	7.5	0.5	40	4.0	0.25	71	N	2N5523
	NQP	1.0	80	15	15	25	—	1000	7.5	0.5	40	4.0	0.25	71	N	2N5524
	NNR	2.0	10	5.0	20	8.0	—	2000	10	0.5	50	2.5	0.025	71	N	U401
	NNR	2.0	10	10	20	8.0	—	2000	10	0.5	50	2.5	0.025	71	N	U402

Product Specifications (Cont'd)

N-Channel Dual FETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.) Gate	THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA) Min.	SATURATION CURRENT (mA) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	TRANS-CONDUCTANCE gfs (μmhos) Max.	INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/$\sqrt{Hz}$, MAX.) or (NF, dB, MAX.)	THRESHOLD Static Match (mV, Max.)	THRESHOLD Temp Tracking μV/°C	OUTPUT CONDUCTANCE gos (μmhos, MAX.)	GEOMETRY (Section 4)	DEVICE
U404	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	15	25	2.0	NNR	LOW NOISE
U405	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	20	40	2.0	NNR	
U406	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	40	80	2.0	NNR	
2N5911	N	78	0.1	5.0	25	7.0	40	5000	—	3.0	20	10	20	100	NZF	RF AMPLIFIER
2N5912	N	78	0.1	5.0	25	7.0	40	5000	—	3.0	20	15	40	100	NZF	
U257	N	78	0.1	5.0	25	5.0	40	5000	—	5.0	30	100	—	150	NZF	
U430	N	99	0.15	4.0	25	12	30	10000	—	7.5	12	—	—	150	NZA	
U431	N	99	0.15	6.0	25	24	60	10000	—	7.5	10	—	—	150	NZA	
U440	N	71	0.50	6.0	25	6.0	30	4500	—	3.5	—	10	—	200	NZF	
U441	N	71	0.50	6.0	25	6.0	30	4500	—	3.5	—	20	—	200	NZF	
U443	N	78	.5	6	25	6.0	30	4500	9000	3.5	—	10	—	200	NZF	
U444	N	78	.5	6	25	6.0	30	4500	9000	3.5	—	20	—	200	NZF	
2N3921	N	71	1.0	3.0	50	1.0	10	1500	—	18	2.0	5.0	10	35	NNR	GENERAL PURPOSE
2N3922	N	71	1.0	3.0	50	1.0	10	1500	—	18	2.0	5.0	25	35	NNR	
2N3954	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	0.5	5.0	10	35	NQP	
2N3954A	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	0.5	5.0	5.0	35	NQP	
2N3955	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	0.5	10	25	35	NQP	
2N3955A	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	0.5	10	15	35	NQP	
2N3956	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	0.5	15	50	35	NQP	
2N3957	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	0.5	20	75	35	NQP	
2N3958	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	0.5	25	100	35	NQP	
2N4084	N	71	1.0	3.0	50	1.0	10	1500	—	18	2	15	10	35	NNR	
2N4085	N	71	1.0	3.0	50	1.0	10	1500	—	18	2	15	25	35	NNR	
2N5045	N	71	0.25	4.5	50	0.5	8.0	1500	—	8.0	200	5.0	67	25	NNR	
2N5046	N	71	0.25	4.5	50	0.5	8.0	1500	—	8.0	200	10	133	25	NNR	
2N5047	N	71	0.25	4.5	50	0.5	8.0	1500	—	8.0	200	15	200	25	NNR	
2N5452	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	20	5.0	5.0	1.0	NQP	
2N5453	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	20	10	10	1.0	NQP	
2N5454	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	20	15	25	1.0	NQP	
2N5564	N	71	0.1	3.0	40	5.0	30	7500	—	12	50	5.0	10	45	NCA-D	
2N5565	N	71	0.1	3.0	40	5.0	30	7500	—	12	50	10	25	45	NCA-D	
2N5566	N	71	0.1	3.0	40	5.0	30	7500	—	12	50	20	50	45	NCA-D	
DN5564	N	71	.1	3.0	40	5	50	7500	12500	12	50	5	10	65	NCA-D	
DN5565	N	71	.1	3.0	40	5	50	7500	12500	12	50	10	25	65	NCA-D	
DN5566	N	71	.1	3.0	40	5	50	7500	12500	12	50	20	50	65	NCA-D	
U231	N	71	0.1	4.5	50	0.5	5.0	1000	—	6.0	80	5.0	10	35	NQP	
U232	N	71	0.1	4.5	50	0.5	5.0	1000	—	6.0	80	10	25	35	NQP	
U233	N	71	0.1	4.5	50	0.5	5.0	1000	—	6.0	80	15	50	35	NQP	
U234	N	71	0.1	4.5	50	0.5	5.0	1000	—	6.0	80	20	75	35	NQP	
U235	N	71	0.1	4.5	50	0.5	5.0	1000	—	6.0	80	25	100	35	NQP	
U410	N	71	0.2	3.5	40	0.5	6.0	1000	—	—	13	10	10	20	NQP	
U411	N	71	0.2	3.5	40	0.5	6.0	1000	—	—	13	20	25	20	NQP	
U412	N	71	0.2	3.5	40	0.5	6.0	1000	—	—	13	40	80	20	NQP	
DN5567	N	71	0.1	3.0	−40	5	60	—	—	7.0	—	20	—	—	NCA-D	SWITCH

Product Specifications (Cont'd)

Low Leakage Diodes

Part Number	Package (TO-)	Diode	Reverse Current (pA, Max.)	Breakdown Voltage (Volts) Min.	Breakdown Voltage (Volts) Max.	Forward Voltage Drop Volts (Max.)	Capacitance (pF, Max.)
DPAD1	78	Dual	1	45	120	1.5	0.8
DPAD2	72	Dual	2	45	120	1.5	0.8
DPAD5	72	Dual	5	45	120	1.5	0.8
DPAD10	72	Dual	10	35	–	1.5	2.0
DPAD20	72	Dual	20	35	–	1.5	2.0
DPAD50	72	Dual	50	35	–	1.5	2.0
DPAD100	72	Dual	100	35	–	1.5	2.0
JPAD2	92	Single	2	35	–	1.5	2.0
JPAD5	92	Single	5	35	–	1.5	2.0
JPAD10	92	Single	10	35	–	1.5	2.0
JPAD20	92	Single	20	35	–	1.5	2.0
JPAD50	TO-92	Single	20	35	–	1.5	2.0
JPAD100	TO-92	Single	50	35	–	1.5	2.0
JPAD200	TO-92	Single	100	35	–	1.5	2.0
JPAD500	TO-92	Single	500	35	–	1.5	2.0
PAD1	18	Single	1	45	120	1.5	0.8
PAD2	18	Single	2	45	120	1.5	0.8
PAD5	18	Single	5	45	120	1.5	0.8
PAD10	18	Single	10	35	–	1.5	2.0
PAD20	18	Single	20	35	–	1.5	2.0
PAD50	18	Single	50	35	–	1.5	2.0
PAD100	18	Single	100	35	–	1.5	2.0

Voltage Controlled Resistors

Part Number	N or P	Package (TO-)	Breakdown Voltage (Volts, Min.)	Threshold Voltage (Volts) Min.	Threshold Voltage (Volts) Max.	Resistance (Channel Ω) Min.	Resistance (Channel Ω) Max.	Geometry
VCR2N	N	18	15	3.5	7.0	20	60	NCA
VCR3P	P	72	15	3.5	7.0	70	200	PSA
VCR4N	N	18	15	3.5	7.0	200	600	NPA
VCR7N	N	72	15	2.5	5.0	4000	8000	NT
VCR11N	N	71	30	8.0	12.0	100	200	NSH

P-Channel MOSFETs

Part Number	Package (TO-)	Operating Mode	Threshold Voltage (Volts, Max.)	Resistance Channel (Ω, Max.)	Leakage Channel On (mA) Min.	Leakage Channel On (mA) Max.	Leakage Channel Off (nA, Max.)	Breakdown Voltage (Volts, Max.)	Input Capacitance (pF, Max.)	Reverse Capacitance (pF, Max.)	Geometry
3N163	72	ENH	5.0	250	5.0	30	–	40	2.5	0.7	MRA
3N164	72	ENH	5.0	300	3.0	30	–	30	2.5	0.7	MRA
MFE823	18	ENH	6.0	–	3.0	–	20	25	6.0	1.5	MRA

N-Channel MOSFETs

Part Number	Package (TO-)	Operating Mode	Threshold Voltage (Volts, Max.)	Resistance Channel (Ω, Max.)	Leakage Channel On (mA) Min.	Leakage Channel On (mA) Max.	Leakage Channel Off (nA, Max.)	Breakdown Voltage (Volts, Max.)	Input Capacitance (pF, Max.)	Reverse Capacitance (pF, Max.)	Geometry
M116		ENH	5.0	200	—	—	—	60	10.0	—	MBN

Product Specifications (Cont'd)

Current Regulator Diodes

Part Number	Package (TO-)	Forward Current (mA)	Forward Current Tolerance (%)	Limiting Voltage (Volts, Max.)	Peak Operating Voltage (Volts, Max.)	Dynamic Impedance (MΩ, Max.)	Forward Capacitance (pF, typ)	Geometry
CR022	18	0.22	10	1.00	100	13	–	NKL
CR024	18	0.24	10	1.00	100	10	–	NKL
CR027	18	0.27	10	1.00	100	9.0	–	NKL
CR030	18	0.30	10	1.00	100	8.0	–	NKL
CR033	18	0.33	10	1.00	100	6.6	–	NKL
CR039	18	0.39	10	1.05	100	4.1	–	NKL
CR043	18	0.43	10	1.05	100	3.3	–	NKL
CR047	18	0.47	10	1.10	100	2.7	–	NKL
CR056	18	0.56	10	1.20	100	1.9	–	NKL
CR062	18	0.62	10	1.30	100	1.55	–	NKL
CR068	18	0.68	10	1.15	100	1.35	–	NKM
CR075	18	0.75	10	1.20	100	1.15	–	NKM
CR082	18	0.82	10	1.25	100	1.00	–	NKM
CR091	18	0.91	10	1 29	100	0.88	–	NKM
CR100	18	1.00	10	1.35	100	0.80	–	NKM
CR110	18	1.10	10	1.40	100	0.70	–	NKM
CR120	18	1.20	10	1.45	100	0.64	–	NKM
CR130	18	1.30	10	1.50	100	0.58	–	NKM
CR140	18	1.40	10	1.55	100	0.54	–	NKM
CR150	18	1.50	10	1.60	100	0.51	–	NKM
CR160	18	1.60	10	1 65	100	0.475	–	NKO
CR180	18	1.80	10	1.75	100	0.42	–	NKO
CR200	18	2.00	10	1 85	100	0.395	–	NKO
CR220	18	2.20	10	1.95	100	0.37	–	NKO
CR240	18	2.40	10	2.00	100	0.345	–	NKO
CR270	18	2.70	10	2.15	100	0.32	–	NKO
CR300	18	3.00	10	2.25	100	0.30	–	NKO
CR330	18	3.30	10	2.35	100	0.28	–	NKO
CR360	18	3.60	10	2.50	100	0.265	–	NKO
CR390	18	3.90	10	2.60	100	0.255	–	NKO
CR430	18	4.30	10	2.75	100	0.245	–	NKO
CR470	18	4.70	10	2.90	100	0.235	–	NKO
CRR0240	18	.24	25	1.0	100	.9	–	NKL
CRR0360	18	.36	25	1.05	100	4.1	–	NKL
CRR0560	18	.56	25	1.30	100	1.15	–	NKL
CRR0800	18	.80	25	1.35	100	0.8	–	NKL
CRR1250	18	1.95	25	1.60	100	.54	–	NKM
CRR1950	18	1.95	25	1.95	100	.37	–	NKM
CRR2900	18	2.90	25	2.35	100	.28	–	NKO
CRR4300	18	4.30	25	3.00	100	0.5	–	NKO
J500	92	0.24	20	1.20	50	5.0	2	NCL
J501	92	0.33	20	1.30	50	3.0	2	NCL
J502	92	0.43	20	1.50	50	2.0	2	NCL
J503	92	0.56	20	1.70	50	1.4	2	NCL
J504	92	0.75	20	1.90	50	1.0	2	NCL
J505	92	1.00	20	2.10	50	0.6	2	NCL
J506	92	1.40	20	2.50	50	0.4	2	NCL
J507	92	1.80	20	2.80	50	0.25	2	NCL
J508	92	2.40	20	3.10	50	0.25	2	NCL
J509	92	3.00	20	3.50	50	0.20	2	NCL
J510	92	3.60	20	3.90	50	0.20	2	NCL
J511	92	4.70	20	4.20	50	0.15	2	NCL
J552	92	0.05	50	1.5	50	2.0	2	NKL
J553	92	(.18 - 0.75)	–	.75	50	10	–	NCL
J554	92	(06 -1.6)	–	.75	50	1.0	–	NCL
J555	92	(1.4 - 2.6)	–	.75	50	.88	–	NCL
J556	92	(2.4 - 3.8)	–	.75	50	.6	–	NCL
J557	92	(3.6 - 5.3)	–	1.5	50	.48	–	NCL
J9100	92	0.05	50	1.5	50	2.0	2	NCL
JR135V	92	0.200	–	0.9	135	2.0	–	VRMA
JR170V	92	0.200	–	0.9	170	2.0	–	VRMA
JR200V	92	0.200	–	0.9	200	2.0	–	VRMA
JR220V	92	0.200	–	0.9	220	2.0	–	VRMA
JR240V	92	0.200	–	0.9	240	2.0	–	VRMA

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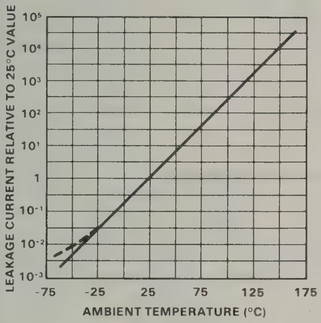
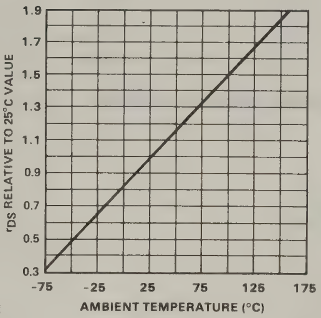
Useful JFET Parameter Relationships (Approximate)

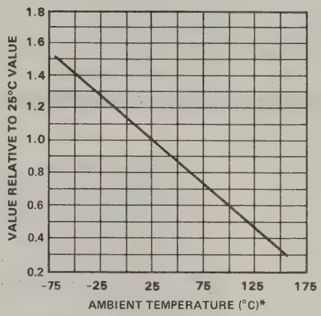
Bulk & Junction Leakage Current vs Ambient Temperature



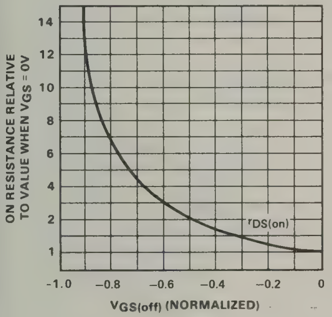
On Resistance vs Ambient Temperature



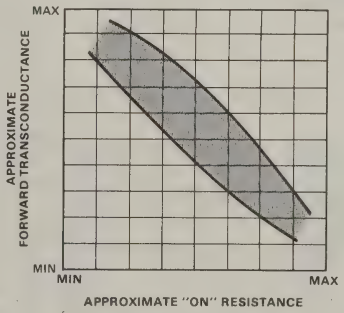
Drain Current and Transconductance vs Ambient Temperature



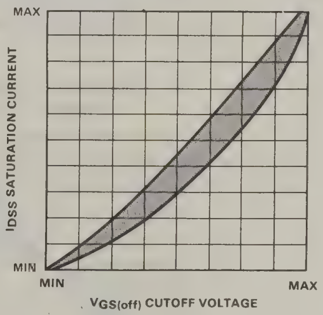
Typical $r_{DS(on)}$ vs Normalized Gate Source Cutoff Voltage



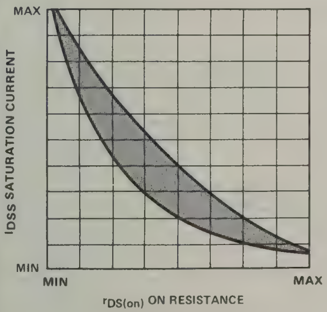
On Resistance vs Transconductance



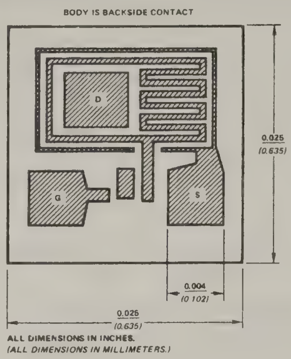
Saturation Current vs Cutoff Voltage



Saturation Current vs ON Resistance



*When $I_D > 5 \times I_{D2}$



enhancement-type n-channel MOSFET *designed for . . .*

Siliconix

- Audio Amplifiers
- Analog Circuits
- Digital Switching Circuits
- Commutating Circuits

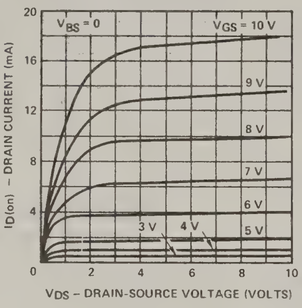
BENEFITS:

- Integrated Zener Clamp Protects the Gate
- Normally OFF

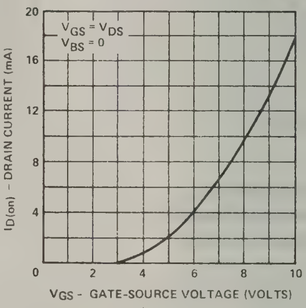
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	M116
Single	Chip	M116CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

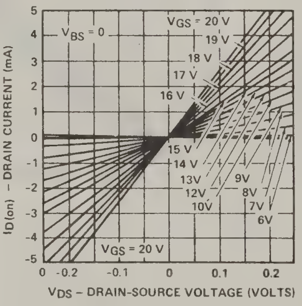
Output Characteristics



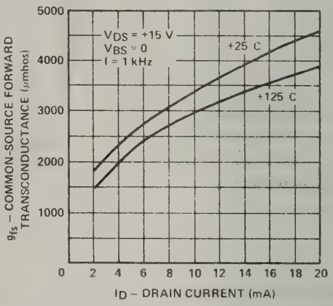
Transfer Characteristic



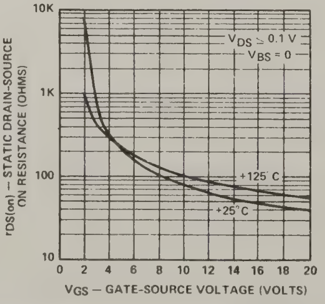
Low Voltage Output Characteristics



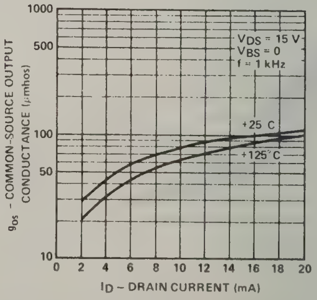
Forward Transconductance vs Drain Current



Drain-Source ON State Resistance vs Gate-Source Bias

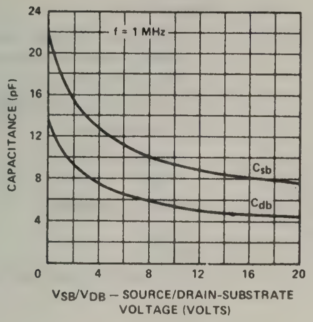


Output Conductance vs Drain Current

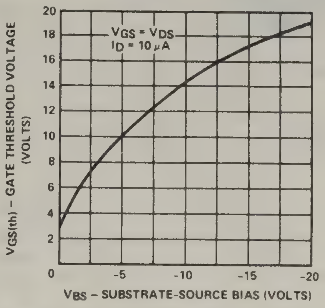


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

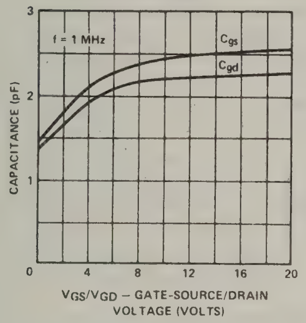
Substrate Capacitance vs Voltage



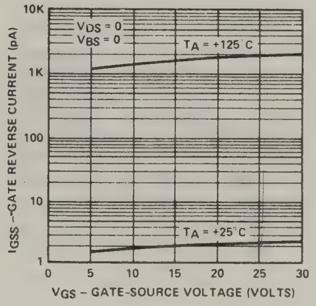
Gate Threshold Voltage vs Substrate Bias



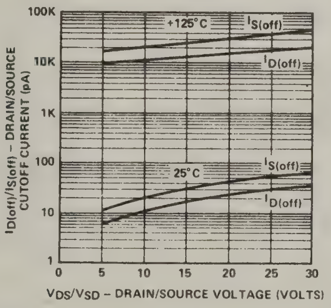
Gate Capacitance vs Voltage

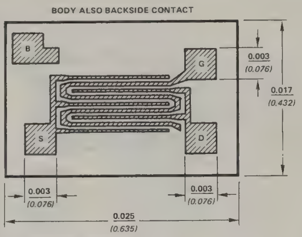


Gate Leakage Current vs Gate-Source Bias



Source-Drain Leakage Currents vs Voltage





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

enhancement-type p-channel MOSFET *designed for . . .*

Siliconix

- Analog and Digital Switching
- General Purpose Amplifiers
- Smoke Detectors

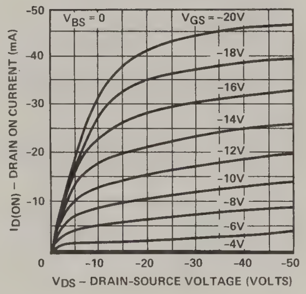
BENEFITS:

- **High Gate Transient Voltage Breakdown Eliminates Need for Gate Protective Diode**
- **Ultra-High Input Impedance**
- **Low Leakage**
- **Normally OFF**

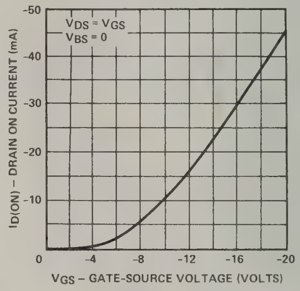
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18	MFE823
Single	TO-72	3N163-64
Single	Chip	3N163-64CHP, MFE823CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

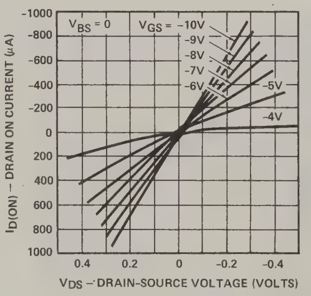
Output Characteristics



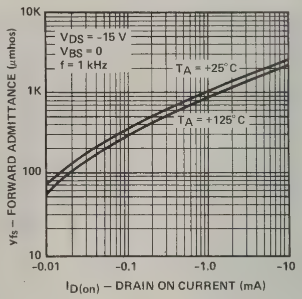
Transfer Characteristic



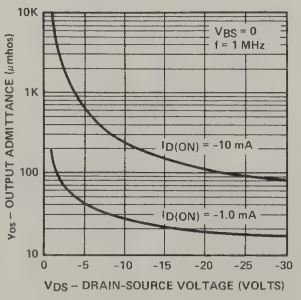
Low-Level Output Characteristics



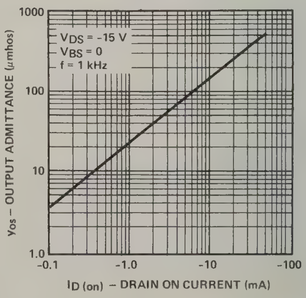
Common-Source, Short-Circuit, Forward Transadmittance vs Drain Current



Common-Source, Short-Circuit, Output Admittance vs Drain Voltage

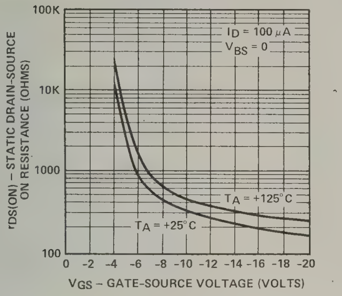


Common-Source, Short-Circuit, Output Admittance vs Drain Current

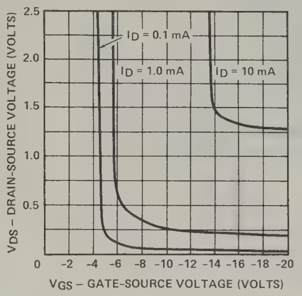


PERFORMANCE CURVES (Cont'd) (25° C unless otherwise noted)

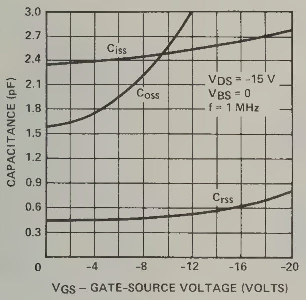
Drain-Source ON Resistance vs Gate-Source Voltage



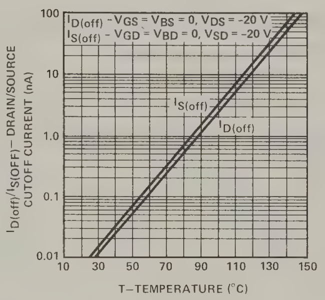
Low-Level ON Drain-Source Voltage vs Gate-Source Voltage

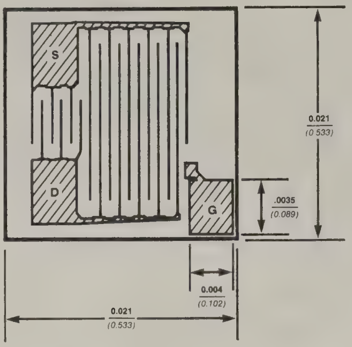


Capacitance vs Gate-Source Voltage



Drain-Source Leakage Current vs Temperature





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFETs
designed for . . .

Siliconix

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

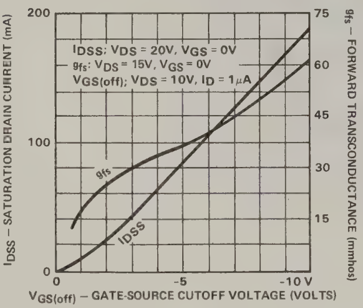
BENEFITS:

- **No Offset or Error Voltages Generated by Closed Switch. Purely Resistive. High Isolation Resistance From Driver**
- **High Off-Isolation $I_{D(off)} < 100$ pA**
- **High Speed $t_{ON} < 20$ ns**

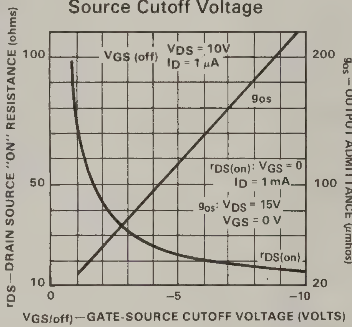
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18	2N3970-72, 2N4091-93, 2N4391-93 2N4856-61, 2N4856A-61A, FN4392,93 U200-01, VCR2N
Single	TO-92	2N5638-40, 2N5653-54, J111-13 PN4091,93 PN4391-93 U1897-99
Dual	TO-71	2N5564-66, DN5564-66, DN5567
Single	Chip	All of above single devices available in chip form
Dual	Chip	2N5566 Chip Set, DN5566 Chip Set

PERFORMANCE CURVES (25°C unless otherwise noted)

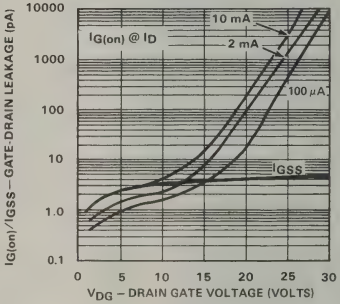
Drain Current & Transconductance vs Gate Source Voltage



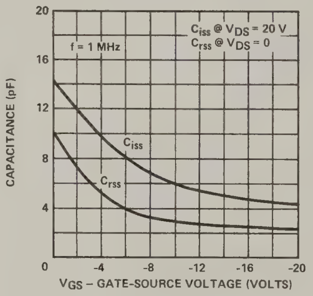
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



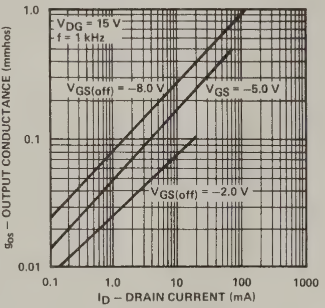
Gate Operating Current vs Drain Gate Voltage



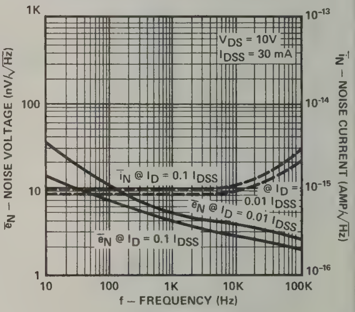
Common-Source Capacitances vs Gate-Source Voltage



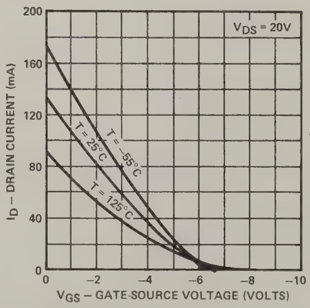
Common-Source Output Conductance vs Drain Current



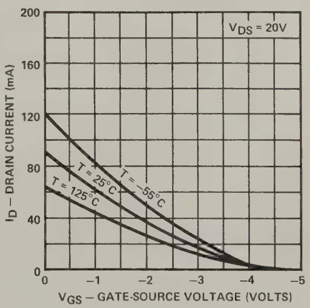
Equivalent Input Noise Voltage and Noise Current vs Frequency



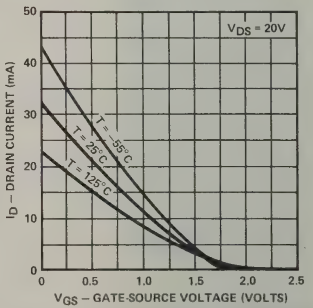
Transfer Characteristics



Transfer Characteristics

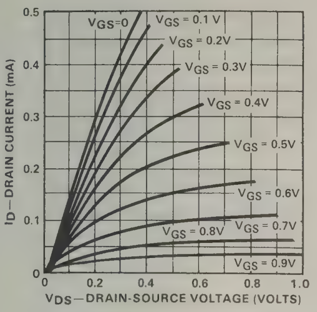


Transfer Characteristics

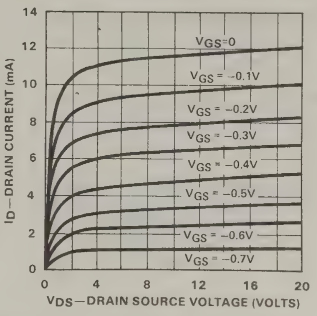


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

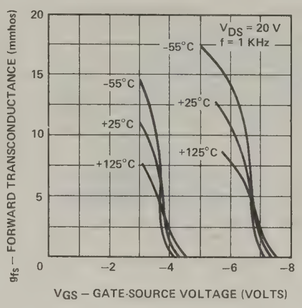
Output Characteristic ($V_{GS(off)} = -1.5V$)



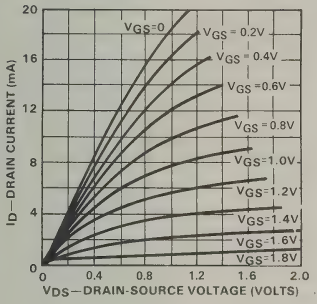
Output Characteristic ($V_{GS(off)} = -1.5V$)



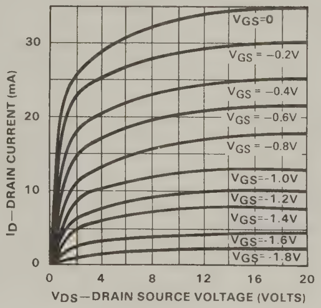
Transconductance Characteristics



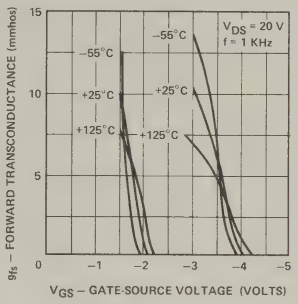
Output Characteristic ($V_{GS(off)} = -3.0V$)



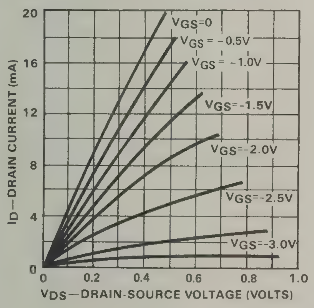
Output Characteristic ($V_{GS(off)} = -3.0V$)



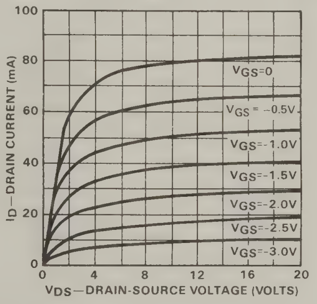
Transconductance Characteristics



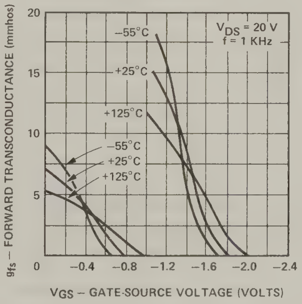
Output Characteristic ($V_{GS(off)} = -5.0V$)



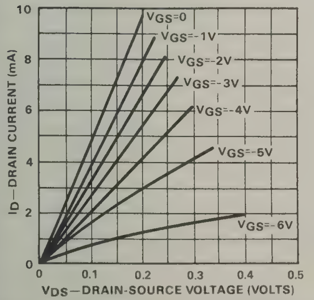
Output Characteristic ($V_{GS(off)} = -5.0V$)



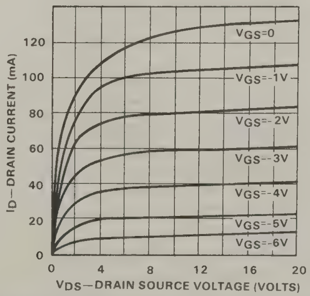
Transconductance Characteristics



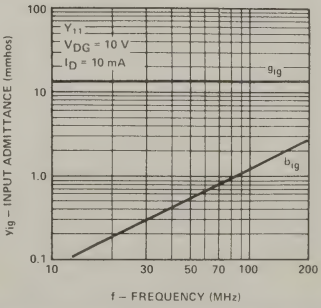
Output Characteristic ($V_{GS(off)} = -8.0V$)



Output Characteristic ($V_{GS(off)} = -8.0V$)

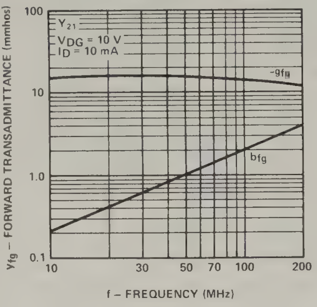


Common-Gate Input Admittance vs Frequency

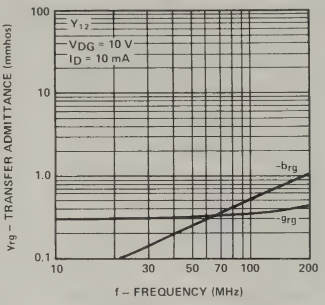


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

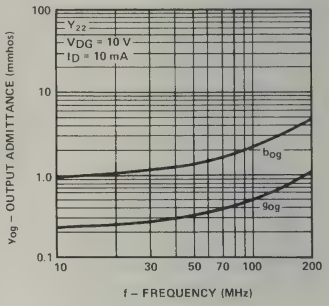
Common-Gate Forward Transadmittance vs Frequency



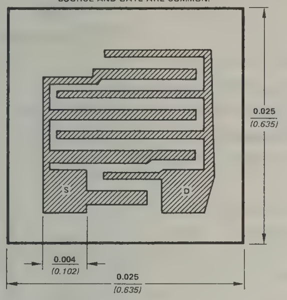
Common-Gate Reverse Transfer Admittance vs Frequency



Common-Gate Output Admittance vs Frequency



GATE IS BACKSIDE CONTACT.
SOURCE AND GATE ARE COMMON.



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET current regulator diode designed for . . .

Siliconix

- Current Regulation
- Current Limiting
- Biasing

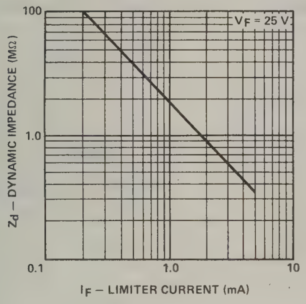
BENEFITS:

- Simple Two Lead Current Source
- Simplifies Floating Current Sources No Power Supplies Required
- Low Cost

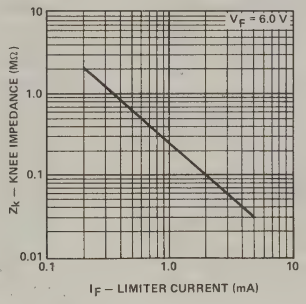
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-92	J500-505, J506-511, J553-7
Single	Chip	J500CHP-505CHP, J506CHP-511 CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

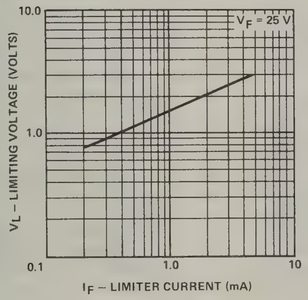
Dynamic Impedance vs Limiter Current



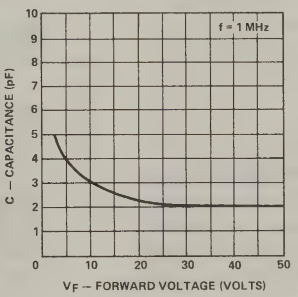
Knee Impedance vs Limiter Current



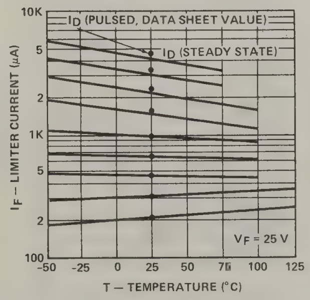
Limiting Voltage at 0.9 I_D vs Limiter Current

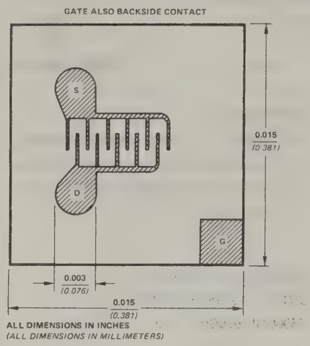


Capacitance vs Forward Voltage



Typical Variation of I_D with Temperature Steady State and Pulsed Value





n-channel JFET *designed for . . .*

Siliconix

- VHF/UHF Amplifiers
- Oscillators
- Mixers
- Low Input Capacitance High Speed Switch

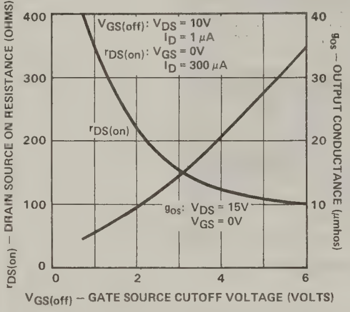
BENEFITS:

- Low Noise
  NF = 3 dB Typical @ 400 MHz
- Wideband
  High g_{fs}/C_{iss} Ratio

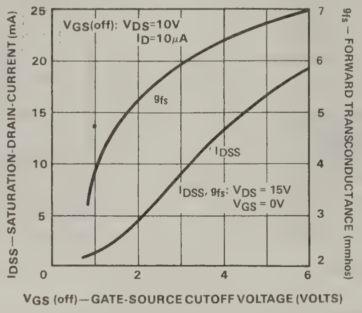
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	2N3966, 2N4416-16A 2N3819
Single	TO-92	2N5484-6, 2N5555, 2N5668-70, MPF102, MPF108, MPF112, PN4416, J304-5,
Single	Chip	All of the above devices

PERFORMANCE CURVES (25°C unless otherwise noted)

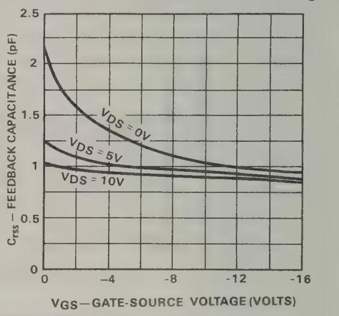
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



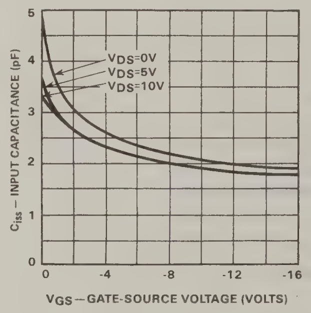
Drain Current & Transconductance vs Gate Source Cutoff Voltage



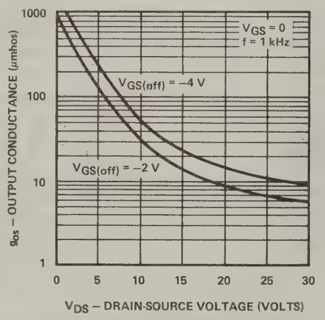
Common Source Reverse Feedback Capacitance vs Gate Source Voltage



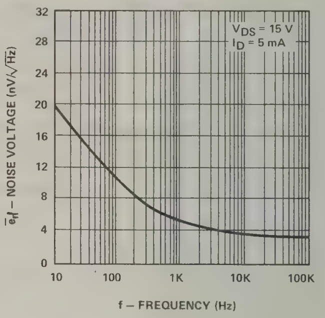
Common Source Input Capacitance vs Gate-Source Voltage



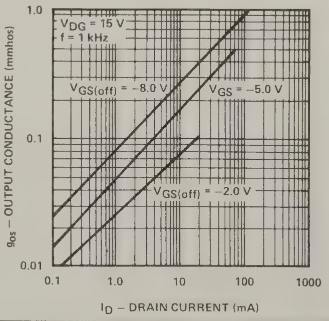
Common-Source Output Conductance vs Drain-Source Voltage



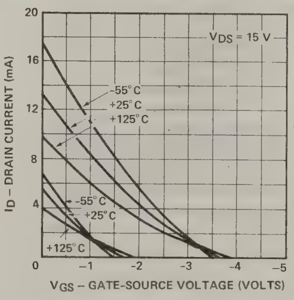
Equivalent Input Noise Voltage vs Frequency



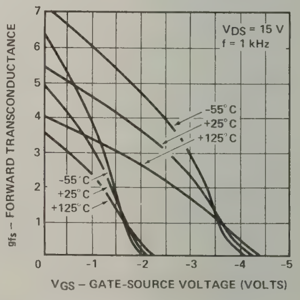
Common-Source Output Conductance vs Drain Current



Transfer Characteristics

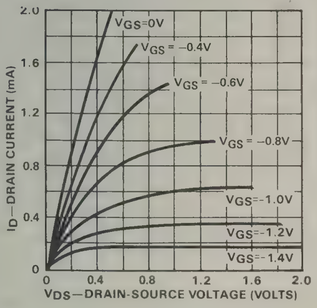


Transconductance Characteristics

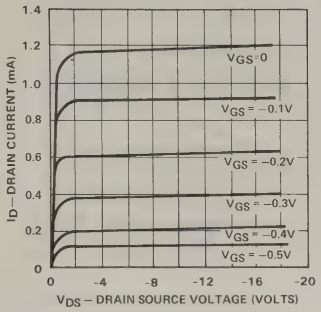


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

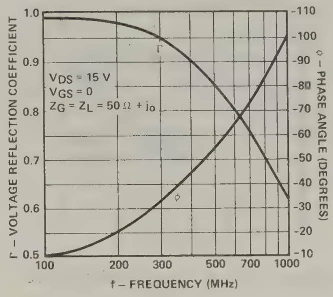
Output Characteristic ($V_{GS(off)} = -2V$)



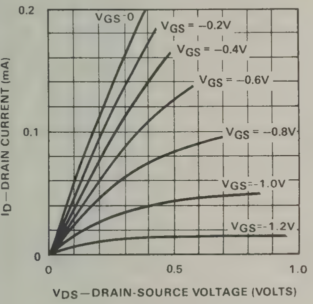
Output Characteristic ($V_{GS(off)} = -1.0V$)



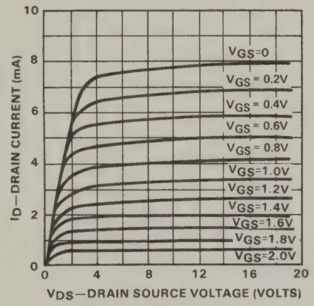
S Parameters S_{11} Common-Source vs Frequency



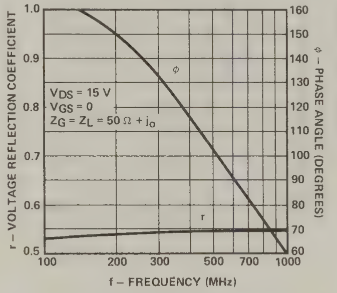
Output Characteristic ($V_{GS(off)} = -1.5V$)



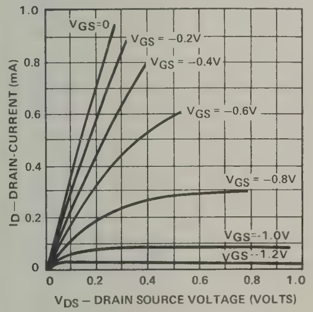
Output Characteristic ($V_{GS(off)} = -3.0V$)



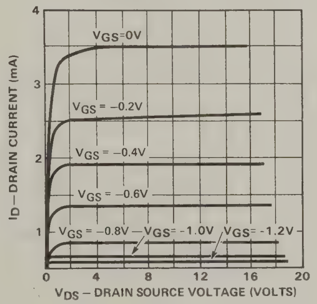
S Parameters S_{21} Common-Source vs Frequency



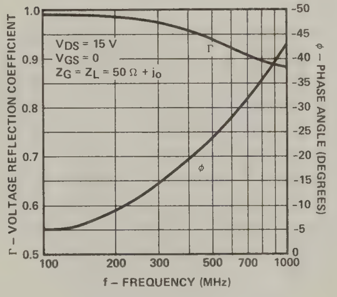
Output Characteristic ($V_{GS(off)} = -1.5V$)



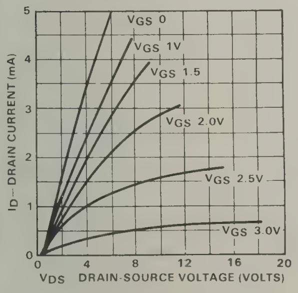
Output Characteristic ($V_{GS(off)} = -1.5V$)



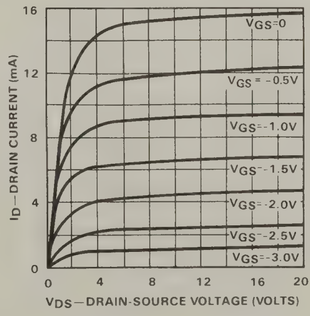
S Parameters S_{22} Common-Source vs Frequency



Output Characteristic ($V_{GS(off)} = -4.0V$)

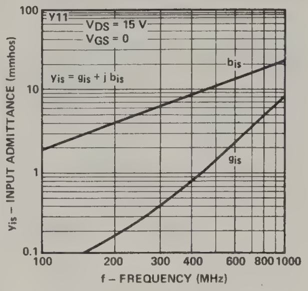


Output Characteristic ($V_{GS(off)} = -4.0V$)

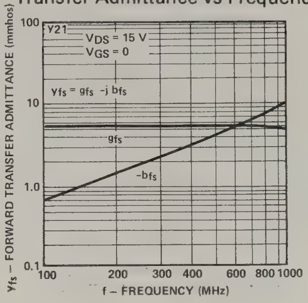


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

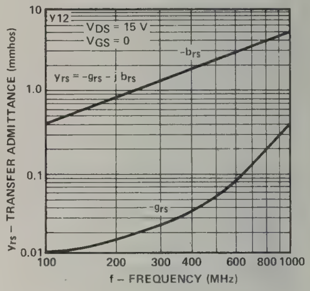
Common-Source Input Admittance vs Frequency



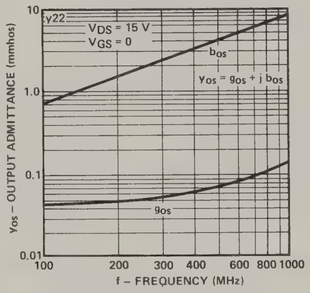
Common-Source Forward Transfer Admittance vs Frequency

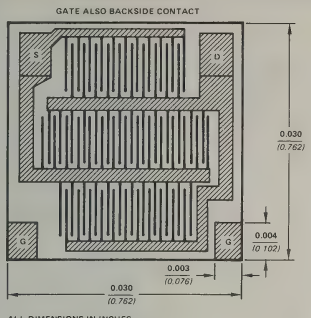


Common-Source Reverse Transfer Admittance vs Frequency



Common-Source Output Admittance vs Frequency





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET
designed for . . .

- Low ON Resistance Analog Switches
- Commutators
- Choppers
- Integrator Reset Capacitors
- Low Noise Audio Amplifiers

Siliconix

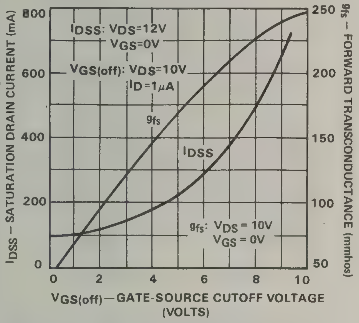
BENEFITS:

- Low Insertion Loss
- Small Error in Measurement Systems $V_{DS(on)} < 50$ mV (2N5432)
- High Off-Isolation $I_{D(off)} < 200$ pA
- High Speed $t_{d(on)} < 4$ ns
- Low Noise Audio-Freq Amplification $\bar{e}_N < 2\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 1 kHz

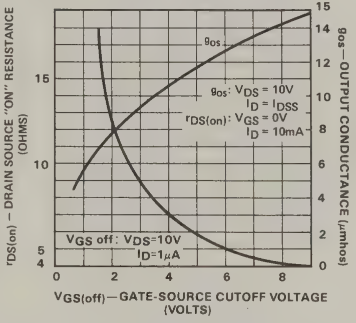
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-52	2N5432-34
Single	TO-92	J108-10
Single	Chip	All of the above devices

PERFORMANCE CURVES (25°C unless otherwise noted)

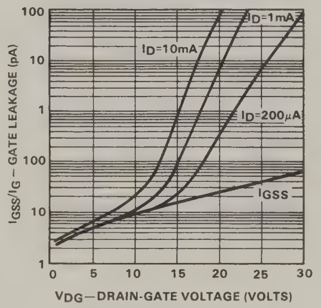
Drain Current & Forward Transconductance vs Gate Source Cutoff Voltage



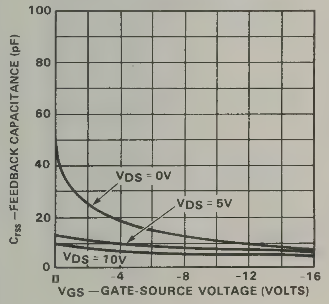
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



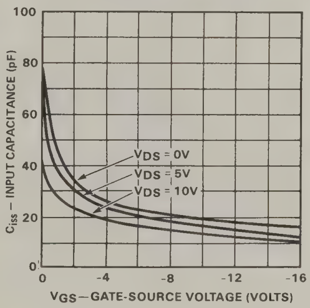
Gate Operating Current vs Drain-Gate Voltage



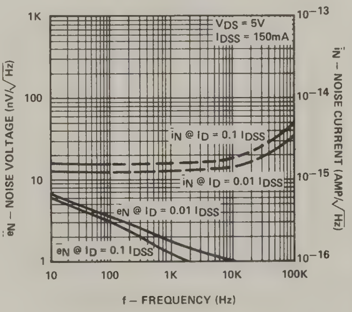
Common Source Reverse Feedback Capacitance vs Gate Source Voltage



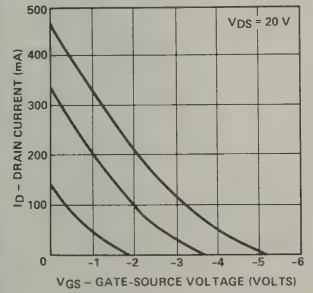
Common Source Input Capacitance vs Gate-Source Voltage



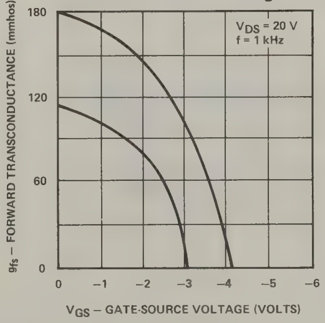
Equivalent Input Noise Voltage and Noise Current vs Frequency



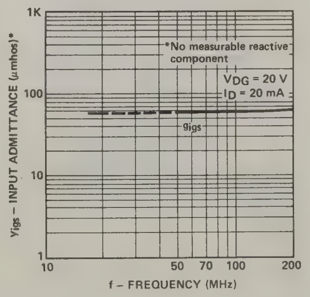
Transfer Characteristics



Forward Transconductance vs Gate Source Voltage

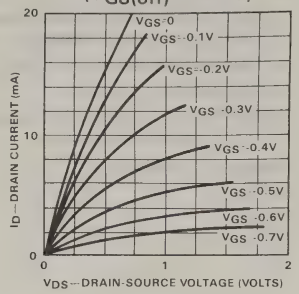


Input Admittance Common Gate vs Frequency

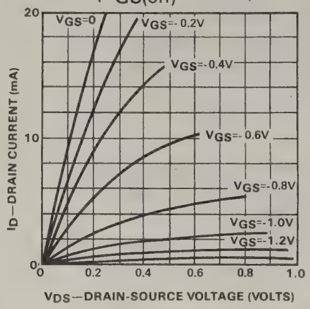


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

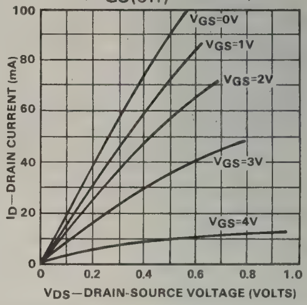
Output Characteristic ($V_{GS(off)} = -1.5V$)



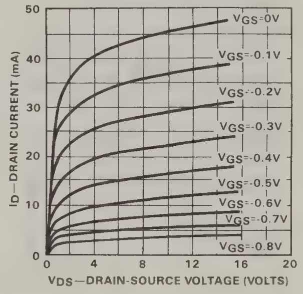
Output Characteristic ($V_{GS(off)} = -2.0V$)



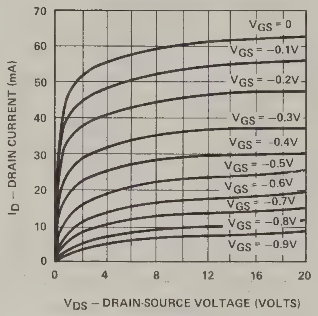
Output Characteristic ($V_{GS(off)} = -6.5V$)



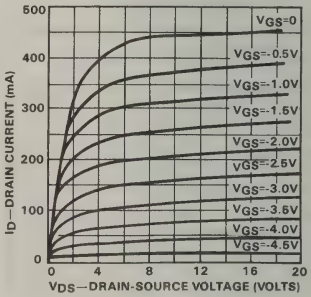
Output Characteristic ($V_{GS(off)} = -1.5V$)



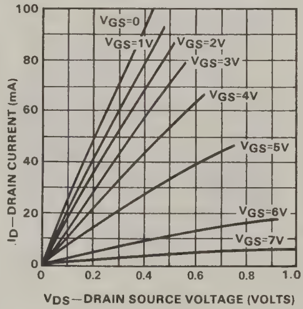
Output Characteristic ($V_{GS(off)} = -2V$)



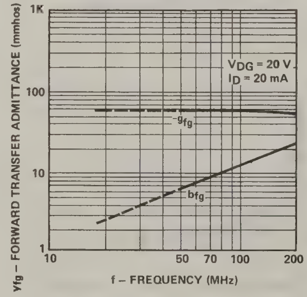
Output Characteristic ($V_{GS(off)} = -6.5V$)



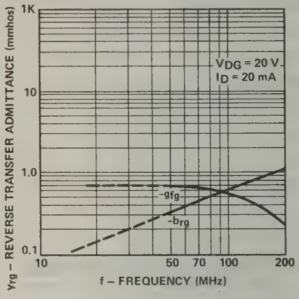
Output Characteristic ($V_{GS(off)} = -9.0V$)



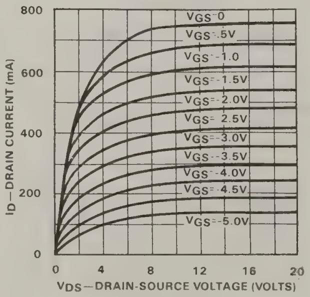
Forward Transfer Admittance Common Gate vs Frequency



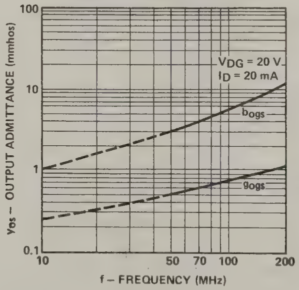
Reverse Transfer Admittance Common Gate vs Frequency



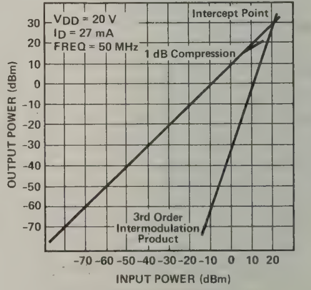
Output Characteristic ($V_{GS(off)} = -9.0V$)

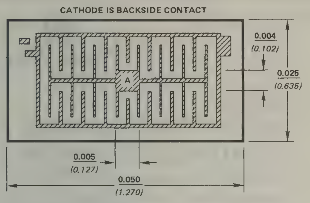


Output Admittance Common Gate vs Frequency



Gain – Intermodulation Characteristics





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET current regulator diode
designed for . . .

Siliconix

- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References

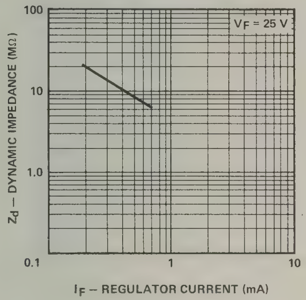
BENEFITS:

- **Simple Two Lead Current Source**
- **Current Insensitive to Temperature Changes. Temperature Coefficient Better Than 0.15%/°C On All Devices**
- **TO-18 Package for Improved Current Control**
- **Simplifies Floating Current Sources No Power Supplies Required**

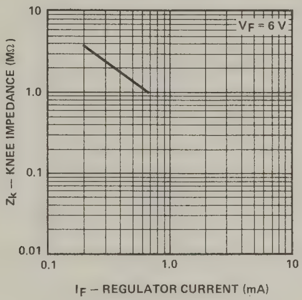
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18 (2-lead)	CR022 Thru CR062 CRR0240 Thru CRR0560
Single	Chip	All of above

PERFORMANCE CURVES (25°C unless otherwise noted)

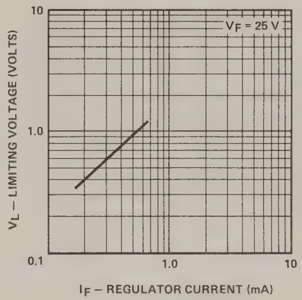
Dynamic Impedance vs Regulator Current



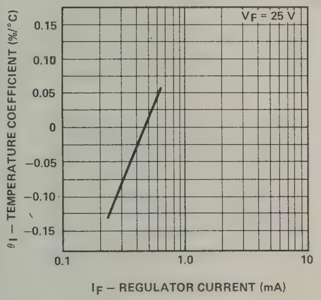
Knee Impedance vs Regulator Current



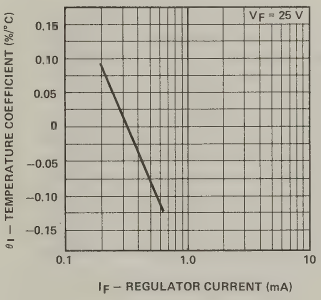
Limiting Voltage @ 0.8 I_F vs Regulator Current



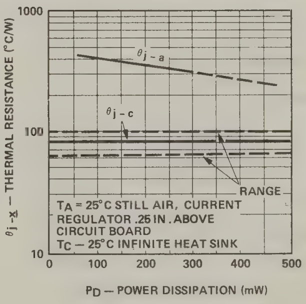
Temperature Coefficient −55°C ⩽ T_j ⩽ 25°C vs Regulator Current



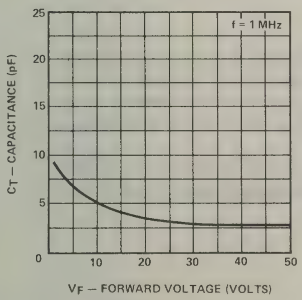
Temperature Coefficient 25°C ⩽ T_j ⩽ 125°C vs Regulator Current



Thermal Resistance vs Power Dissipation

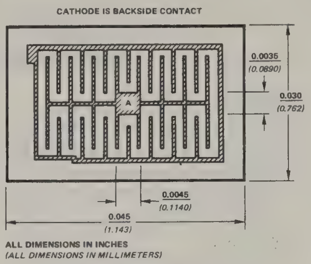


Capacitance vs Forward Voltage



NOTE: I_F, Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature. I_F (steady state) = $I_F \times [1 + \theta_I (T_j - 25°C)]$ where θ_I is the temperature coefficient of I_F and T_j is the junction temperature.

T_j may be found by $T_j = T_{amb} + \theta_{j\text{-}a} PD = T_{case} + \theta_{j\text{-}c} PD$. T_j must not exceed 150°C. $\frac{1}{\theta_{j\text{-}c}}$ or $\frac{1}{\theta_{j\text{-}a}}$ is the derating factor for all devices.



n-channel JFET current regulator diode

designed for . . .

- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References

Siliconix

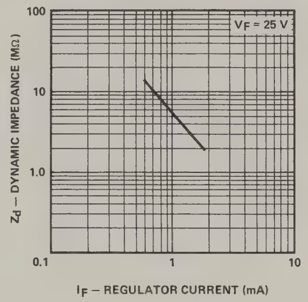
BENEFITS:

- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes. Temperature Coefficient Better Than 0.15%/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources No Power Supplies Required

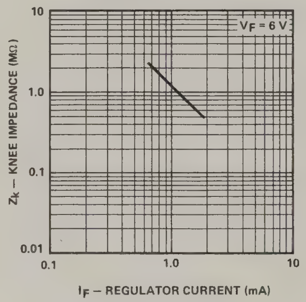
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18 (2-lead)	CR068 Thru CR150 CRR0800 Thru CRR1250
Single	Chip	All of above

PERFORMANCE CURVES (25°C unless otherwise noted)

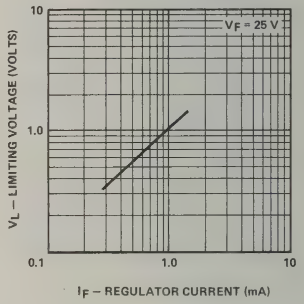
Dynamic Impedance vs Regulator Current



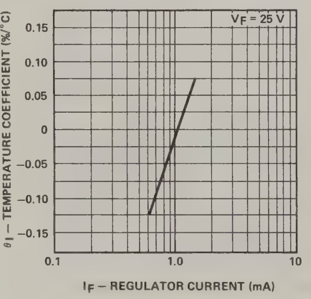
Knee Impedance vs Regulator Current



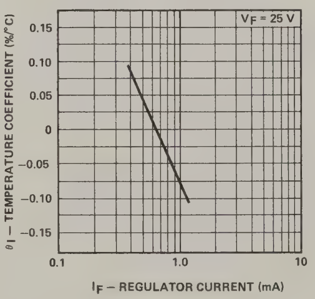
Limiting Voltage @ 0.8 I_F vs Regulator Current



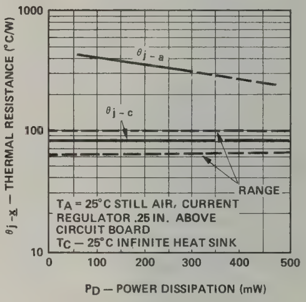
Temperature Coefficient −55°C ≤ T_j ≤ 25°C vs Regulator Current



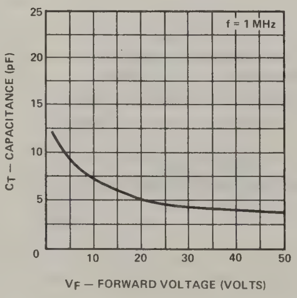
Temperature Coefficient 25°C ≤ T_j ≤ 125°C vs Regulator Current



Thermal Resistance vs Power Dissipation

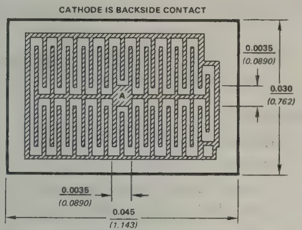


Capacitance vs Forward Voltage



NOTE: I_F, Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature. I_F (steady state) = $I_F \times [1 + \theta_I (T_j - 25°C)]$ where θ_I is the temperature coefficient of I_F and T_j is the junction temperature.

T_j may be found by $T_j = T_{amb} + \theta_{j\text{-}a} P_D = T_{case} + \theta_{j\text{-}c} P_D$. T_j must not exceed 150°C. $\frac{1}{\theta_{j\text{-}c}}$ or $\frac{1}{\theta_{j\text{-}a}}$ is the derating factor for all devices.



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET current regulator diode

designed for . . .

Siliconix

- Current Regulation
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- Low Voltage References

BENEFITS:

- Simple Two Lead Current Source
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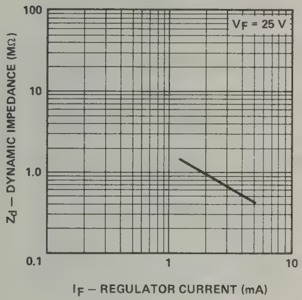
- Simplifies Floating Current Sources No Power Supplies Required

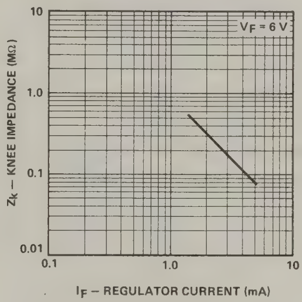
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18 (2-lead)	CR160 Thru CR470 CRR1950 Thru CRR4300
Single	Chip	All of above

PERFORMANCE CURVES (25°C unless otherwise noted)

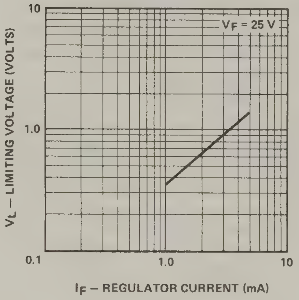
Dynamic Impedance vs Regulator Current



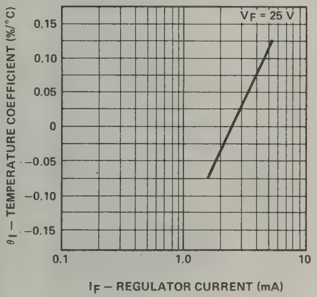
Knee Impedance vs Regulator Current



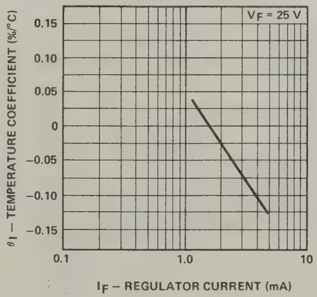
Limiting Voltage @ 0.8 IF vs Regulator Current



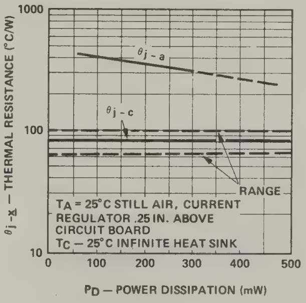
Temperature Coefficient $-55°C \leqslant T_j \leqslant 25°C$ vs Regulator Current



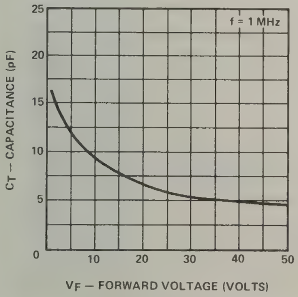
Temperature Coefficient $25°C \leqslant T_j \leqslant 125°C$ vs Regulator Current



Thermal Resistance vs Power Dissipation

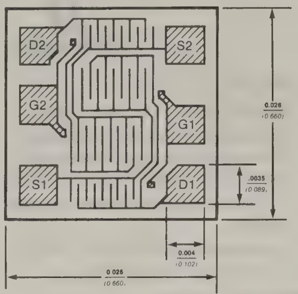


Capacitance vs Forward Voltage



NOTE: I_F, Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature. I_F (steady state) $= I_F \times [1 + \theta_I (T_j - 25°C)]$ where θ_I is the temperature coefficient of I_F and T_j is the junction temperature.

T_j may be found by $T_j = T_{amb} + \theta_{j\text{-}a} P_D = T_{case} + \theta_{j\text{-}c} P_D$. T_j must not exceed 150°C. $\frac{1}{\theta_{j\text{-}c}}$ or $\frac{1}{\theta_{j\text{-}a}}$ is the derating factor for all devices.



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

monolithic dual n-channel JFET designed for . . .

- FET Input Amplifiers
- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Compartors

Siliconix

BENEFITS

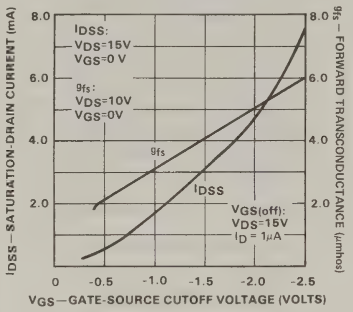
- Minimum System Error and Calibration
  5 mV Offset Maximum (J401)
  95 dB Minimum CMRR
- Low Drift With Temperature
  10 μV/°C (J401)
- Simplifies Amplifier Design
  Output Conductance < 2 μmho
- Low Noise
  $\overline{e_n}$ = 6 nV/$\sqrt{Hz}$ at 10 Hz Typical

TYPE	PACKAGE
Dual	TO-71
Dual	Chip

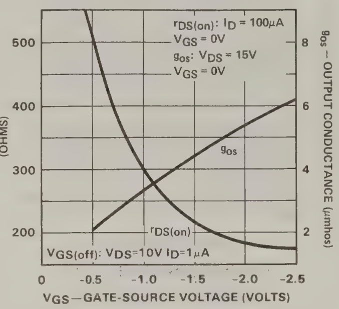
PRINCIPAL DEVICES

2N3921-2, 2N4084-5, 2N5045-7, U401-6, 2N5046CHP-47CHP, U403CHP-06CHP, 2N4085CHP

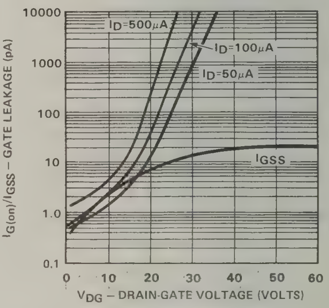
Drain Current & Transconductance vs Gate Source Voltage



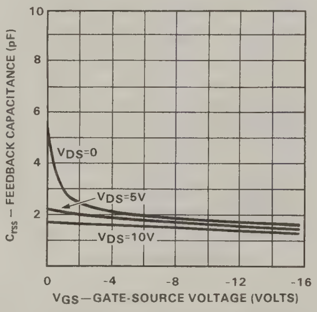
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



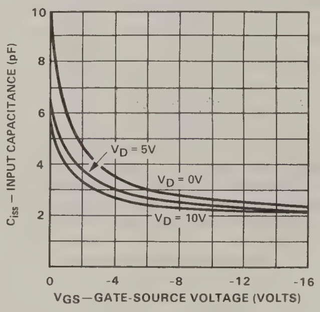
Gate Operating Current vs Drain Gate Voltage



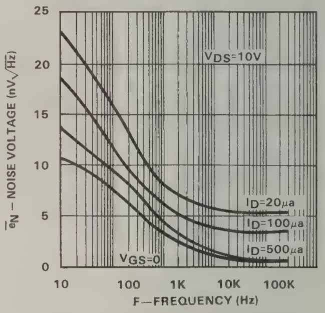
Common Source Reverse Feedback Capacitance vs Gate Source Voltage



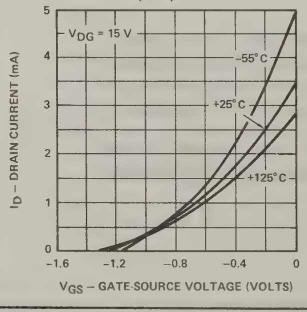
Common-Source Input Capacitance vs Gate-Source Voltage



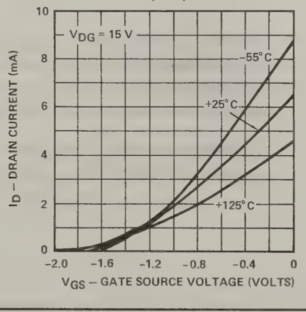
Noise Voltage vs Frequency



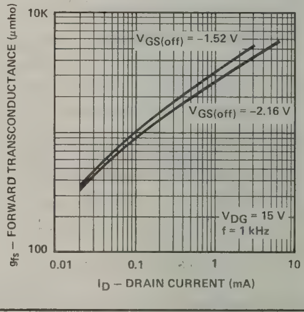
Transfer Characteristics Low $V_{GS(off)}$ Unit (–1.5 V)



Transfer Characteristics Medium $V_{GS(off)}$ Unit (–2.2 V)

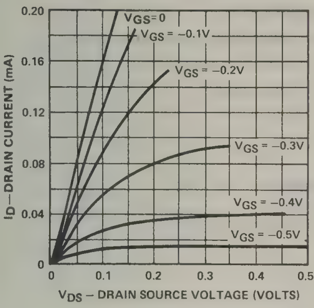


Forward Transconductance vs Drain Current

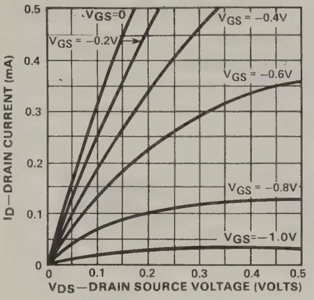


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

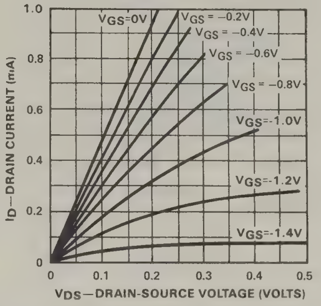
Output Characteristic ($V_{GS(off)} = -0.6V$)



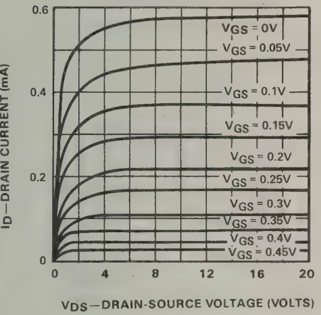
Output Characteristic ($V_{GS(off)} = -1.2V$)



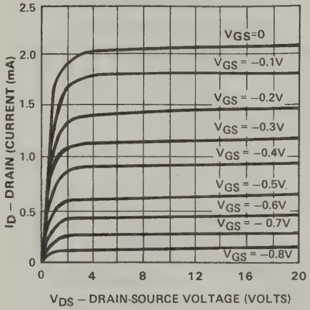
Output Characteristic ($V_{GS(off)} = -1.7V$)



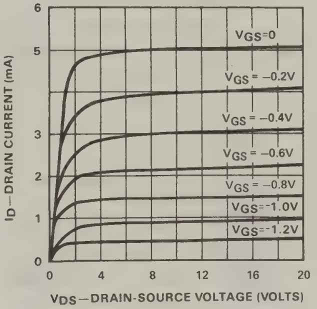
Output Characteristic ($V_{GS(off)} = -0.6V$)



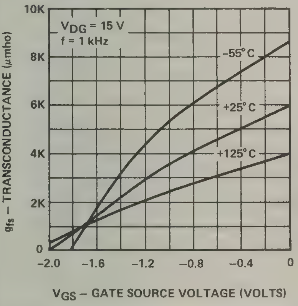
Output Characteristic ($V_{GS(off)} = -1.2V$)



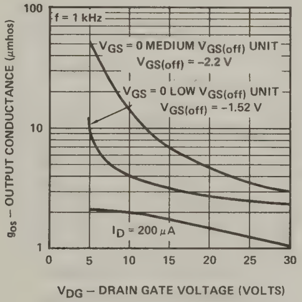
Output Characteristic ($V_{GS(off)} = -1.7V$)

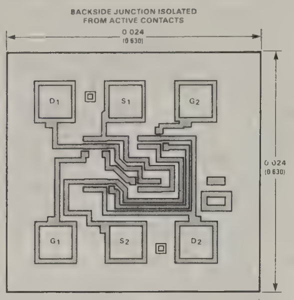


Transconductance vs Gate Source Voltage Medium $V_{GS(off)}$ Unit (−2.0V)



Output Conductance vs Drain Gate Voltage





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMITERS)

monolithic dual n-channel JFETs

designed for . . .

Siliconix

- **Low Leakage FET Input Op Amps**
- **pH Meters**
- **Electrometers**

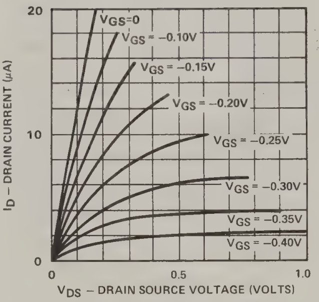
BENEFITS:

- **Ultra-High Input Impedance**
- **Good Voltage Gain**
- **Low Noise**

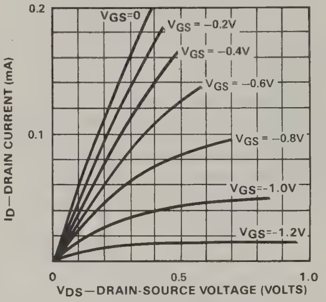
TYPE	PACKAGE	PRINCIPAL DEVICES
Dual	TO-78	U421-28
Dual	Chip	U423CHP-428CHP

PERFORMANCE CURVES (25° C unless otherwise noted)

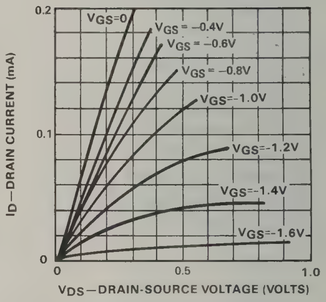
Output Characteristic
($V_{GS(off)} = -0.5V$)



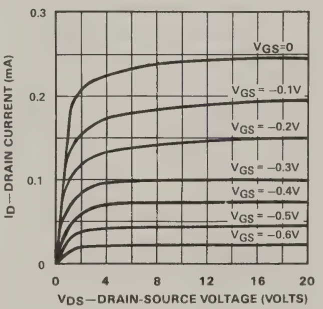
Output Characteristic
($V_{GS(off)} = -1.5V$)



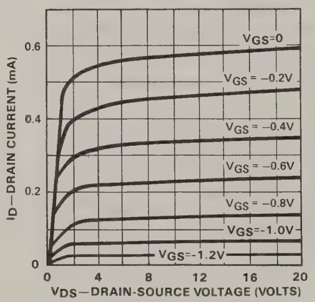
Output Characteristic
($V_{GS(off)} = -2.0V$)



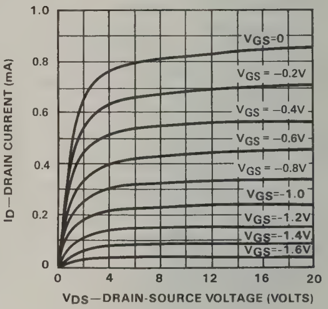
Output Characteristic
($V_{GS(off)} = -0.5V$)



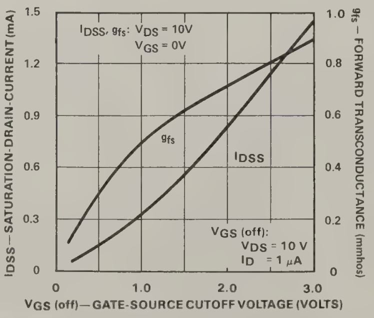
Output Characteristic
($V_{GS(off)} = -1.5V$)



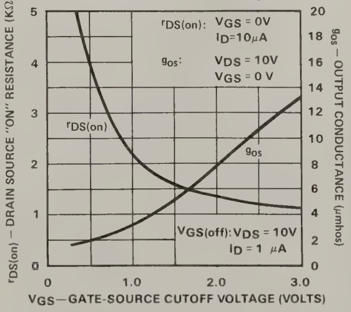
Output Characteristic
($V_{GS(off)} = -2.0V$)



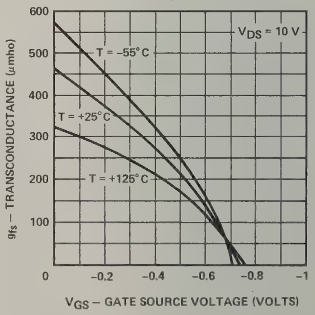
Drain Current & Transconductance vs Gate Source Cutoff Voltage



On Resistance & Output Conductance vs Gate-Source Cutoff Voltage

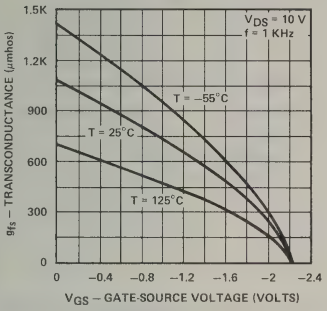


Transconductance vs Gate Source Voltage Low $V_{GS(off)}$ Unit (1.0 V)

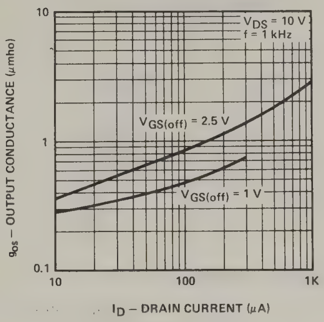


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

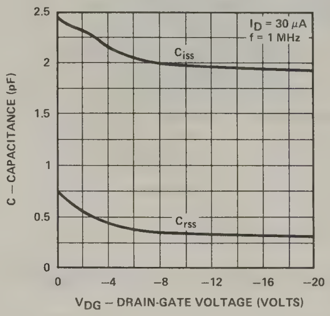
Transconductance vs Gate Source Voltage High $V_{GS(off)}$ Unit (2.5 V)



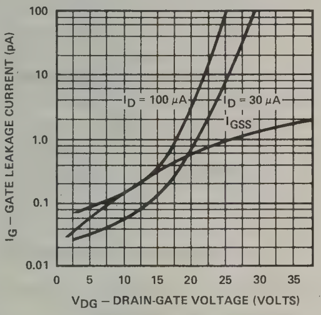
Common-Source Output Conductance vs Drain Current



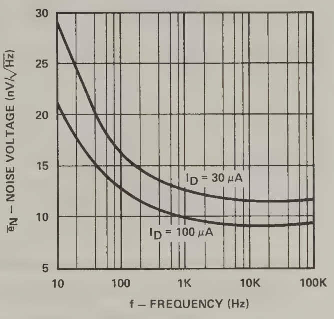
Capacitance vs Drain Gate Voltage

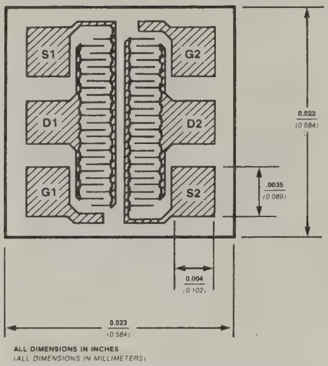


Gate Operating Current vs Drain-Gate Voltage



Equivalent Input Noise Voltage vs Frequency





n-channel JFET
designed for . . .

Siliconix

- High Frequency Amplifiers
- Mixers
- Oscillators

BENEFITS:

- High Power Gain
- Low Input Capacitance

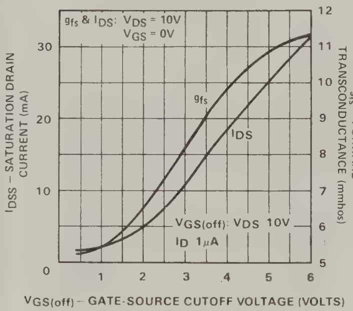
TYPE	PACKAGE
Dual	TO-78
Dual	TO-71
Dual	Chip

PRINCIPAL DEVICES

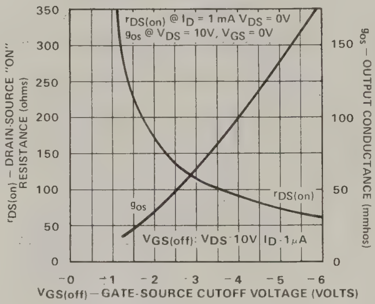
2N5911-12, U257 U443-U444
U440-41
M5911CHP, M5912CHP,
M440CHP, M441CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

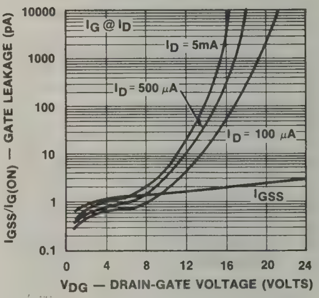
Drain Current and Transconductance vs Gate-Source Cutoff Voltage



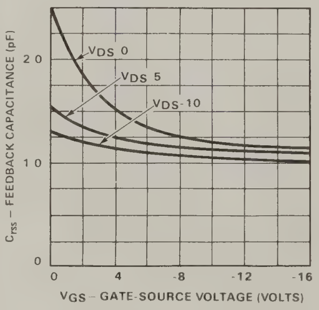
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



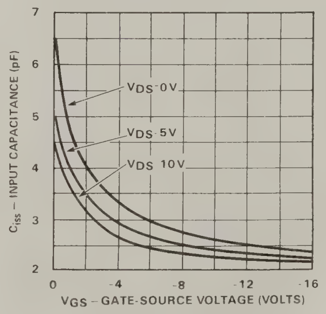
Gate Operating Current vs Drain-Gate Voltage



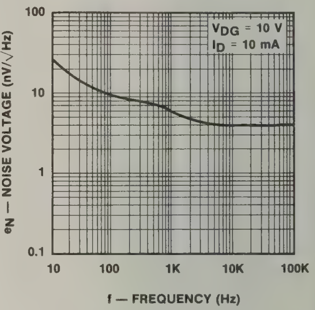
Common Source Feedback Capacitance vs Gate-Source Voltage



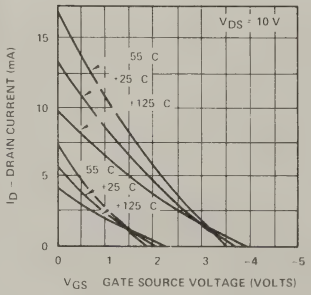
Common Source Input Capacitance vs Gate-Source Voltage



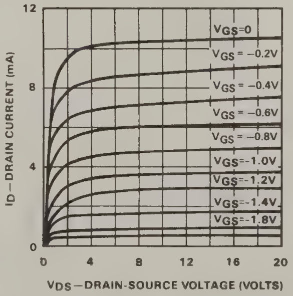
Equivalent Input Noise Voltage vs Frequency



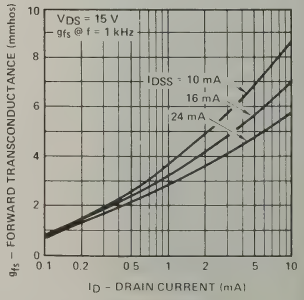
Transfer Characteristics

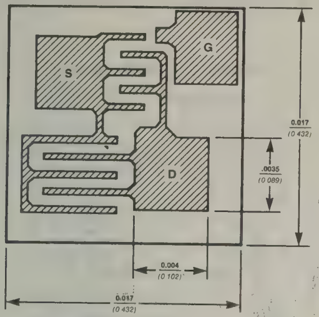


Output Characteristic ($V_{GS(off)}$ = −2.8V)



Forward Transconductance vs Drain Current





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET
designed for . . .

Siliconix

- Small Signal Amplifiers
- Choppers
- Voltage-Controlled Resistors

BENEFITS:

- Low Noise NF < 1 dB at 1 kHz
- Operation From Low Power Supply Voltages, $V_{GS(off)} < 1$ V (2N4338)
- High Off-Isolation As a Switch $I_{D(off)} < 50$ pA
- High Input Impedance

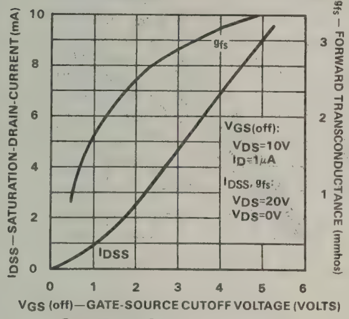
TYPE	PACKAGE
Single	TO-18
Single	TO-72
Single	TO-92
Dual	Chip
Single	Chip

PRINCIPAL DEVICES
2N4338-41, VCR4N
2N4867-9, 2N4869A-9A
J201-204, PN4302-04, J230-2

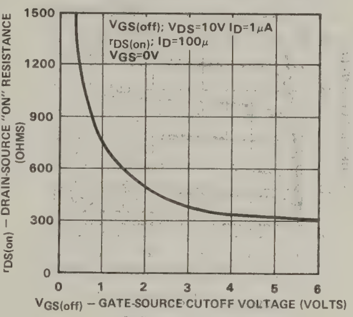
All single Part No's above

PERFORMANCE CURVES (25°C unless otherwise noted)

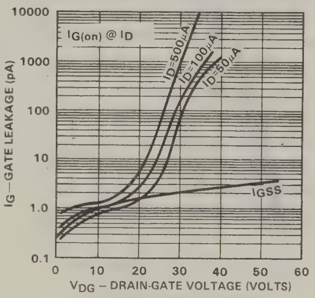
Drain Current & Transconductance vs Gate-Source Cutoff Voltage



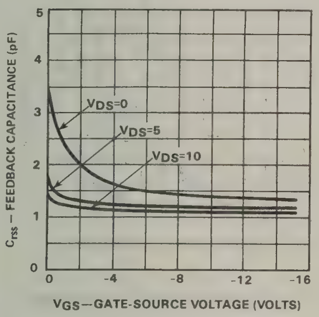
ON Resistance vs Gate-Source Cutoff Voltage



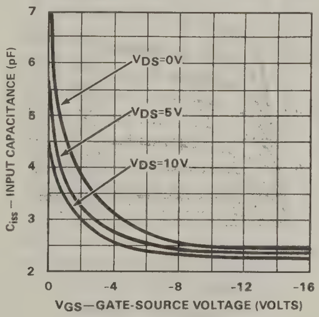
Gate Operating Current vs Drain-Gate Voltage



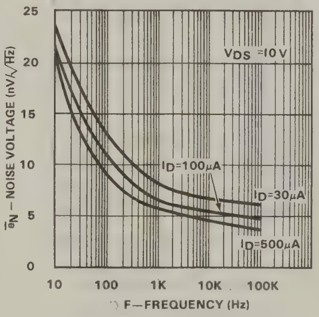
Common Source Reverse Feedback Capacitance vs Gate Source Voltage



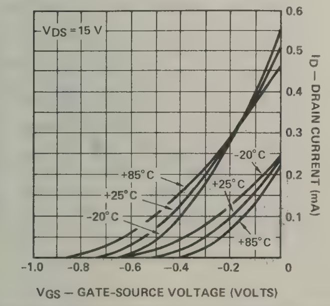
Common Source Input Capacitance vs Gate-Source Voltage



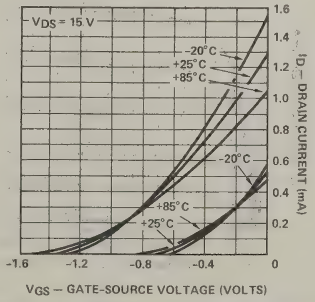
Noise Voltage vs Frequency



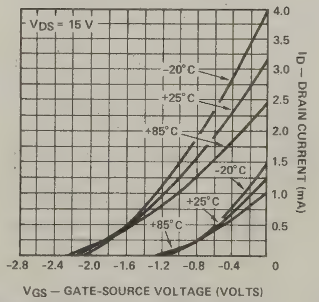
Transfer Characteristics



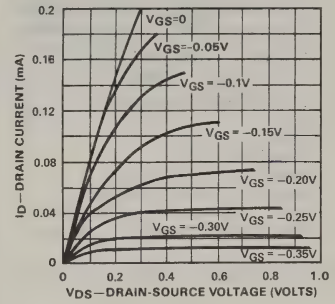
Transfer Characteristics

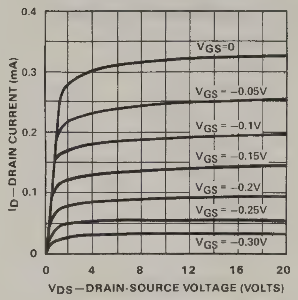


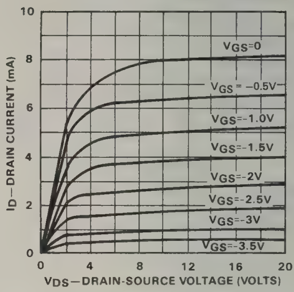
Transfer Characteristics

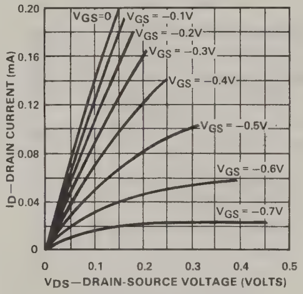


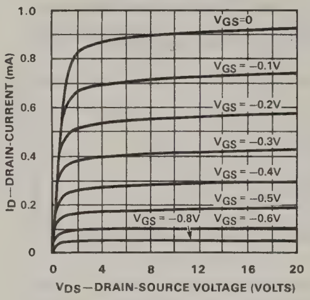
PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

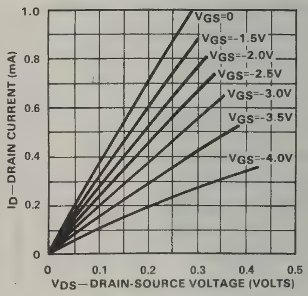

Output Characteristic ($V_{GS(off)}$ = –0.5V)

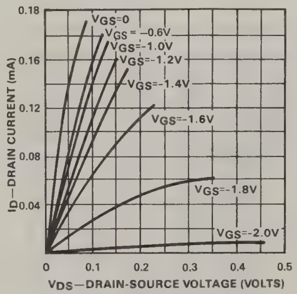

Output Characteristic ($V_{GS(off)}$ = –0.5V)

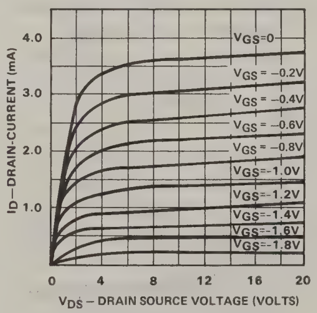

Output Characteristic ($V_{GS(off)}$ = –4.2V)

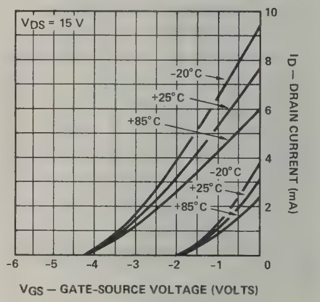

Output Characteristic ($V_{GS(off)}$ = –1.0V)

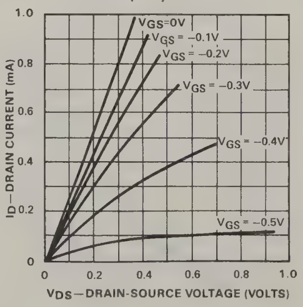

Output Characteristic ($V_{GS(off)}$ = –1.0V)

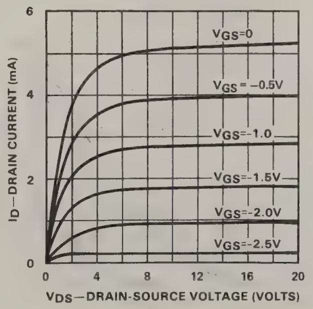

Output Characteristic ($V_{GS(off)}$ = –4.2V)

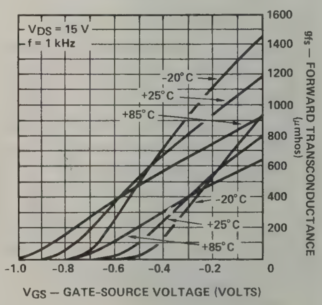

Output Characteristic ($V_{GS(off)}$ = –2.3V)


Output Characteristic ($V_{GS(off)}$ = –2.3V)

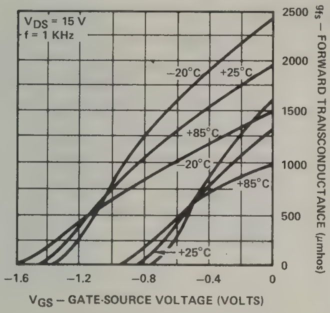

Transfer Characteristics

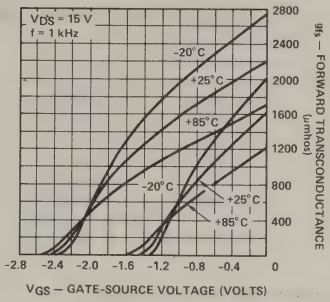

Output Characteristic ($V_{GS(off)}$ = –3.0V)

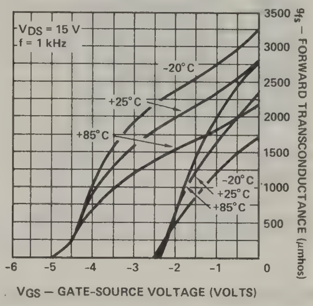

Output Characteristic ($V_{GS(off)}$ = –3.0V)

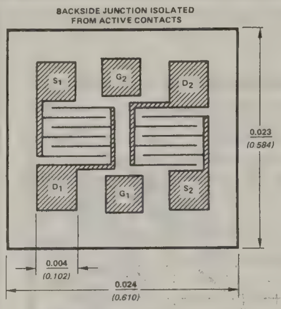

Transconductance Characteristics

PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)


Transconductance Characteristics


Transconductance Characteristics


Transconductance Characteristics



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

monolithic dual n-channel JFET designed for . . .

Siliconix

- General Purpose Differential Amplifiers

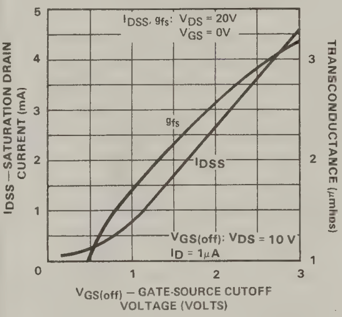
BENEFITS:

- Low Cost
- High Input Impedance

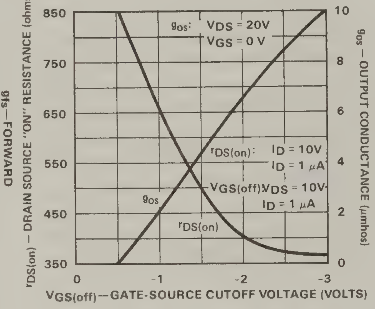
TYPE	PACKAGE	PRINCIPAL DEVICES
Dual	TO-71	2N3954-55, 2N3954A-55A, 2N3956-58, 2N5045-47, 2N5196-99, 2N5515-24, 2N5452-54 U231-35, U410-12
Dual	Chip	2N3955, 2N3956-58 2N5047, 2N5199 2N5454, U233-35 U411, 12

PERFORMANCE CURVES (25°C unless otherwise noted)

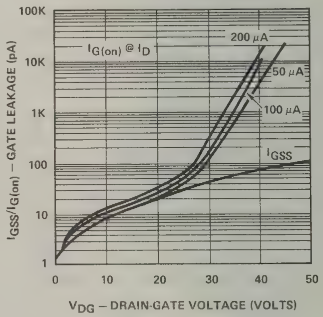
Drain Current & Transconductance vs Gate-Source Cutoff Voltage



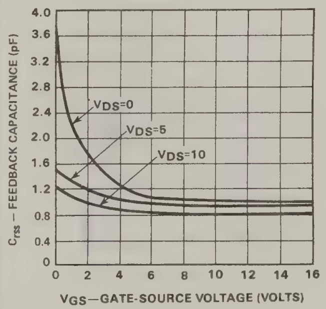
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



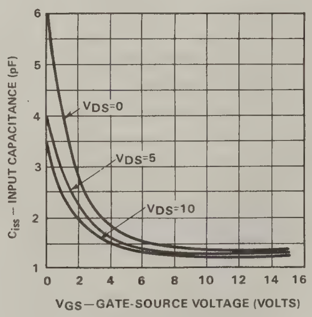
Gate Operating Current vs Drain Current



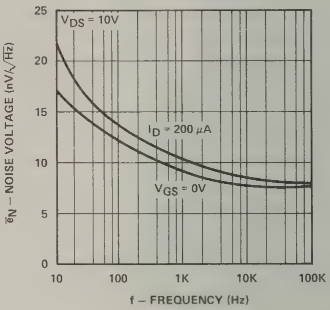
Common Source Reverse Feedback Capacitance vs Gate Source Voltage



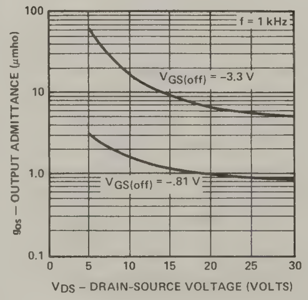
Common Source Input Capacitance vs Gate-Source Voltage



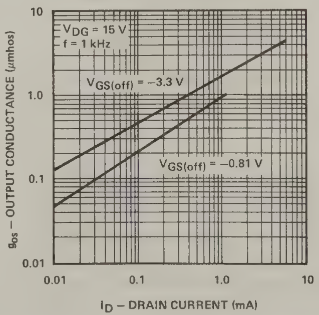
Equivalent Input Noise Voltage vs Frequency



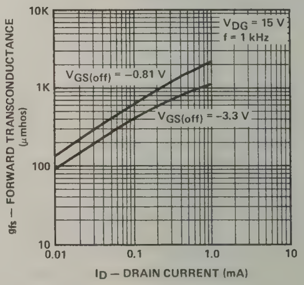
Common Source Output Admittance vs Drain-Source Voltage



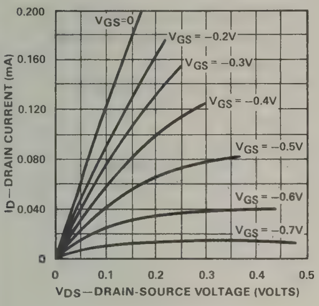
Common-Source Output Conductance vs Drain Current



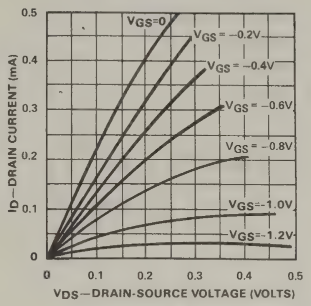
Common Source Forward Transconductance vs Drain Current



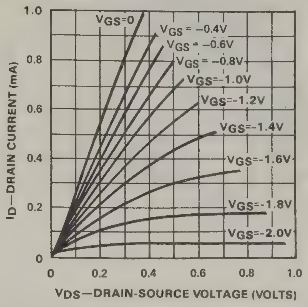
PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)



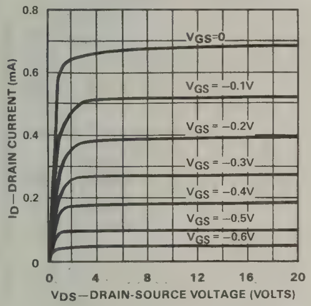
Output Characteristic ($V_{GS(off)} = -1.0V$)



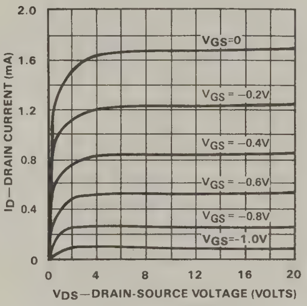
Output Characteristic ($V_{GS(off)} = -1.5V$)



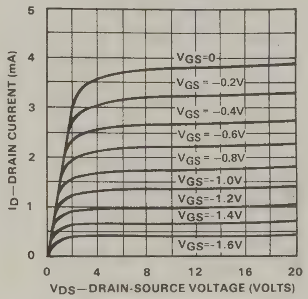
Output Characteristic ($V_{GS(off)} = -2.3V$)



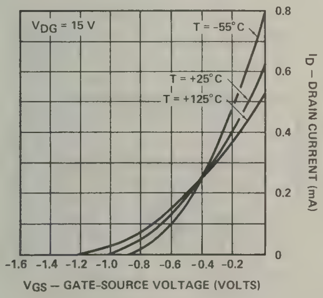
Output Characteristic ($V_{GS(off)} = -1.0V$)



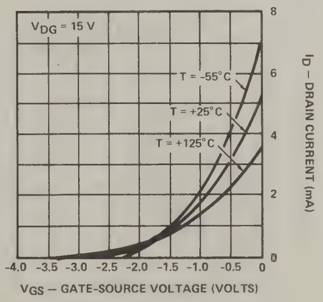
Output Characteristic ($V_{GS(off)} = -1.5V$)



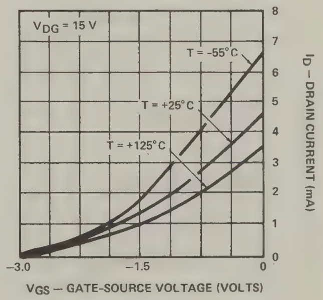
Output Characteristic ($V_{GS(off)} = -2.3V$)



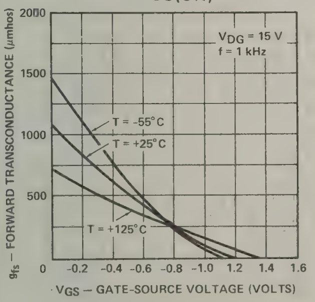
Transfer Characteristics Low $V_{GS(off)}$



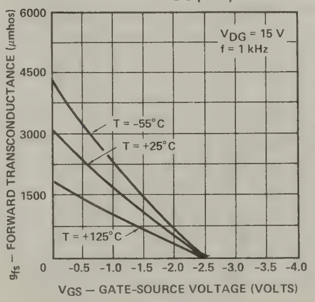
Transfer Characteristics Medium $V_{GS(off)}$



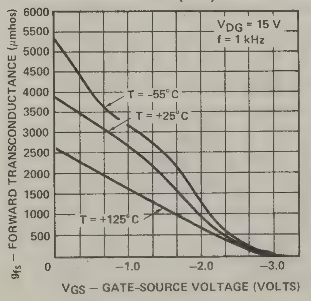
Transfer Characteristics High $V_{GS(off)}$



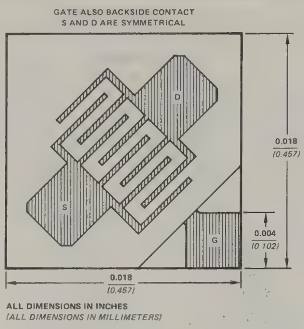
Transconductance Characteristics Low $V_{GS(off)}$



Transconductance Characteristics Medium $V_{GS(off)}$



Transconductance Characteristics High $V_{GS(off)}$



n-channel JFET
designed for . . .

Siliconix

- Small Signal Amplifiers
- VHF Amplifiers
- Oscillators
- Mixers
- Switches

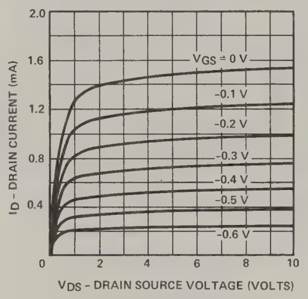
BENEFITS:

- Wide Input Dynamic Range
  High I_G Breakpoint Voltage
- High Gain
- Low Insertion Loss Switches

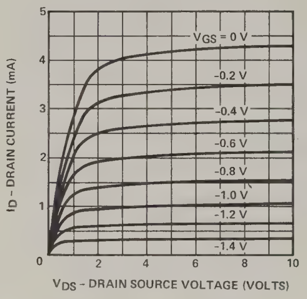
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	2N3821-4, 2N3921-22, 2N4220-2 2N4220A-2A, 2N4223-24
Single	TO-92	2N3819, 2N5457-9 MPF109, MPF111
Single	Chip	All of the above

PERFORMANCE CURVES (25°C unless otherwise noted)

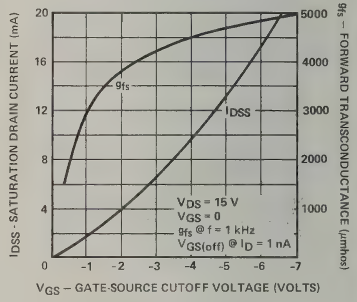
Output Characteristic
($V_{GS(off)} = -0.8V$)



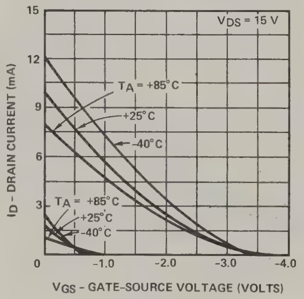
Output Characteristic
($V_{GS(off)} = -2.0V$)



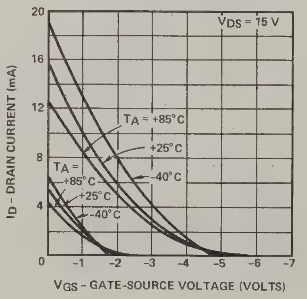
Drain Current & Transconductance vs
Gate-Source Cutoff Voltage



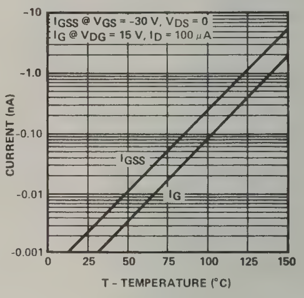
Transfer Characteristic



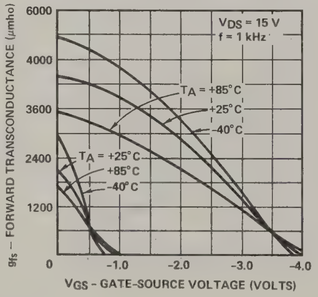
Transfer Characteristics



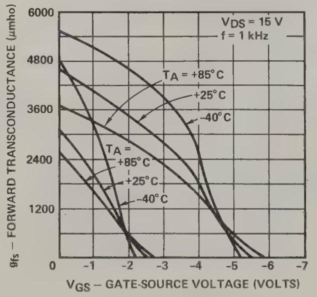
Leakage Currents vs
Ambient Temperature



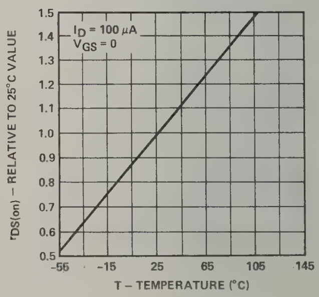
Transconductance Characteristics



Transconductance Characteristics

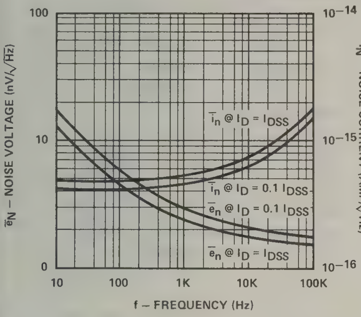


'ON' Resistance vs
Ambient Temperature

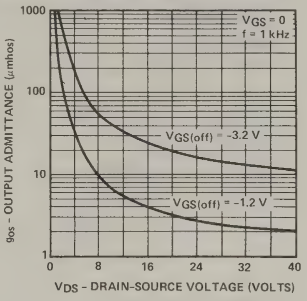


PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

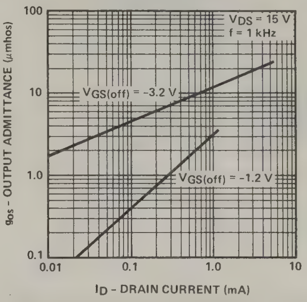
Equivalent Input Noise Voltage and Noise Current vs Frequency



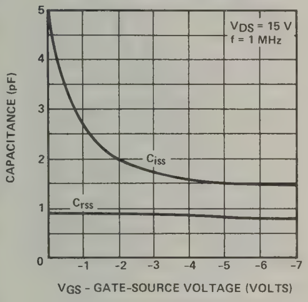
Common-Source Output Admittance vs Drain-Source Voltage



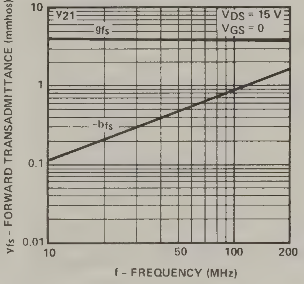
Common-Source Output Admittance vs Drain Current



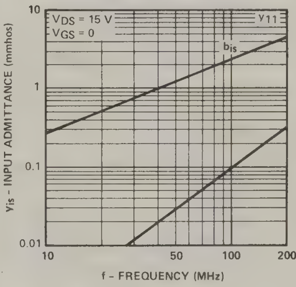
Common-Source Capacitances vs Gate-Source Voltage



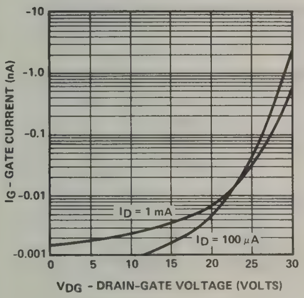
Common-Source Forward Transadmittance vs Frequency



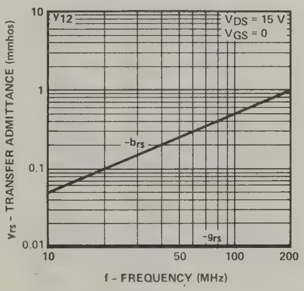
Common-Source Input Admittance vs Frequency



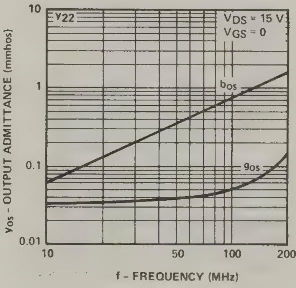
Gate Operating Current vs Drain-Gate Voltage



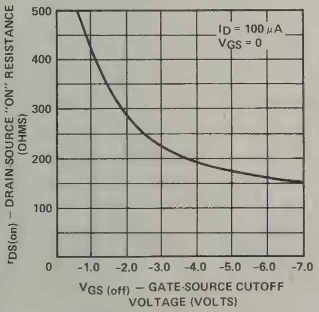
Common-Source Reverse Transfer Admittance vs Frequency



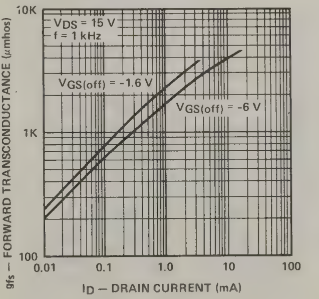
Common-Source Output Admittance vs Frequency



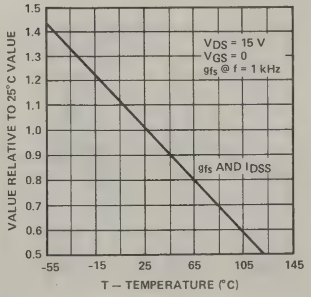
Static Drain-Source 'ON' Resistance vs Gate-Source Cutoff Voltage

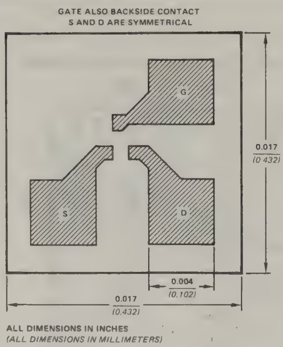


Common-Source Forward Transconductance vs Drain Current



Drain Current and Transconductance vs Ambient Temperature





n-channel JFET
designed for . . .

- Ultra-High Input Impedance Amplifiers
  - Electrometers
  - pH Meters
  - Smoke Detectors

TYPE	PACKAGE
Single	TO-72
Single	TO-92
Dual	TO-78
Single	Chip

BENEFITS:

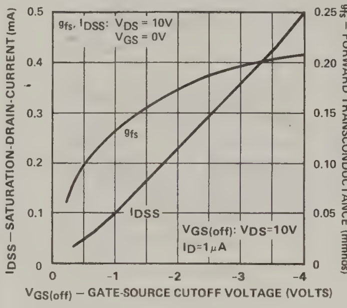
- Low Power
  $I_{DSS} < 90\ \mu A$ (2N4117)
- High Input Impedance
  $I_G < 1$ pA (2N5906-09)

PRINCIPAL DEVICES

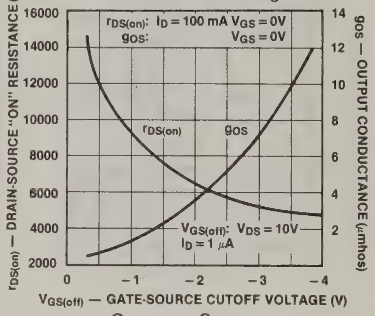
2N4117-9, 2N4117A-9A,
FN4117-18, FN4117A-18A, VCR7N
PN4117 Thru PN4120
PN4117A Thru 4120A
2N5902-9
All singles above,
Dual - 2N5905CHP, 2N5909CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

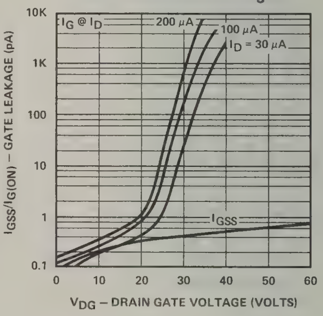
Drain Current and Transconductance vs Gate-Source Cutoff Voltage



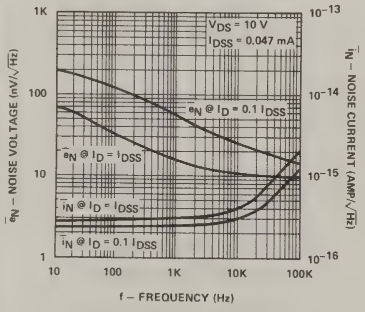
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



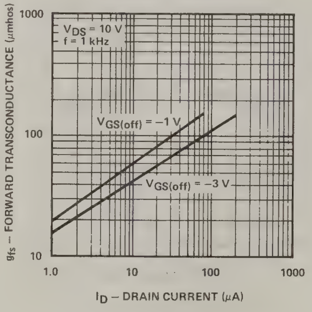
Gate Operating Current vs Drain-Gate Voltage



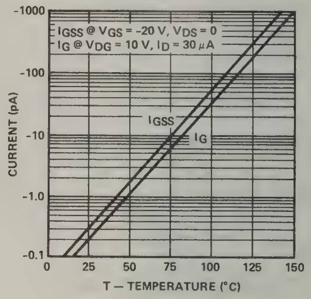
Equivalent Input Noise Voltage and Noise Current vs Frequency



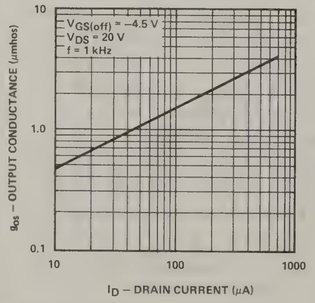
Common-Source Forward Transconductance vs Drain Current



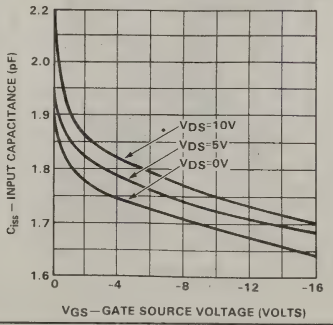
Leakage Currents vs Ambient Temperature



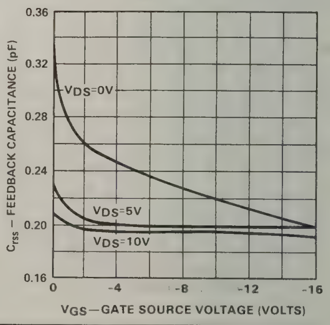
Common-Source Output Conductance vs Drain Current



Input Capacitance vs Gate-Source Voltage

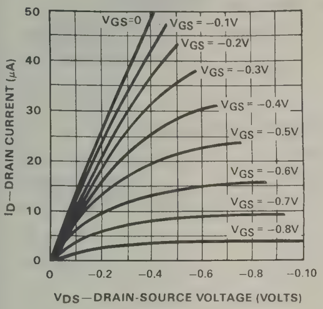


Reverse Feedback Capacitance vs Gate Source Voltage

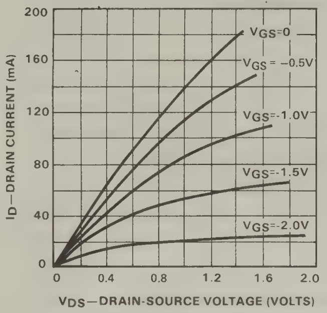


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

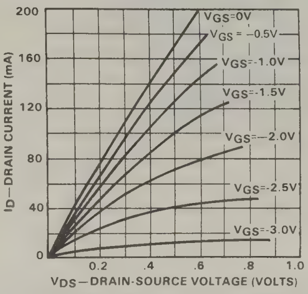
Output Characteristic ($V_{GS(off)} = -1.0V$)



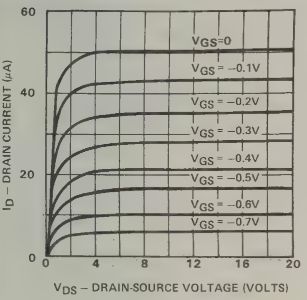
Output Characteristic ($V_{GS(off)} = -2.5V$)



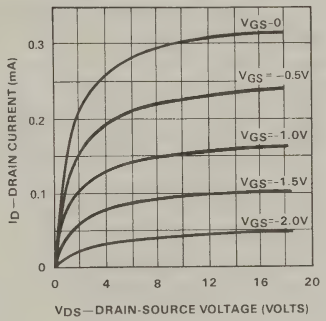
Output Characteristic ($V_{GS(off)} = -3.5V$)



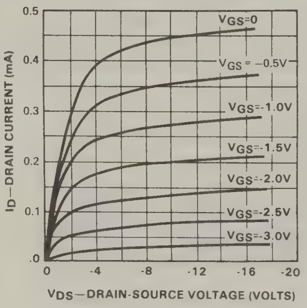
Output Characteristic ($V_{GS(off)} = -1.0V$)



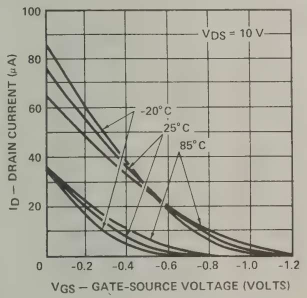
Output Characteristic ($V_{GS(off)} = -2.5V$)



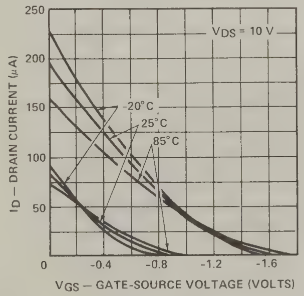
Output Characteristic ($V_{GS(off)} = -3.5V$)



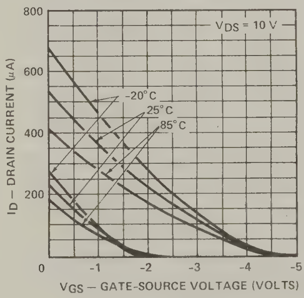
Transfer Characteristics



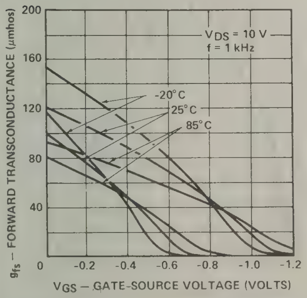
Transfer Characteristics



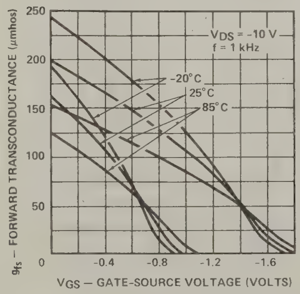
Transfer Characteristics



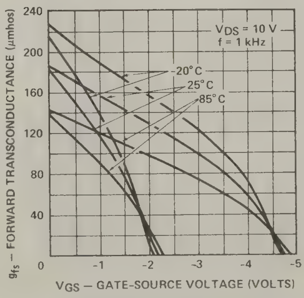
Transconductance Characteristics

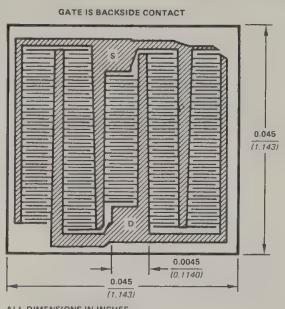


Transconductance Characteristics



Transconductance Characteristics





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET
designed for . . .

Siliconix

- Analog Switches
- Commutators
- Choppers

BENEFITS:

- Very Low Insertion Loss
  $r_{DS(on)} < 2.5$ Ohms (U290)
- High Off-Isolation

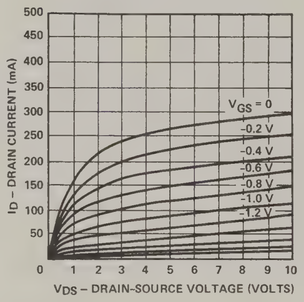
TYPE	PACKAGE
Single	TO-52
Single	TO-92
Single	Chip

PRINCIPAL DEVICES

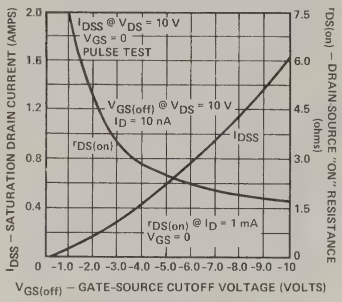
U290-1
J105-7
U290CHP-1CHP, J105CHP-7CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

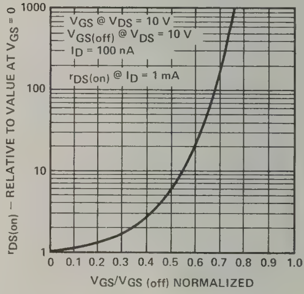
Output Characteristic



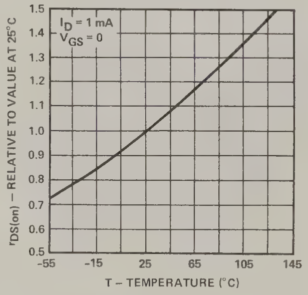
Saturation Drain Current and Drain-Source 'ON' Resistance vs Gate-Source Cutoff Voltage



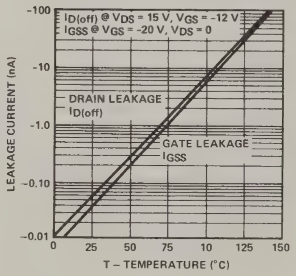
Drain-Source Resistance vs Normalized Gate-Source Voltage



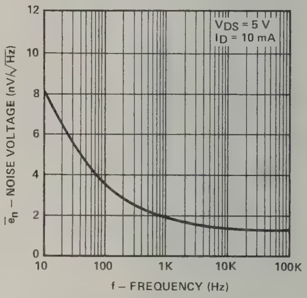
Drain-Source 'ON' Resistance vs Ambient Temperature



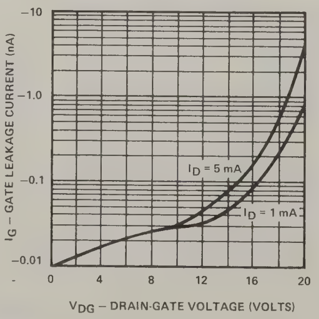
Leakage Currents vs Ambient Temperature



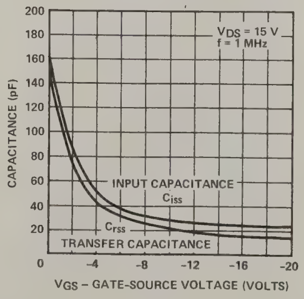
Equivalent Input Noise Voltage vs vs Frequency



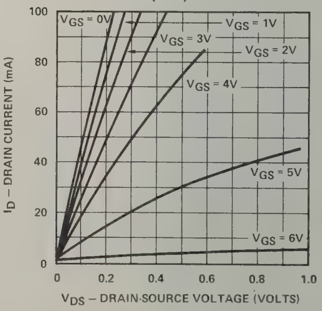
Leakage Current vs Drain-Gate Voltage

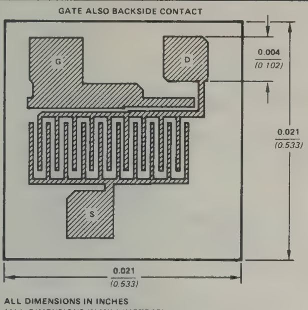


Common-Source Capacitance vs Gate-Source Voltage



Output Characteristic ($V_{GS(off)} = -7.5V$)





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET *designed for . . .*

- VHF/UHF Amplifiers
- Front End High Sensitivity Amplifiers
- Oscillators
- Mixers

BENEFITS

- Industry Standard
- High Power Gain
  16 dB at 100 MHz, Common Gate
  11 dB at 450 MHz, Common Gate

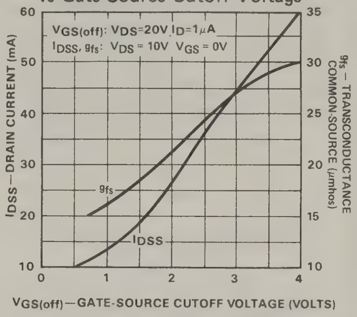
BENEFITS

- Low Noise
  3 dB Noise Figure at 450 MHz
- Wide Dynamic Range
  Greater Than 100 dB
- 75 Ohm Input Match Common Gate

Siliconix

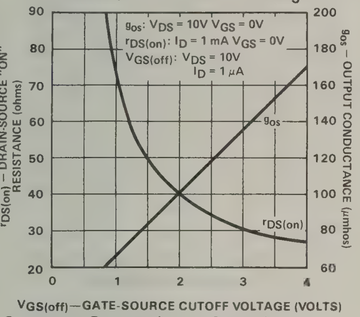
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-52	U308-10
Single	TO-72	U311
Single	TO-92	J308-10
Dual	TO-99	U430-1
Single	Chip	J308CHP-10CHP, U308CHP-10CHP, U311CHP
Dual	Chip	U430CHP-1CHP

Drain Current & Transconductance vs Gate-Source Cutoff Voltage

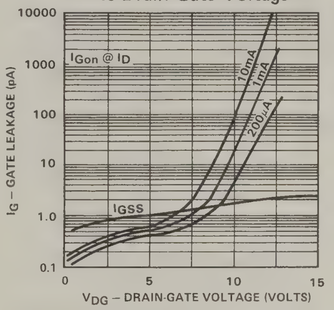


PERFORMANCE CURVES (25°C unless otherwise noted)

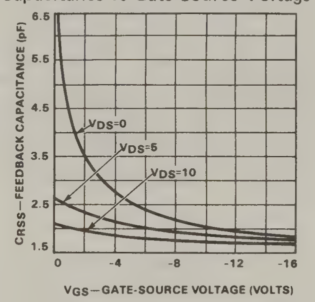
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



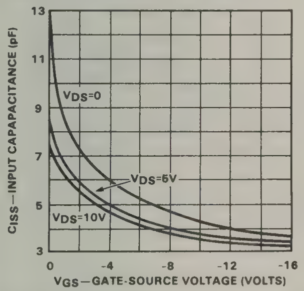
Gate Operating Current vs Drain-Gate Voltage



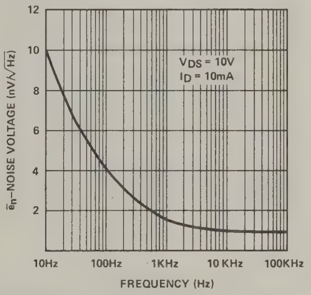
Common Source Reverse Feedback Capacitance vs Gate Source Voltage



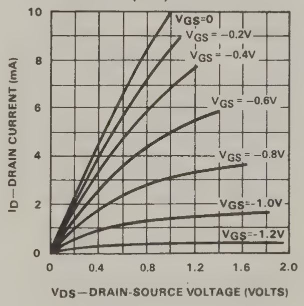
Common Source Input Capacitance vs Gate-Source Voltage



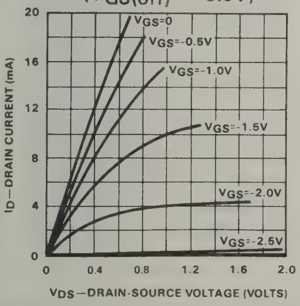
Noise Voltage vs Frequency



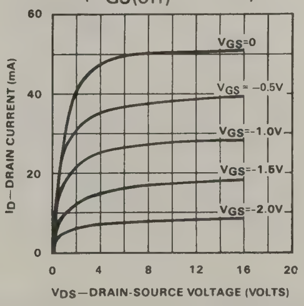
Output Characteristic ($V_{GS(off)} = -1.7V$)



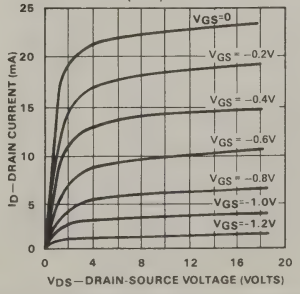
Output Characteristic ($V_{GS(off)} = -3.0V$)



Output Characteristic ($V_{GS(off)} = -3.0V$)

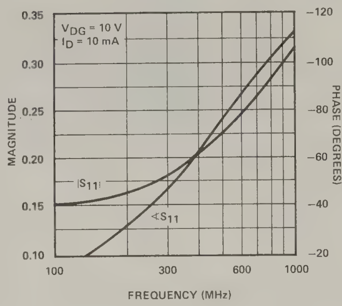


Output Characteristic ($V_{GS(off)} = -1.7V$)

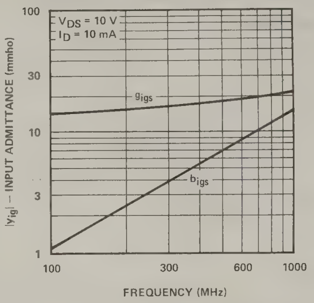


PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

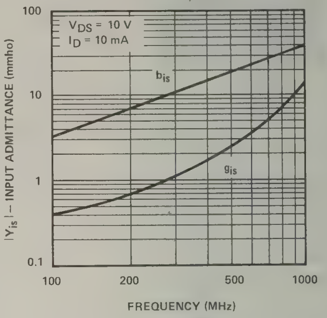
Forward Reflection Coefficient Common Gate



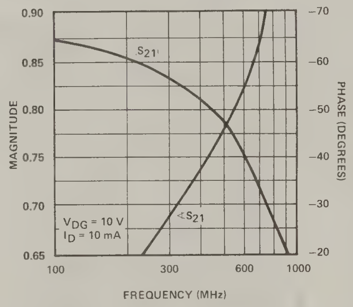
Input Admittance Common Gate



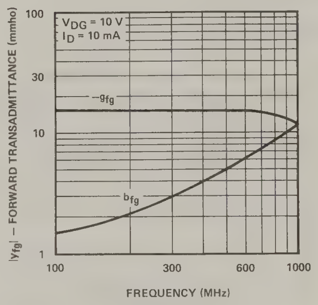
Input Admittance Common Source



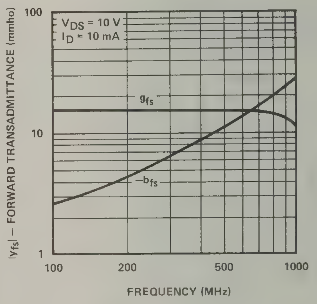
Forward Transmission Coefficient Common Gate



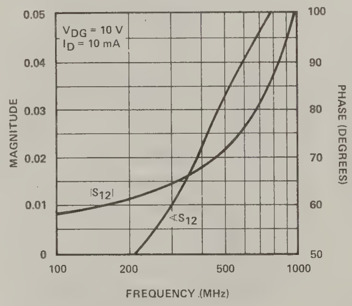
Forward Transfer Admittance Common Gate



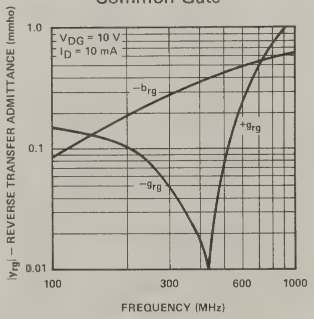
Forward Transfer Admittance Common Source



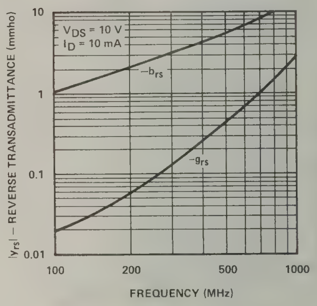
Reverse Transmission Coefficient Common Gate



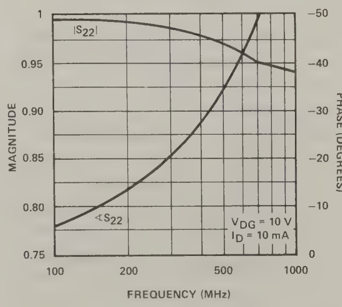
Reverse Transfer Admittance Common Gate



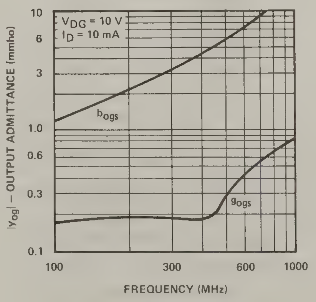
Reverse Transfer Admittance Common Source



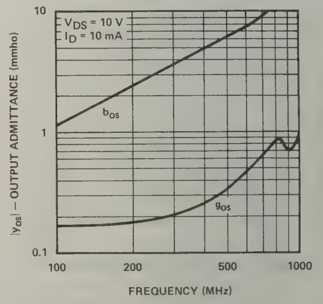
Reverse Reflection Coefficient Common Gate

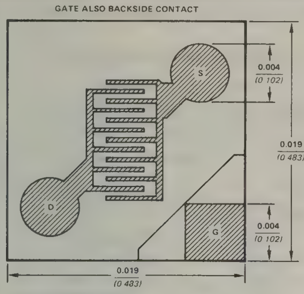


Output Admittance Common Gate



Output Admittance Common Source





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET
designed for . . .

Siliconix

- High Frequency Amplifiers
- Mixers
- Oscillators

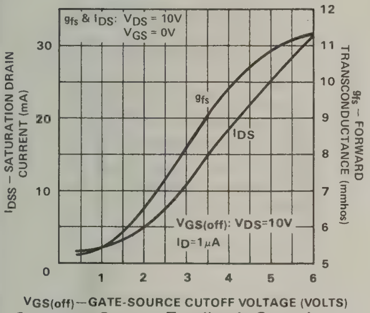
BENEFITS:

- High Power Gain
- Low Input Capacitance

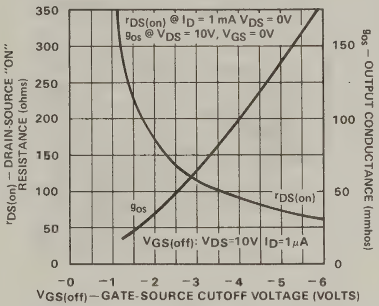
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-92	J300, J210-12
Dual	TO-78	2N5911-12, U257 U443-U444
Dual	TO-71	U440-41
Single	Chip	J300, J210-2CHP
Dual	Chip	2N5912CHP, U257CHP U441CHP, U444CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

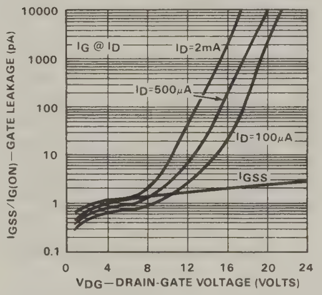
Drain Current and Transconductance vs Gate-Source Cutoff Voltage



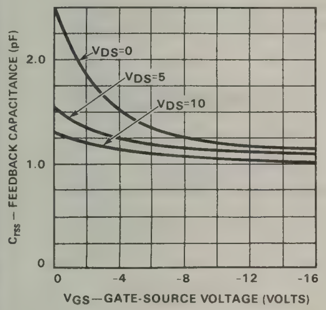
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



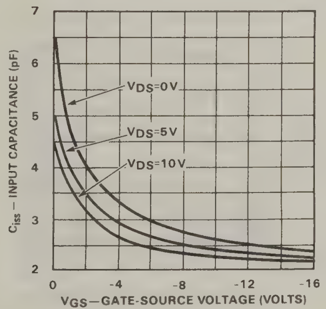
Gate Operating Current vs Drain-Gate Voltage



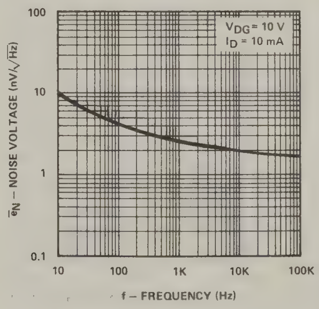
Common Source Feedback Capacitance vs Gate-Source Voltage



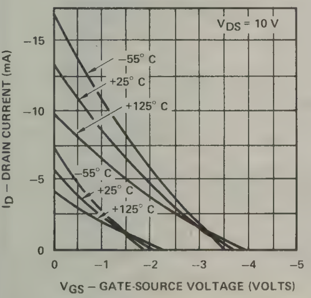
Common Source Input Capacitance vs Gate-Source Voltage



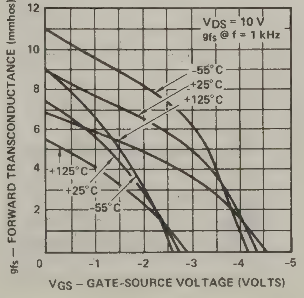
Equivalent Input Noise Voltage vs Frequency



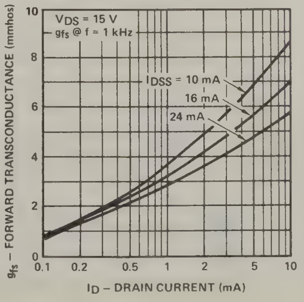
Transfer Characteristics



Transconductance Characteristics

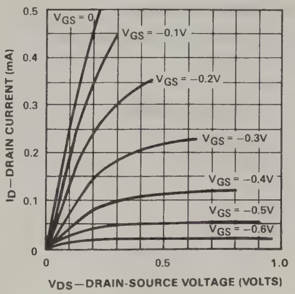


Forward Transconductance vs Drain Current

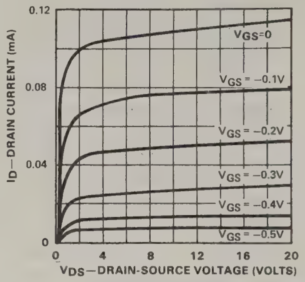


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

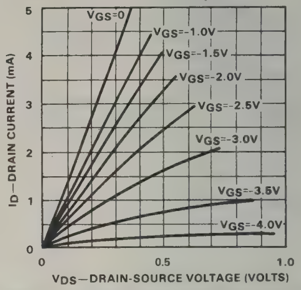
Output Characteristic
($V_{GS(off)}$ = −0.8V)



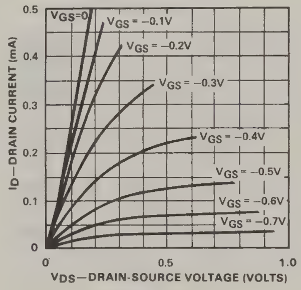
Output Characteristic
($V_{GS(off)}$ = −0.8V)



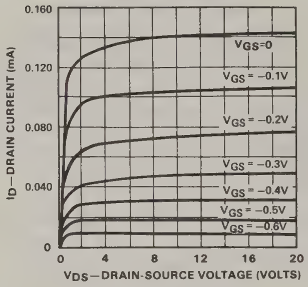
Output Characteristic
($V_{GS(off)}$ = −5.0V)



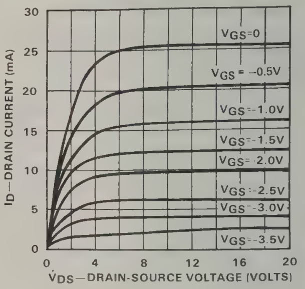
Output Characteristic
($V_{GS(off)}$ =-1.0V)



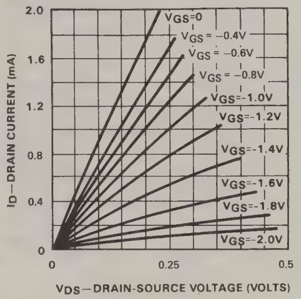
Output Characteristic
($V_{GS(off)}$ =-1.0V)



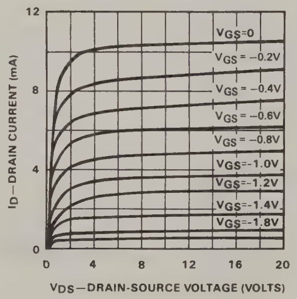
Output Characteristic
($V_{GS(off)}$ = −5.0V)



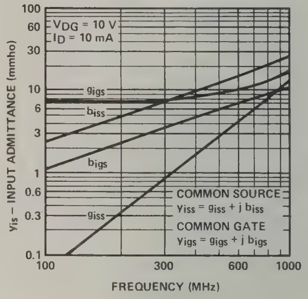
Output Characteristic
($V_{GS(off)}$ = −2.8V)



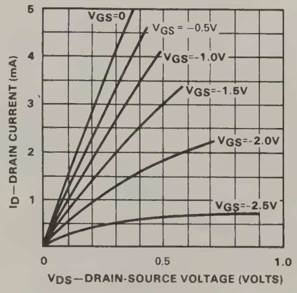
Output Characteristic
($V_{GS(off)}$ = −2.8V)



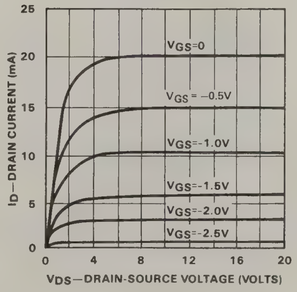
Input Admittance vs Frequency



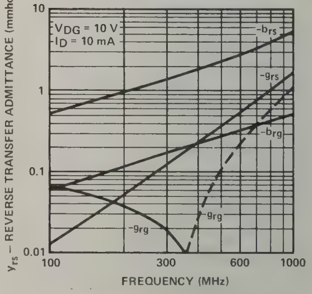
Output Characteristic
($V_{GS(off)}$ = −3.5V)



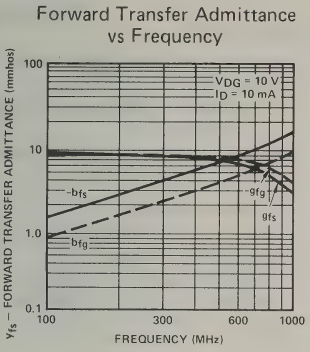
Output Characteristic
($V_{GS(off)}$ = −3.5V)

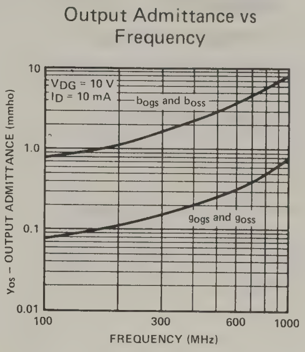


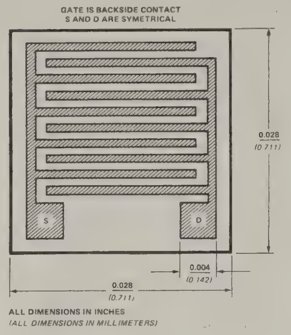
Reverse Transfer Admittance vs Frequency



PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)


Forward Transfer Admittance vs Frequency


Output Admittance vs Frequency



Siliconix

p-channel JFET
designed for . . .

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

BENEFITS:

- Low Insertion Loss in Switching Systems $R_{ON} < 75\ \Omega$ (2N5114)
- Short Sample and Hold Aperture Time $C_{rss} < 7$ pF
- High Off-Isolation $I_{D(off)} < 500$ pA

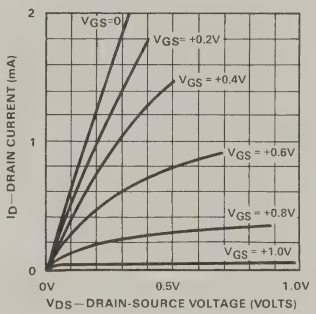
TYPE	PACKAGE
Single	TO-18
Single	TO-92
Single	Chip

PRINCIPAL DEVICES

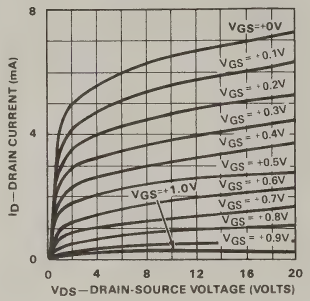
2N5018-19, 2N5114-16, U304-6, VCR3P
J174-7, J270-1, P1086-87
2N5018CHP-19CHP, 2N5114CHP-16CHP
U304CHP-6CHP, P1086CHP-87CHP
J270CHP-271CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

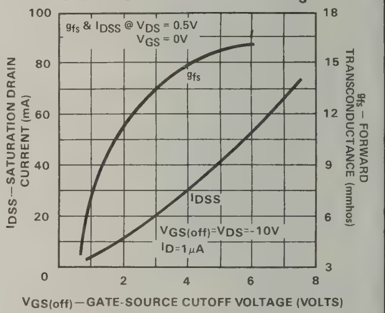
Output Characteristic ($V_{GS(off)} = +1.5V$)



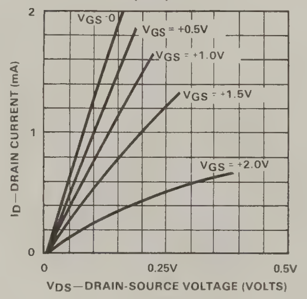
Output Characteristic ($V_{GS(off)} = +1.5V$)



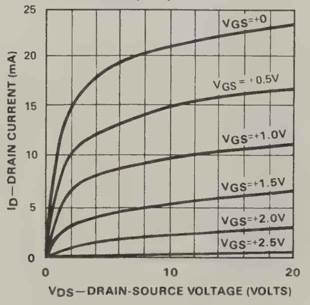
Drain Current & Transconductance vs Gate-Source Cutoff Voltage



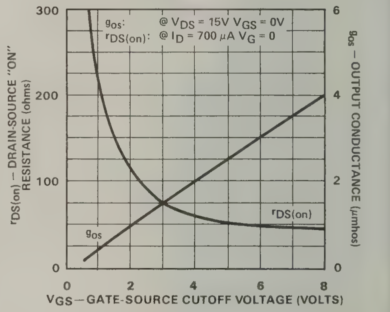
Output Characteristic ($V_{GS(off)} = +3.0V$)



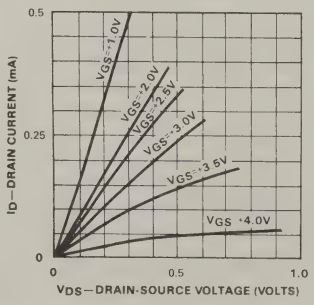
Output Characteristic ($V_{GS(off)} = +3.0V$)



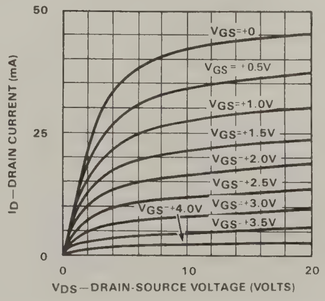
On Resistance and Output Conductance vs Gate-Source Voltage



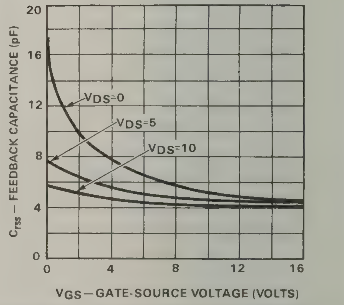
Output Characteristic ($V_{GS(off)} = +5.0V$)



Output Characteristic ($V_{GS(off)} = +5.0V$)

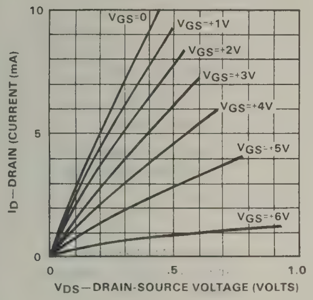


Common Source Reverse Feedback Capacitance vs Gate Source Voltage

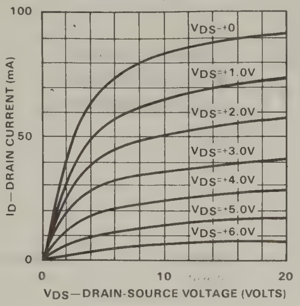


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

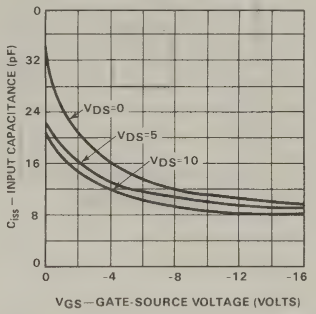
Output Characteristic ($V_{GS(off)}$ = +8.0V)



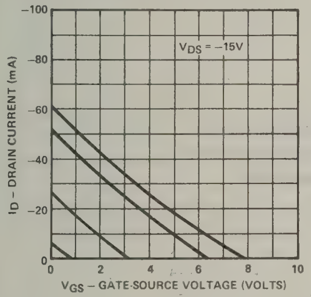
Output Characteristic ($V_{GS(off)}$ = +8.0V)



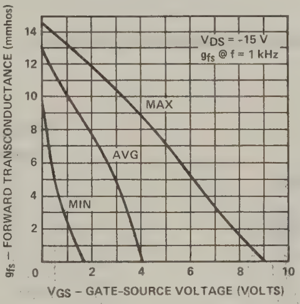
Common Source Input Capacitance vs Gate-Source Voltage



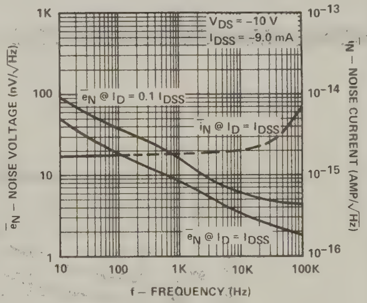
Transfer Characteristics



Transconductance Characteristics

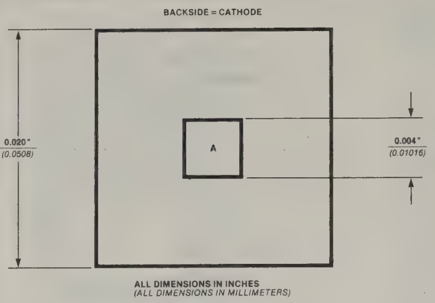


Equivalent Input Noise Voltage and Noise Current vs Frequency



high voltage protection diode

designed for . . .



- **Limiting Current**
- **Voltage Protection**
- **Voltage Decoupling**

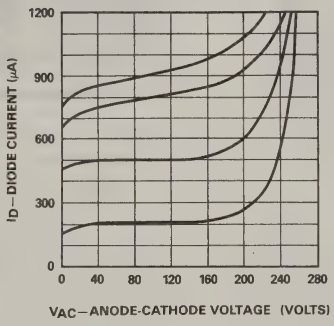
BENEFITS

- Series element
- Two terminals
- Simple to use
- High breakdown voltage (JR240V—240 volts)
- Low Cost

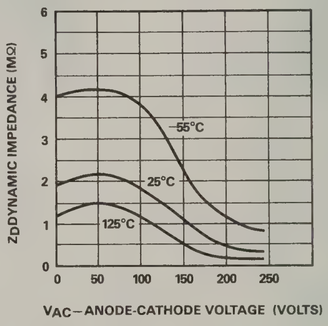
TYPE	**PACKAGE**	**PRINCIPAL DEVICES**
Single	TO-92	JR135V, JR170V, JR200V JR220V, JR240V

PERFORMANCE CURVES (25°C unless otherwise specified)

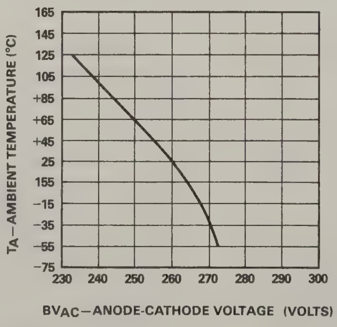
Output Characteristic



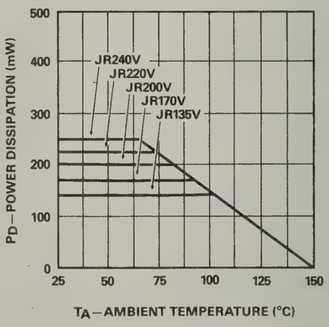
Dynamic Impedance Vs. Anode-Cathode Voltage at Temperature



Breakdown Voltage Vs. Temperature



Free Air Temperature Dissipation Derating Curve



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APPLICATION NOTE

An Introduction to FETs

INTRODUCTION

The basic principle of the field-effect transistor (FET) has been known since J.E. Lilenfeld's patent of 1925. The theoretical description of a FET made by Schockley in 1952 paved the way for development of a classic electronic device which provides the designer with the means by which he can accomplish nearly every circuit function. The field-effect transistor earlier was known as a "unipolar" transistor, and the term refers to the fact that current is transported by carriers of one polarity (majority), whereas in the conventional bipolar transistor carriers of both polarities (majority and minority) are involved.

This Application Note provides an insight into the nature of the FET, and touches briefly on its basic characteristics, terminology and parameters, and typical applications.

The following list of FET applications indicates the versatility of the FET family:

Amplifiers
Small Signal
Low Distortion
High Gain
Low Noise
Selective
D.C.
High-Frequency

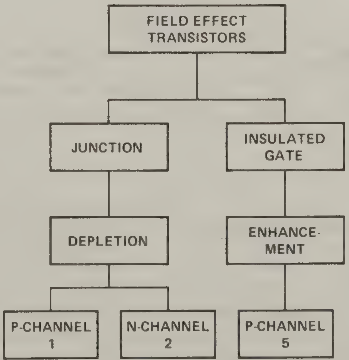
Switches
Chopper-type
Analog Gate
Commutator

Current Limiters
Voltage-Controlled Resistors
Mixers
Oscillators

This very wide range of FET applications by no means implies that the device will replace the more widely-known bipolar transistor in every case. The simple fact is that FET characteristics – which are very different from those of bipolar devices – can often make possible the design of technically superior (and sometimes cheaper) circuits. This comment applies not only to networks employing discrete devices and conventional components such as resistors and capacitors, but also extends to both linear and digital integrated circuits. In fact, FET technology today allows a greater packaging density in large-scale integrated circuits (LSI) than would ever be possible with bipolar devices.

(Although there is no industry-accepted definition of LSI, apparently when the equivalent circuit of an IC contains more than 1,000 active elements (500 gates) or is "very complex", the end product may be called LSI. With a typical LSI chip measuring less than 200 x 200 mils, this is high-density packaging indeed.)

The family tree of FET devices (Figure 1) may be divided into two main branches, junction FETs (JFETs) and Insulated Gate FETs (or MOSFETs, *metal-oxide-silicon field-effect transistors*). Junction FETs are inherently depletion-mode devices, and are available in both P- and N-Channel configurations. MOSFETs are available in both enhancement or depletion modes, and exist as both N- and P-Channel devices. The two main FET groups depend on different phenomena for their operation, and will be discussed separately.

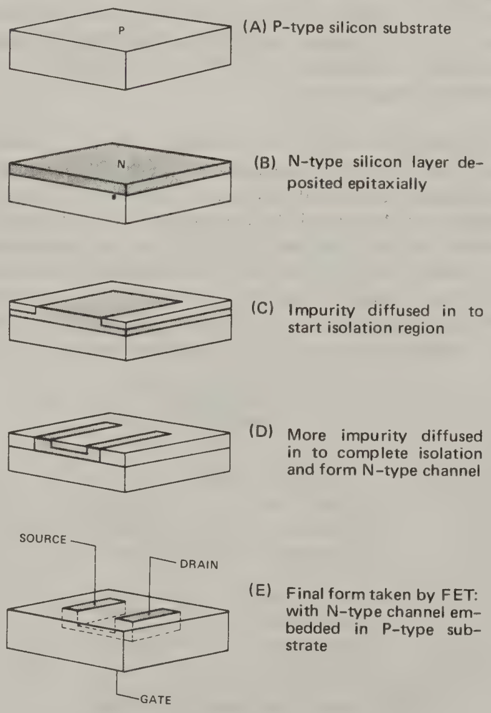


FET Family Tree
Figure 1

Junction FETs

In its most elementary version, this transistor consists of a piece of high-resistivity semiconductor material (usually silicon) which constitutes a channel for the majority carrier flow. The magnitude of this current is controlled by a voltage applied to a *gate*, which is a reverse-biased PN junction formed along the channel. Implicit in this description is the fundamental difference between FET and bipolar devices: when the FET junction is reverse-biased the gate current is practically zero, whereas the base current of the bipolar transistor is always some value greater than zero. The FET is a high input resistance device, while the input resistance of the bipolar transistor is comparatively low. If the channel is doped with a donor impurity, N-type material is formed and the channel current will consist of electrons. If the channel is doped with an acceptor impurity, P-type material will be formed and the channel current will consist of holes. N-Channel devices have greater conductivity than P-Channel types, since electrons have higher mobility than do holes; thus N-Channel FETs tend to be more efficient conductors than their P-Channel counterparts.

Junction FETs are particularly suited to manufacture by modern planar epitaxial processes. Figure 2 shows this process in an idealized manner. First, N-type silicon is deposited epitaxially (single-crystal condensation surface) onto monocrystalline P-type silicon, so that crystal integrity is maintained. Then a layer of silicon dioxide is grown on the surface of the N-type layer, and the surface is etched so that an acceptor-type impurity can be diffused through into the silicon. The resulting cross-section is shown in Figure 2C, and demonstrates how a P-type annulus has been formed in the layer on N-type silicon. Figure 2D shows how a further sequence of oxide growth, etching, and diffusion can produce a channel of N-type material within the substrate.


P
(A) P-type silicon substrate
N
(B) N-type silicon layer deposited epitaxially
(C) Impurity diffused in to start isolation region
(D) More impurity diffused in to complete isolation and form N-type channel
SOURCE
DRAIN
GATE
(E) Final form taken by FET: with N-type channel embedded in P-type substrate

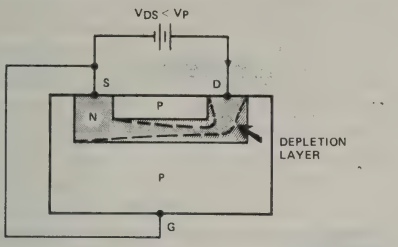
Idealized Manufacture of an N-Channel Junction FET
Figure 2

In addition to the channel material, a FET contains two ohmic (non-rectifying) contacts, the *source* and the *drain*. These are shown in Figure 2E. Since a symmetrical geometry is shown in the idealized FET chip, it is immaterial which contact is called the source and which is called the drain; the FET will conduct current equally well in either direction and the source and drain leads are usually interchangeable.

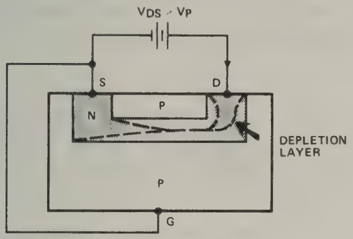
(For certain FET applications, such as amplifiers, an asymmetrical geometry is preferred for lower capacitance and improved frequency response. In these cases, the source and drain leads should not be interchanged.)

Figure 2E also shows how the N-Channel is embedded in the P-type silicon substrate, so that the gate above the channel becomes part of this substrate. Figure 3 shows how the FET functions. If the gate is connected to the source, then the applied voltage (V_{DS}) will appear between the gate and the drain. Since the PN junction is reverse-biased, little current will flow in the gate connection. The potential gradient established will form a *depletion* layer, where almost all the electrons present in the N-type channel will be swept away. The most depleted portion is in the high field between the gate and the drain, and the least-depleted area is between the gate and the source. Because the flow of current along the channel from the (positive) drain to the (negative) source is really a flow of free electrons from source to drain in the N-type silicon, the magnitude of this current will fall as more silicon becomes depleted of free electrons. There is a limit to the drain current (I_D) which increased V_{DS} can drive through the channel. This limiting current is known as I_{DSS} (*Drain-to-Source* current with the gate *Shorted* to the source). Figure 3B shows the almost complete depletion of the channel under these conditions.

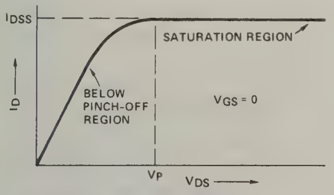
Figure 3C shows the output characteristics of an N-Channel JFET with the gate short-circuited to the source. The initial rise in I_D is related to the buildup of the depletion layer as V_{DS} increases. The curve approaches the level of the limiting current I_{DSS} when I_D begins to be *pinched off.* The physical meaning of this term leads to one definition of *pinch-off voltage,* V_P, which is the value of V_{DS} at which the maximum I_{DSS} flows.



(A) N-channel FET working below saturation ($V_{GS} = 0$). (Depletion shown only in channel region).



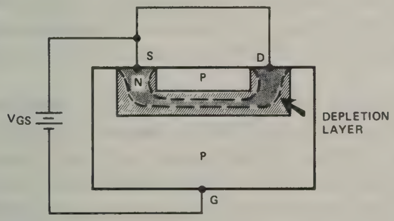
(B) N-channel FET working in saturation region ($V_{GS} = 0$)



(C) Idealized output characteristic for $V_{GS} = 0$.

Figure 3

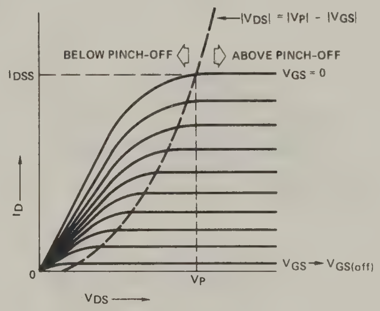
In Figure 4, consider the case where $V_{DS} = 0$, and where a negative voltage V_{GS} is applied to the gate. Again, a depletion layer has built up. If a small value of V_{DS} were now applied, this depletion layer would limit the resultant channel current to a value lower than would be the case for $V_{GS} = 0$. In fact, at a value of $|V_{GS}| \geqslant |V_P|$ the channel current would be almost entirely cut off. This cutoff voltage is referred to as the gate cutoff voltage, and may be expressed by the symbol V_P or by $V_{GS(off)}$. V_P has been widely used in the past, but $V_{GS(off)}$ is now more commonly accepted since it eliminates the ambiguity between gate cut-off and drain pinch-off. $V_{GS(off)}$ and V_P, strictly speaking, are equal in magnitude but opposite in polarity.



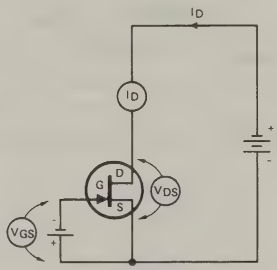
N-channel FET Showing Depletion Due To Gate-Source Voltage ($V_{DS} = 0$)
Figure 4

The mechanisms of Figure 3 and 4 react together to provide a family of output characteristics as shown in Figure 5A. The area below the pinchoff voltage locus is known as the triode or "below pinchoff" region; the area above pinchoff is often referred to as the pentode or saturation region. FET behavior in these regions is comparable to that of a power grid vacuum tube, and for this reason FETs operating in the saturation region may be used as excellent amplifiers. Note that in the "below pinchoff" region both V_{GS} and V_{DS} control the channel current, while in the saturation region V_{DS} has little effect and V_{GS} essentially controls I_D.

Figure 5B relates the curves of Figure 5A to the actual circuit arrangement, and shows the number of meters which may be connected to display the conditions relevant to any combination of V_{DS} and V_{GS}. Note that the direction of the arrow at the gate gives the direction of current flow for the forward-bias condition of the junction. In practice, however, it is always reverse-biased.



(A) Family of output characteristics for N-channel FET

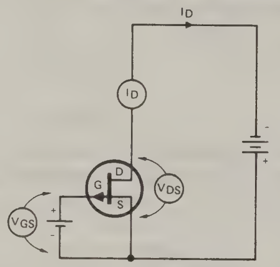


(B) Circuit arrangement for N-channel FET

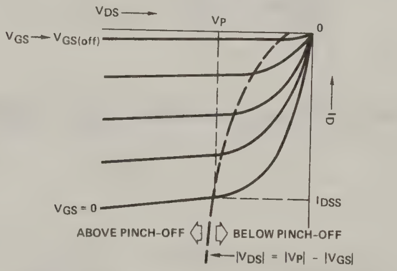
Figure 5

The P-Channel FET works in precisely the same way as does the N-Channel FET. In manufacture, the planar process is essentially reversed, with the acceptor impurity diffused first onto N-type silicon, and the donor impurity diffused later to form a second N-type region and leave a P-type channel. In the P-Channel FET, the channel current is due to hole movement, rather than to electron mobility. Consequently, all the applied polarities are reversed, along with their directions and the direction of current flow. Figure 6A shows the circuit arrangement for a P-Channel FET, and Figure 6B shows the output characteristics of the device. Note that the curves are shown in another quadrant than those of the N-Channel FET, in order to stress the current directions and polarities involved.

In summary, a junction FET consists essentially of a channel of semiconductor material along which a current may flow whose magnitude is a function of two voltages, V_{DS} and V_{GS}. When V_{DS} is greater than V_P, the channel current is controlled largely by V_{GS} alone, because V_{GS} is applied to a reverse-biased junction. The resulting gate current is extremely small.



(A) Circuit arrangement for P-channel FET

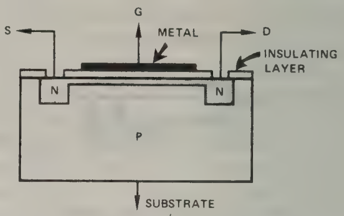


(B) Family of output characteristics for P-channel FET

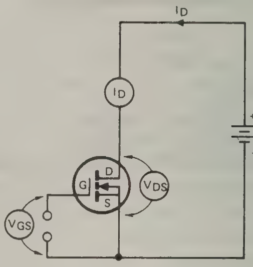
Figure 6

MOSFETs

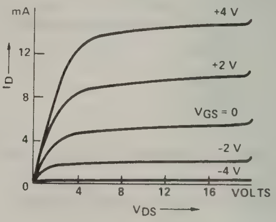
The metal-oxide-silicon FET (MOSFET) depends for its operation on the fact that it is not actually necessary to form a semiconductor junction on the channel of a FET in order to achieve gate control of the channel current. Instead, a metallic gate may be simply isolated from the channel by a thin layer of silicon dioxide, as shown in Figure 7A. Although the bottom of the insulating layer is in contact with the P-type silicon substrate, the physical processes which occur at this interface dictate that free electrons will accumulate at the interface, spontaneously forming an N-type channel. Thus a conducting path exists between the diffused N-type source and drain regions. Further, the MOSFET will behave in a manner similar to the N-Channel junction FET when a voltage of the correct polarity is applied to the channel, as in Figure 7B.



(A) Idealized cross-section through an N-channel depletion-type MOSFET



(B) Circuit arrangement for N-channel depletion MOSFET



(C) Family of output characteristics for the 2N3631 N-channel depletion MOSFET

Figure 7

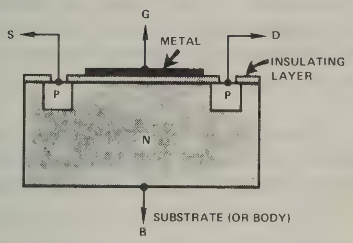
Output characteristics of an N-Channel MOSFET are shown in Figure 7C. Because there is no junction involved, V_{GS} can be reversed without engendering a gate current; the gate may be made either positive or negative with respect to the source. Under these circumstances, still more free electrons will be attracted to the channel region, and I_D will become greater than I_{DSS}. This mode of operation is represented by the higher members of the family of ourput characteristics. Because the application of a negative gate voltage causes the channel to be depleted of free electrons – thus reducing I_D – the device just described is called a *depletion-mode* MOSFET.

The foregoing has established that the depletion-mode MOSFET is a "normally-ON" device: when $V_{GS} = 0$, a conducting path exists between source and drain. In many circuits a "normally-OFF" device would be useful, a condition which leads to the concept of an *enhancement-mode* MOSFET. In the latter device, an increasing voltage applied to the gate will enhance channel conduction, and depletion will never occur, I_D being zero when $V_{GS} = 0$.

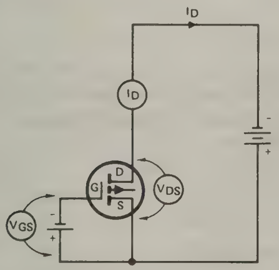
A P-Channel enhancement-mode MOSFET is shown in Figure 8. Here, an acceptor impurity has been diffused into an N-type substrate to form P-type source and drain regions. No conducting channel exists between the source and the drain, because no matter how the drain-source voltage is applied one of the PN junctions will always be reverse-biased. On the other hand, if a negative voltage is applied to the gate, a field will be set up in such a direction as to attract holes into the upper layer of the substrate and produce a P-type channel. A family of output characteristics for a typical MOSFET is shown in Figure 8C. The idealized cross-section illustrated in Figure 8A may be used to show how the characteristics of Figure 8C come about. Refer to Figure 9 for an extension of this phenomenon.

If a constant (negative) gate voltage, ($V_{GS(K)}$) is applied, then an essentially-uniform P-Channel depletion layer will be induced, as in Figure 9A. If a negative drain voltage is applied, then current, I_D, will flow through the drain. As $|V_{DS}|$ increases, I_D also increases. However, the voltage between the drain and the gate decreases, so that the thickness of the channel at the drain end is reduced as in Figure 9B. Therefore, the relationship of I_D versus V_{DS} will eventually reach a limiting value when $V_{DS} = V_{GS}$, and the channel becomes pinched off. This condition is shown in Figure 9C.

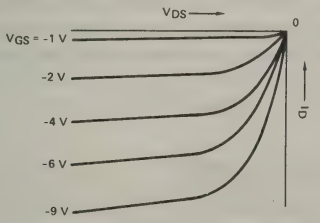
Different values of V_{GS} give rise to limiting values of I_D, so that the characteristic family of output curves which was shown in Figure 8 is realized. Characteristics of depletion-mode MOSFETs also come about for the same reason, except that members of the output characteristics family also exist for V_{GS} values of zero or reversed polarity. The P-Channel enhancement-mode MOSFET is currently the most popular member of the FET family in current use, and is in fact the basic element in many LSI integrated circuits.



(A) Idealized cross-section through a P-channel enhancement MOSFET

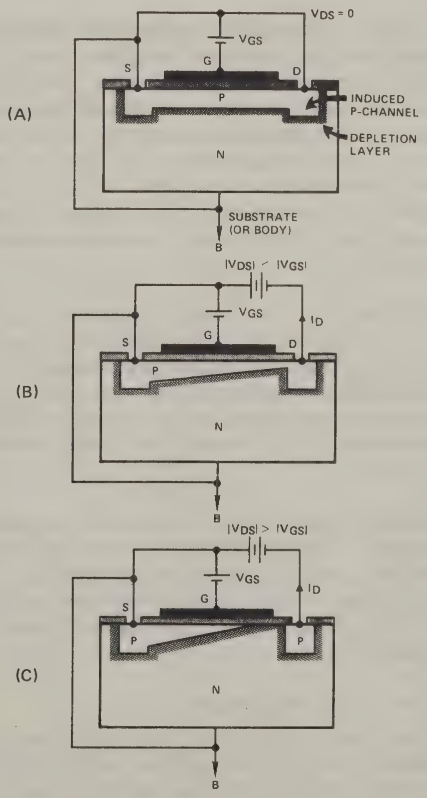


(B) Circuit arrangement for P-channel enhancement MOSFET



(C) Family of output characteristics for a P-channel enhancement MOSFET

Figure 8



Idealized approach of pinch-off,
(A) $V_{DS} = 0$, (B) $|V_{DS}| < |V_{GS}|$, (C) $|V_{DS}| > |V_{GS}|$

Figure 9

FET Characteristics

The FET enjoys certain inherent advantages over bipolar transistors because of the unique construction and method of operation of the field-effect device. These characteristics include:

- Low noise
- No thermal runaway
- Low distortion and negligible intermodulation products
- High input impedance at low frequencies
- Very high dynamic range (> 100 dB)
- Zero temperature coefficient Q point
- Junction capacitance independent of device current

The transfer function of a FET approximates to a square-law response, and the second and higher-order derivatives of g_m are near zero; thus strong second and negligible higher-order harmonics are produced. Intermodulation products are extremely low.

The input impedance of a FET is simply the impedance of a reverse-biased PN junction, which is on the order of 10^{10} to 10^{12} Ω. In practice, the input impedance is limited by the value of the shunt gate resistor used in a self-bias common-source circuit configuration. At RF frequencies, the input impedance drop is proportional to the square of the frequency; for example, in a 2N4416 FET, the input impedance would be 22K Ω at 100 MHz. Also, the input susceptance increases linearly with frequency, since it is a simple parasitic capacitance.

The FET has very high dynamic range, in excess of 100 dB. Thus it can amplify very small signals because it produces very little noise, or it can amplify very large signals because it has negligible intermodulation distortion products. It also has a zero temperature coefficient bias point (zero TC point) at which changes in temperature do not change the quiescent operating point.

Junction FET capacitances are more constant over wide current variation than are the same parameters in a bipolar device. This inherent stability allows high-frequency (VHF through L-band) oscillators to be built which are far more stable than oscillators using low-frequency crystals and multiplier stages.

FET Terminology and Parameters

Any introduction to the nature, behavior, and applications of field-effect transistors requires that certain questions be answered on FET electrical quantities and parameters – in particular, the most important parameters, and the means by which they can be measured. The following discussion will define specific FET parameters and their associated subscript notations, and present basic test circuits and results.

Major parameters include:

- I_{DSS} – Drain current with the gate shorted to the source
- $V_{GS(off)}$ – Gate-source cutoff voltage
- I_{GSS} – Gate-to-source current with the drain shorted to the source
- BV_{GSS} – Gate-to-source breakdown voltage with the drain shorted to the source
- g_{fs} – Common-source forward transconductance
- C_{gs} – Gate-source capacitance
- C_{gd} – Gate-drain capacitance

Special attention should be given to the subscript "s" because it has two different meanings and three possible uses. In FET notations, an "s" for the first or second subscript identifies the source terminal as a node point for voltage reference or current flow. However, when using triple subscript notation, an "s" for the third subscript does not refer to the FET source terminal. It is an abbreviation for "shorted", and signifies that all terminals not designated by the first two subscripts must be tied together and shorted to the common terminal, which is always the second subscript. Therefore, the term I_{GSS} refers to the gate-source current with the drain tied to the source.

Because of the typical low input and output admittance of the FET, four-pole admittance equations are commonly used to describe electrical characteristics of the FET:

$$I_1 = Y_{11}\ V_{11} + Y_{21}\ V_{22} \tag{1}$$

When Y_{11}, Y_{21}, Y_{12} and Y_{22} are defined as the input, reverse transfer, forward transconductance, and output admittances respectively, Equation 1 reduces to

$$\begin{aligned} i_1 &= y_i\ v_{11} + y_r\ v_{22} \\ i_2 &= y_f\ v_{11} + y_o\ v_{22} \end{aligned} \tag{2}$$

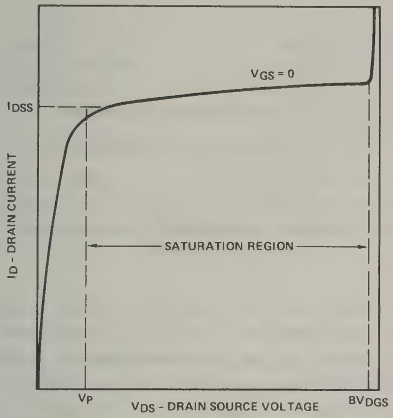
For a three-lead FET, 11 usually corresponds to the gate-source terminal and 22 corresponds to the drain-source terminal (i.e., the device is connected in the common-source mode). Thus

$$\begin{aligned} i_i &= y_{is}\ v_{gs} + y_{rs}\ v_{ds} \\ i_o &= y_{fs}\ v_{gs} + y_{os}\ v_{ds} \end{aligned} \tag{3}$$

Here, the second subscript for the y parameters designates the source lead as the common or ground terminal.

I_{DSS} – Drain Current at Zero Gate Voltage (I_D at $V_{GS} = 0$)

By itself, I_{DSS} merely refers to the drain current that will flow for any applied V_{DS} with the gate shorted to the source. However, when a particular value for V_{DS} is given, equal to or greater than V_P (see Figure 10), I_{DSS} indicates the drain saturation current at zero gate voltage. Some FET data sheets label I_{DSS} for V_{DS} greater than V_P as $I_{D(on)}$.



FET Characteristic at $V_{GS} = 0$
Figure 10

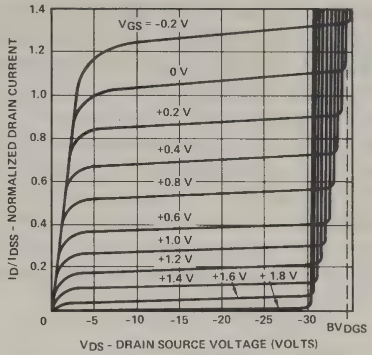
$V_{GS(off)}$ – Gate-Source Cutoff Voltage

The resistance of a semiconductor channel is related to its physical dimensions by $R = \rho L/A$, where

ρ = resistivity
L = length of the channel
A = W x T = cross-sectional area of channel

In the usual FET structure, L and W are fixed by device geometry, while channel thickness T is the distance between the depletion layers. The position of the depletion layer can be varied either by the gate-source bias voltage or by the drain-source voltage. When T is reduced to zero by any combination of V_{GS} and V_{DS}, the depletion layers from the opposite sides come in contact, and the a-c or incremental channel resistance, r_{DS}, approaches infinity. As earlier noted, this condition is referred to as "pinch-off" or "cutoff" because the channel current has been reduced to a very thin sheet, and current will no longer be conducted. Further increases in V_{DS} (up to the junction reverse-bias breakdown) will cause little change in I_D. Accordingly, the pinch-off region is also referred to as the pentode or "constant-current" region.

In Figure 10, pinch-off occurs with $V_{GS} = 0$. In Figure 11, V_{GS} controls the magnitude of the saturated I_D, with increases in V_{GS} resulting in lower values of constant I_D, and smaller values of V_{DS} necessary to reach the "knee" of the curve. The current scale in Figure 11 has been normalized to a specific value of I_{DSS}.



FET I_D vs V_D Output Characteristics
Figure 11

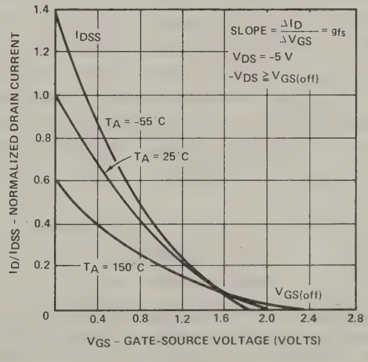
The knee of the curve is important to the circuit designer because he must know what minimum V_{DS} is needed to reach the pinch-off region with $V_{GS} = 0$. When appropriate bias voltage is applied to the gate, it will pinch off the channel so that no drain current can flow; V_{DS} has no effect until breakdown occurs. The specific amount of V_{GS} that produces pinch-off is known as the gate-source cutoff voltage, $V_{GS(off)}$.

$V_{GS(off)}$ Test Procedure

Although the magnitude of $V_{GS(off)}$ is equal to the pinch-off voltage, V_P, defined by the pinch-off knee in Figure 10, rapid curvature in the area makes it difficult to define any precise point as V_P. Taking a second derivative of V_{DS}/I_D would yield a peak corresponding to the inflection point at the knee, which approximates V_P. However, this is not a simple measurement for production quantities of devices. A better measure is to approach the cutoff point of the I_D versus V_{GS} characteristic. This is easier than trying to specify the location of the knee of the I_D versus V_{DS} output characteristic.

A typical transfer characteristic I_D versus V_{GS} is shown in Figure 12. The curve can be closely approximated by

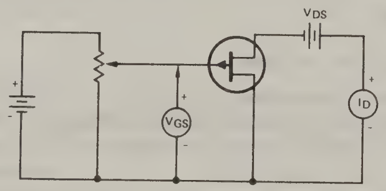
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 \qquad (4)$$



Typical I_D vs V_{GS} Transfer Characteristic
Figure 12

Equation 4 and Figure 12 indicate that at $V_{GS} = V_{GS(off)}$, $I_D = 0$. In a practical device, this cannot be true because of leakage currents. If I_D is reduced to less than 1 percent of I_{DSS}, V_{GS} will be within 10 percent of the $V_{GS(off)}$ value indicated by Equation 4. If I_D is reduced to 0.1 percent of I_{DSS}, the indicated $V_{GS(off)}$ error will be reduced to about 3 percent. For a true indication of $V_{GS(off)}$, and a realistic picture of the parameters of Figure 12, care must be taken that leakage currents do not result in an error in the $V_{GS(off)}$ reading. Typically, at room temperature, 1 percent of I_{DSS} is still well above leakage currents but is low enough to give a fairly accurate value of $V_{GS(off)}$.

A typical circuit for measuring $V_{GS(off)}$ is shown in Figure 13. At $V_{GS} = 0$, the value of I_{DSS} can be measured. Then, by increasing V_{GS} until I_D is 0.01 percent of I_{DSS}, the value of $V_{GS(off)}$ is obtained. From a production standpoint, it is more convenient to specify I_D at some fixed value (such as 1 nA), rather than as a certain percentage of I_{DSS}. Thus a pinchoff voltage specification may be given as indicated in Table I.



Circuit for Measuring $V_{GS(OFF)}$
Figure 13

Table I

Typical Pinch-Off Voltage Specification

Characteristic		Min	Max	Units
$V_{GS(off)}$	Gate-source pinch-off voltage of: $V_{DS} = -5$ V, $I_D = -1$ μA	1	4	Volts

Another method which provides an indirect indication of the maximum value of $V_{GS(off)}$ is shown in Table II. The characteristic specified is $I_{D(off)}$, whereas the parameter of interest is $V_{GS} = 8$ volts. The specification does say that the maximum $V_{GS(off)}$ is approximately 8 volts, but no provision is made for stating a *minimum* $V_{GS(off)}$, as was done in Table I. Therefore, another test must be made if $V_{GS(off)\,(min)}$ is to be specified.

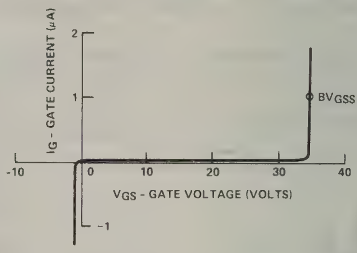
Table II

Indication of Maximum V_P

Characteristic		Test Conditions	Min	Max	Unit
$I_{D(off)}$	Pinch-off drain current	$V_{DS} = -12$ V, $V_{GS} = 8$ V		−10	μA

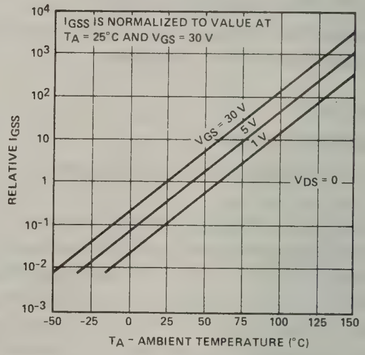
I_{GSS} – Gate-Source Cutoff Current

The input gate of a P-Channel FET appears as a simple PN junction; thus the input d-c input characteristic is analogous to a diode V-I curve, as is shown in Figure 14.



P-Channel FET Input Gate Characteristic
Figure 14

In the normal operating mode, with V_{GS} positive for a P-Channel device, the gate is reverse-biased to a voltage between zero and $V_{GS(off)}$. This results in a d-c gate-source resistance which is typically more than 100M Ω. The gate current is both voltage- and temperature-sensitive. Figure 15 shows this relationship for I_{GSS} versus temperature and V_{GS}.



I_{GSS} vs Temperature
Figure 15

If the gate-source junction becomes forward-biased, (negative voltage in a P-Channel device) or if V_{GS} exceeds the reverse-bias breakdown for the junction, the input resistance will then become very low.

The FET is normally operated with a slight reverse bias applied to the gate-source; hence a good measure of the d-c input characteristic is to check the gate current at a value of gate-channel voltage that is below the junction breakdown rating. In device evaluation, there are three common measurements of gate current: I_{GDO}, I_{GSO}, and the combined measurement I_{GSS}. These measurement circuits are shown in Figure 16.

The question is, should I_{GDO} and I_{GSO} be measured separately, or will one measurement of I_{GSS} suffice? One thing is certain: $I_{GSO} + I_{GDO} > I_{GSS}$, because the drain and the source are not completely isolated. They are, in fact, electrically connected via channel resistance. For most FETs, if V_G is greater than $V_{GS(off)}$, the difference between $(I_{GSO} + I_{GDO})$ and I_{GSS} is small; therefore, the measurement of I_{GSS} is a realistic means of controlling both I_{GDO} and I_{GSO}.

In a circuit, V_{GD} may be biased between zero and BV_{GDS}, while V_{GS} will be between zero and $V_{GS(off)}$: therefore, I_G is not necessarily the same as I_{GSS}.

BV_{GSS} – Gate-Source Breakdown Voltage

FET input terminals have been previously described as having NP or PN junctions, depending on the channel material. As such, the junction breakdown voltage is a necessary parameter.

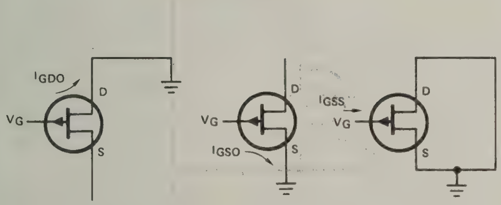
A useful equivalent circuit for a FET is the distributed constant network shown in Figure 17, for a P-Channel FET. If an N-Channel device is being evaluated, the diodes would be reversed. In most applications, the gate-drain voltage is greater than the gate-source voltage; thus the gate-drain breakdown rating is most important. However, it is also possible to consider the gate-source junction breakdown and the apparent drain-source breakdown (i.e., in Figure 17, when a high negative voltage is applied from drain to source, CR_1 will break down while CR_n becomes forward-biased).

Some device manufacturers use a BV_{GDO} rating, which means they are only checking diode CR_1. A better method is to use a BV_{GSS} rating (gate-source breakdown with the drain shorted to the source), because it checks both CR_1 and CR_n, in addition to exposing the *weakest* breakdown path along the entire gate-channel junction. The BV_{GSS} test also allows the user to interchange source and drain lead connections without worry about device breakdown ratings.

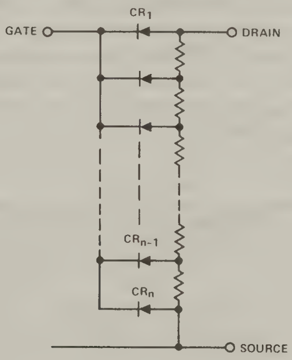
Admittedly, a BV_{GSS} test will reject some units which might pass a BV_{GDO} test; the number rejected, however, will be insignificant compared to the advantage of providing symmetrical operation.

Test Procedures for BV_{GSS}

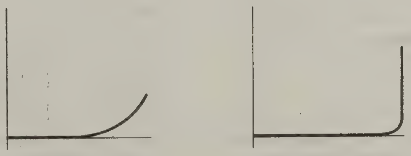
Junctions may break down softly or sharply; junctions with soft knee breakdown are undesirable. Without examining each individual unit on a curve tracer, devices with a soft knee may be eliminated by selecting a low current level for breakdown measurement (see Figure 18).



Three Common Measurement of Gate Current
Figure 16



A Useful FET Equivalent Circuit
Figure 17



SOFT KNEE (FAILING)

SHARP BREAKDOWN

Examples of Soft Knee and Sharp Knee Breakdown
Figure 18

g_{fs} – Transconductance

Transconductance, g_{fs}, is a measure of the effect of gate voltage upon drain current:

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}, \quad V_{DS} = \text{constant} \qquad (5)$$

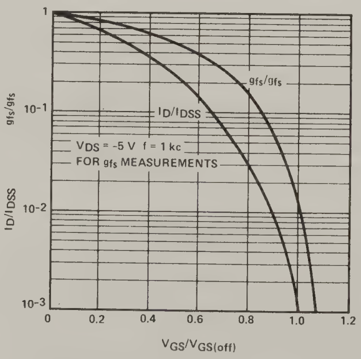
The interrelation of g_{fs} to the parameters I_{DSS} and $V_{GS(OFF)}$ should be noted. Equations 4, 6 and 7 describe the value of I_D and g_{fs} in a FET for any value of V_{GS} between zero and $V_{GS(OFF)}$.

$$g_{fs} = g_{fso}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) \qquad (6)$$

$$g_{fso} = -\frac{2I_{DSS}}{V_{GS(off)}} \qquad (7)$$

where g_{fso} is the value of g_{fs} at $V_{GS} = 0$ and I_{DSS} is the value of I_D at $V_{GS} = 0$. With these equations, the value of g_{fs} can be calculated with a fair degree of accuracy (20 percent) if I_{DSS} and $V_{GS(off)}$ are known.

Figure 19 shows normalized curves for I_D and g_{fs} as functions of V_{GS} in a P-Channel FET. These curves were obtained from actual measurements on typical diffused channel FETs, such as the 2N2606. The curves agree very well with Equations 4 and 6 until $V_{GS(off)}$ is approached. For these curves, $V_{GS(off)}$ was assumed to be the value of V_{GS} where $I_D/I_{DSS} = 0.001$.



Normalized Curves for I_D and g_{fs} as Functions of V_{GS}
Figure 19

The drain current of a JFET operating in the triode (below pinch-off) region can be accurately predicted by using Equation 8, where

$$I_D/\text{triode} = I_{DSS}\left(\frac{V_{DS}}{V_{GS(off)}}\right)^{1/2} \qquad (8)$$

Specifications for g_{fs} are shown in Tables III and IV. Note that there is a difference in the test conditions specified for the N-Channel 2N3823 and the P-Channel 2N3329. The gate voltage for the 2N3823 is established as zero. This means that g_{fs} is measured at $I_D = I_{DSS}$, as in Table III.

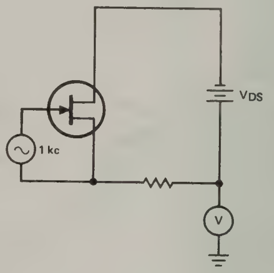
Table III (2N3823)

Characteristic		Test Conditions	Min	Max	Unit
g_{fs}	Small-signal common-source forward transconductance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1 kHz	3,500	6,500	μmho

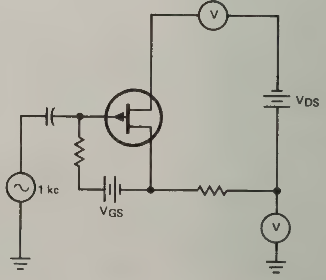
Table IV (2N3329)

Characteristic		Test Conditions	Min	Max	Unit
y_{fs}	Common-source forward transfer admittance	$V_{DS} = -10$ V, $I_D = -1$ mA f = 1 kHz		20	μmho

The test conditions shown in Table IV specify a certain value for I_D (−1 mA for the 2N3329). This means that for each unit tested, V_{GS} is adjusted until I_D equals the specified value. The conditions specified in Table III simplify testing of the g_{fs} parameter by eliminating the necessity of adjusting V_{GS}. Figures 20 and 21 show typical test setups for the two methods.



Test Circuit for g_{fs} with $V_{GS} = 0$
Figure 20



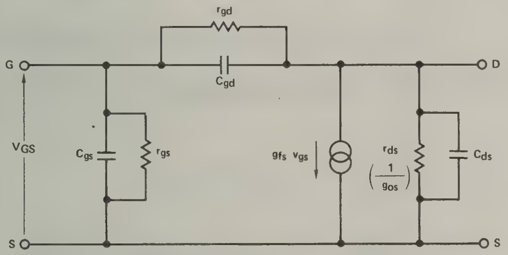
Test Circuit for g_{fs} with I_D Specified
Figure 21

Junction FET Capacitances

Associated with the junction between the gate and the channel of a FET is a capacitance whose value and geometric distribution are functions of the applied voltages V_{GS} and V_{DS}. Because of the complexity of dealing with such a distributed capacitance, a simplification is made so that two lumped capacitances, C_{gs} and C_{gd}, exist between the gate and the source and drain, respectively. (A much smaller capacitance, C_{ds}, also exists between the drain and the source, stemming mainly from the device package; this header capacitance is small enough so that it can be ignored for most purposes.)

Data sheets quote C_{gs} and C_{gd} (or other capacitances from which they may be derived) for specified operating conditions. Occasionally, graphs are included which show the variations of C_{gs} and C_{gd} as the result of changing conditions of V_{DS}, V_{GS} and temperature. If these data are not presented, an estimate of inter-electrode capacitance values may be made by assuming that these values vary inversely with the square root of the bias voltage. The temperature variations will be very small, because they depend on the -2.2 mV/°C change in junction potential difference.

Assuming that the FET is properly biased – that is, that the d-c conditions are met by the external circuitry – it is possible to construct an incremental equivalent circuit from which the small-signal or a-c performance may be predicted. Such an equivalent circuit is shown in Figure 22.



NOTE: $C_{gss} = C_{iss} = C_{gs} + C_{gd}$
$C_{oss} = C_{gd} + C_{ds} \cong C_{gd} = C_{rss}$

Incremental Equivalent Circuit for the Junction FET
Figure 22

The equivalent capacitance from the gate to the source, C_{gs}, is shunted by a very large input resistance, r_{gs}, with both of these parameters being characteristic of a reverse-biased junction. Similarly, the equivalent capacitance from the gate to the drain is shunted by the very large resistance r_{gd}. (For most purposes, r_{gs} and r_{gd} may be neglected, and the gate impedance of the FET treated as pure capacitance). At the drain side of the equivalent circuit the small capacitance C_{ds} – which stems from the header material – is shunted by the incremental channel resistance, r_{ds}. This resistance is capable of wide variations, depending on bias conditions. Since the equivalent circuit is fundamentally relevant to the pinch-off or saturated condition, r_{ds} will be on the order of megohms.

The incremental channel current is given by the transconductance, g_{fs}, multiplied by the incremental gate voltage. For the small signal, v_{gs}, this is manifested in the equivalent circuit by the current generator $g_{fs}v_{gs}$. Notice that the conventional direction of flow of this current is such that i_d flows into the FET, in a "positive" direction.

Many circuits can be designed around the equivalent circuit for the junction FET. The actual values of g_{fs} adn r_{ds} can be measured as previously mentioned; there remains only the requirement to establish the methods of determining C_{gs} and C_{gd}.

First, assume that the FET is in operation and that the drain is connected to the source via a large capacitor, i.e., the drain and source are short-circuited to a-c. Under these circumstances, a capacitance measurement between the gate and the source will give

$$C_{gss}\ (\text{or } C_{iss}) = C_{gs} + C_{gd} \tag{9}$$

Second, assume that the gate and source are short-circuited to a-c in a similar manner. A capacitance measurement between the drain and the source will now give

$$C_{dss}\ (\text{or } C_{oss}) \approx C_{gd} \tag{10}$$

The alternative symbols C_{iss} and C_{oss} simply refer to measurements made at the input (gate) and the output (drain) respectively. An alternative symbol for C_{gd} is C_{rss}, which refers to the "reverse" capacitance.

In data sheets, it is customary to state (= C_{iss}) C_{gss} and C_{dss} (= C_{oss}). C_{rss} is often given in place of C_{oss} because if $C_{ds} \ll C_{oss}$, which is usually the case, then $C_{rss} \cong C_{oss}$. Equations (9) and (10) can be used in those instances where it is necessary to extract C_{gs} and C_{gd}, as in

$$C_{gs} = C_{iss} - C_{gd} = C_{iss} - C_{rss} \tag{11}$$

and

$$C_{gd} = C_{rss} \tag{12}$$

Remember that all capacitance measurements should be made at the same bias levels, since the capacitances are functions of applied voltages. To indicate the order of the capacitances to be found in a junction FET, consider the values given in the data sheet for the Siliconix J202 N-channel FET. They are given as

C_{iss} (at V_{DS} = 20 V and f = 1 MHz) = 5 pF max.

and

C_{rss} (at V_{DS} = 20 V and F = 1 MHz) = 2 pF max.

Hence, at a drain-source voltage of 20 V and a frequency of 1 MHz, $C_{gs} = 5 - 2 = 3$ pF maximum. Even though the FET is physically symmetrical, bias conditions have forced the capacitances to be unequal.

Siliconix

APPLICATION NOTE

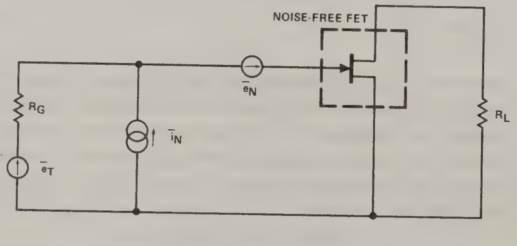
Audio-Frequency Noise Characteristics of Junction FETs

INTRODUCTION

The purpose of this application note is to identify and characterize audio frequency noise in junction field-effect transistors. Emphasis is placed on basic device characteristics rather than on end applications, since it is important for the circuit designer to know the salient noise behavior of the FET, and how those characteristics may be specified by production-oriented test parameters.

Defining FET Noise Figure

For analysis, it is convenient to represent noise in a FET by assuming that an ideal noise-free device has two external noise sources, $\overline{e}_N$ and $\overline{i}_N$. These noise sources are chosen to have the same output as would an actual noisy FET. An equivalent circuit is shown in Figure 1.



Representing Noise in an Ideal FET
Figure 1

A noise factor (F) is a Figure of Merit of a device with respect to the resistance of a generator. To calculate a noise factor, a source resistor R_G, with a thermal noise voltage $\overline{e}_T$, is added to the circuit.

A noise factor (F) may be defined as

$$F = \frac{\text{Total available output noise power}}{\text{Noise power at output due to thermal noise of } R_G}$$

or

$$F = \frac{\text{Noise power output due to } R_G + \text{noise power output due to FET}}{\text{Noise power output due to } R_G}$$

or

$$F = 1 + \frac{\text{Noise power output due to FET}}{\text{Noise power output due to } R_G}$$

or

$$F = 1 + \frac{\text{Gain X noise power of FET referred to input}}{\text{Gain X noise power due to } R_G}$$

or

$$F = 1 + \frac{\text{Noise power of FET referred to input}}{\text{Noise power due to } R_G}$$

The thermal noise voltage across R_G is$^{(1)}$

$$\overline{e}_T = \sqrt{4kTR_GB} \qquad (1)$$

where k = 1.380 x 10^{-23} Joules/°K (Boltzmann's Constant), T = temperature in °K, and B = bandwidth in Hz. Therefore noise power due to R_G is

$$\frac{\overline{e}_T^{\,2}}{R_G} = \frac{4kTR_GB}{R_G} = 4kTB \qquad (2)$$

The noise power of the FET referred to the input is

$$\frac{\overline{e}_N^{\,2}}{R_G} + i_N^{\,2} \cdot R_G \tag{3}$$

When expressions for the noise power of both the FET and R_G are substituted, the noise factor becomes

$$F = 1 + \frac{\overline{e}_N^{\,2} + \overline{i}_N^{\,2} R_G^{\,2}}{4kTR_GB} \tag{4}$$

A noise figure (NF) expressed in dB indicates the presence of added noise power from the FET or another active device. The noise figure is always given with reference to a standard, specifically the generator resistance R_G:

$$NF = 10 \log_{10} [F] \tag{5}$$

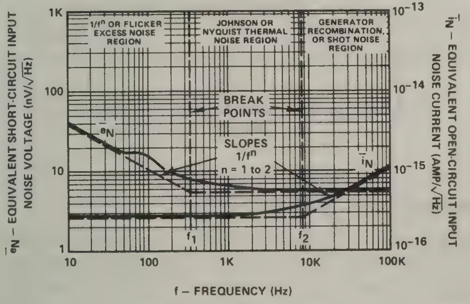
The noise figure of the FET is

$$NF = 10 \log_{10} \left[1 + \frac{\overline{e}_N^{\,2} + \overline{i}_N^{\,2} R_G^{\,2}}{4kTR_GB} \right] \text{dB} \tag{6}$$

When junction FET noise is expressed in terms of the noise figure (NF), an inherent disadvantage arises in that the noise figure value is dependent upon the value of the generator resistance, R_G. Therefore, the $\overline{e}_N$, $\overline{i}_N$ method remains as the best way to quantitatively express the noise characteristics of the FET itself.

Describing Junction FET Noise Characteristics

Junction FET $\overline{e}_N$ and $\overline{i}_N$ characteristics are frequency-dependent within the audio noise spectrum, and take a form as shown in Figure 2.



Characteristics of Junction FET Noise
Figure 2

$\overline{e}_N$, the equivalent short circuit input noise voltage (with the exception of the 1/f^n region), is defined as$^{(2)}$

$$\overline{e}_N = \sqrt{4kTR_NB} \tag{7}$$

where $R_N \cong 0.67/g_{fs}$, the equivalent resistance for noise. The $\overline{e}_N$, except in the 1/f^n region, closely approximates the equivalent thermal noise voltage of the channel resistance.

In the so-called 1/f^n region, $\overline{e}_N$ is expressed as

$$\overline{e}_N = \sqrt{4KR_NB(1 + f_1/f^n)} \tag{8}$$

where n varies between 1 and 2 and is device- and lot-oriented.

The characteristic bulge in $\overline{e}_N$ in the 1/f^n region has been observed to some extent in all junction FETs submitted to test. The breakpoint or corner frequency shown as f_1 in Figure 2 is lot- and device design-oriented, and varies from about 100 Hz to 1 kHz.

As indicated in Equations (7) and (8), $\overline{e}_N$ is inversely proportional to the square root of the transconductance of the FET ($\overline{e}_N \propto 1/\sqrt{g_{fs}}$). $\overline{e}_N$ can be lowered by a factor of $1/\sqrt{N}$ if N devices with matched electrical characteristics are connected parallel. For example, when

$$N = 2 \tag{9}$$

let

$$\overline{e}_{N1} = \overline{e}_{N2} \tag{10}$$

and let

$$g_{fs1} = g_{fs2} \tag{11}$$

Thus,

$$g_{fs}\text{TOTAL} = 2\ g_{fs1} \text{ or } 2\ g_{fs2} \tag{12}$$

From Equation (7)

$$\overline{e}_{N1} = \sqrt{4kT(0.67/g_{fs1})B} \tag{13}$$

and

$$\overline{e}_N\text{TOTAL} = \sqrt{4kT(0.67/2g_{fs1})B} \tag{14}$$

Thus,

$$\overline{e}_N\text{TOTAL} = \frac{1}{\sqrt{2}}\, \overline{e}_{N1} \tag{15}$$

A second way to achieve low $\overline{e}_N$ is to use a device with a large gate area. Empirically, $\overline{e}_N$ is inversely proportional to the square of the gate area ($\overline{e}_N \propto 1/A_G^{\,2}$), independent of g_{fs}. This large gate area philosophy has been followed in the design of the Siliconix 2N4867A FET, and noise performance of the device is discussed later in this Application Note. A major advantage of this type of design is that $\overline{e_N}$ is significantly lowered and $\overline{i_N}$ also remains at a low value.

The equivalent open-circuit input noise current, $\overline{i_N}$, with the exception of the shot noise region shown in Figure 2, is due to thermally-generated reverse current in the gate channel junction. It is defined as

$$\overline{i_N} = \sqrt{2qI_GB} \tag{16}$$

where $q = 1.602 \times 10^{-19}$ coulomb (the magnitude of the electron charge), I_G is the measured DC operating gate current in amperes, and B is bandwidth in Hz. The expression is accurate only when the measured gate current is the result of bulk device conductance. It is possible for the measured gate current to be due to conductance stemming from contamination across the leads of the semiconductor package.

At higher frequencies, as in the shot noise region shown in Figure 2, $\overline{i_N}$ can be approximated as being equal to the Nyquist thermal noise current generated by a resistor:(3)

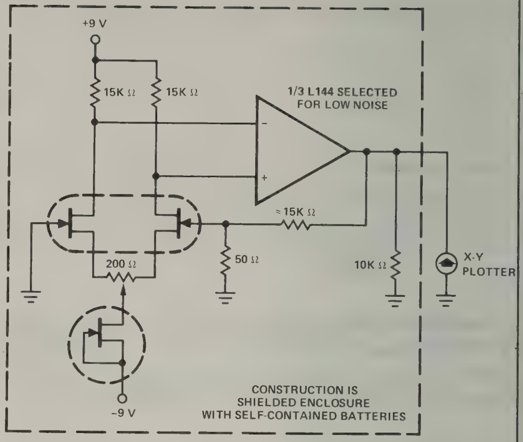
$$\overline{i_N} = \sqrt{\frac{4kTB}{R_p}} \tag{17}$$

where R_p is the real part of the gate-to-source input impedance. The breakpoint or corner frequency f_2 in Figure 2 is lot- and device design-oriented and can vary from 5 kHz to 50 kHz.

Another form of noise found in junction FETs is known as "popcorn" or burst noise; the term popcorn noise was originated in the hearing aid industry because of noise or level shifts which are present in input stages, and which resemble the sound of corn popping.

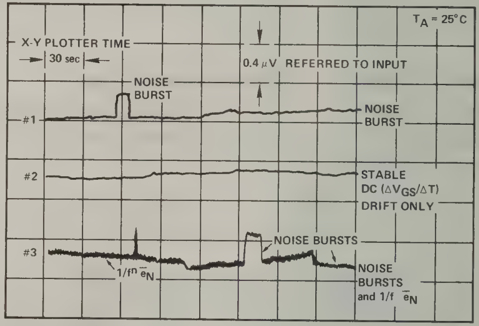
Popcorn noise is a form of random burst input noise current which remains at the same amplitude, and which is confined to frequencies of 10 Hz or lower. The suitability of a FET device is dependent on the amplitude of the burst, its duration, and its repetition rate. The origins of popcorn noise are not completely identified, but are believed to be caused by intermittent contact in aluminum-silicon interfaces and by contamination in the oxidation processes.

A test circuit to measure popcorn noise in differential junction FET amplifiers is shown in Figure 3. In practice, popcorn noise is evaluated on an engineering basis, and not on a production-line basis. No correlation between $1/f^n$ noise at 10 Hz and popcorn noise has yet been found in junction FETs. However, if the amplitude of the burst is large and occurs frequently, then $1/f^n$ noise voltage ($\overline{e_N}$) is masked and difficult to evaluate at 10 Hz.


+9 V
15K Ω
15K Ω
1/3 L144 SELECTED FOR LOW NOISE
-
+
≈ 15K Ω
200 Ω
50 Ω
10K Ω
X-Y PLOTTER
-9 V
CONSTRUCTION IS SHIELDED ENCLOSURE WITH SELF-CONTAINED BATTERIES

Test Circuit to Measure Popcorn Noise
Figure 3

The graph in Figure 4 shows "moderate" burst noise observed in a group of junction FET differential amplifiers which were measured in the test circuit.



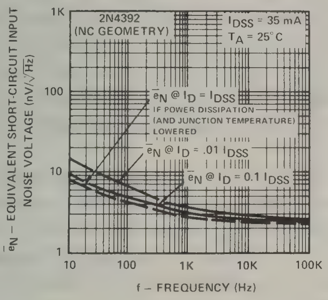
Popcorn Noise in Differential Amplifiers
Figure 4

Operating Point Considerations

Unlike bipolar transistors, where $\overline{e_N}$ and $\overline{i_N}$ characteristics vary directly with change in collector current (I_C), similar characteristics in junction FETs will vary only slightly as drain current (I_D) is varied. This is true so long as the FET is biased so that the drain-source voltage is greater than the pinch-off voltage ($V_{DS} > V_p$ or $V_{GS(off)}$).

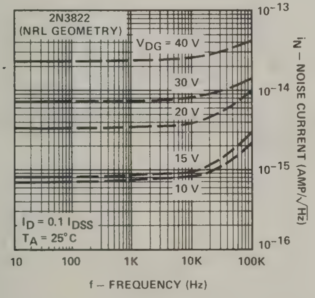
The $\overline{e_N}$ in junction FETs will be lowest when the devices are operated at $V_{GS} = 0$ ($I_D = I_{DSS}$), where transconductance (g_{fs}) is at its highest value. This will be true only if device dissipation is maintained very low in relation to the total dissipation capability of the FET.

The curves in Figure 5 illustrate changes in $\overline{e}_N$ as the operating drain current (I_D) is varied. Note that the lowest $\overline{e}_N$ did not occur at $V_{GS} = 0$, because of high power dissipation and a resultant rise in junction temperature at the operating point.



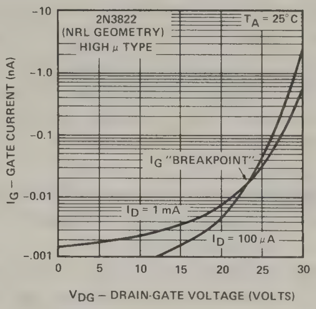
$\overline{e}_N$ Changes vs I_D Variations
Figure 5

The optimum (lowest) $\overline{i}_N$ in depletion-mode junction FETs should occur at $V_{GS} = 0$ ($I_D = I_{DSS}$). In practice, very little change will be seen in $\overline{i}_N$ when the operating point is changed, provided that the drain-gate voltage is maintained below the gate current (I_G) breakpoint and power dissipation is kept at a low level. The curves in Figure 6 illustrate $\overline{i}_N$ characteristics as a function of drain-gate voltage at points below, on, and above the I_G breakpoint voltage.

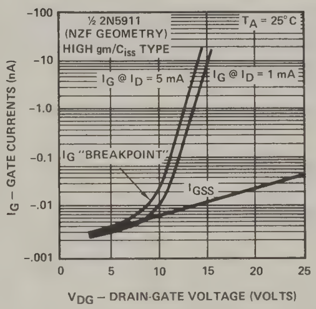


$\overline{i}_N$ Characteristics as Function of Drain-Gate Voltage
Figure 6

In circuit design, particular attention must be paid to drain-gate voltage (V_{DG}) to minimize gate current (I_G) under operating conditions. The critical drain-gate voltage (I_G breakpoint voltage) can be anywhere from 8 to 40 V, depending on device design.$^{(4)}$ Gate operating current (I_G) should not be considered equal to gate reverse current (I_{GSS}) in linear amplifier applications. I_{GSS} is only an indication of reverse-biased junction leakage under non-operating conditions. The Curves in Figures 7 and 8 show how I_G breakpoint is related to basic device design. Device designs with a high g_{fs}/C_{iss} ratio have low breakpoint voltages, typically at $V_{DG} = 10$ V, whereas high μ devices ($\mu = r_{ds} \cdot g_{fs}$). have much higher I_G breakpoints, typically $V_{DG} = 20 - 30$ V.



Gate Operating Current vs Drain-Gate Voltage
Figure 7

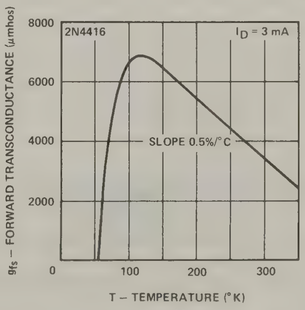


Gate Currents vs Drain-Gate Voltage
Figure 8

Characteristics of $\overline{e}_N$ and $\overline{i}_N$ at Low Temperature

Three equations presented earlier ((7), (16) and (17)) show that $\overline{e}_N$ and $\overline{i}_N$ are temperature dependent. $\overline{e}_N$ and $\overline{i}_N$ are proportional to $\sqrt{T}$, and both will be reduced if the temperature is lowered. In Equation (16), $\overline{i}_N$ is proportional to $\sqrt{I_G}$; I_G will halve for each temperature drop of 10 to 11°C. $\overline{e}_N$ is also proportional to $\sqrt{R_N}$, where $R_N \cong 0.67/g_{fs}$. Thus when g_{fs} is increased, which is typical of junction FETs operating at low temperature, $\overline{e}_N$ will also lower.

In Figure 9, g_{fs} has been plotted vs temperature for a silicon junction FET, and the low temperature limitation caused by a dropoff in g_{fs} is clearly shown.



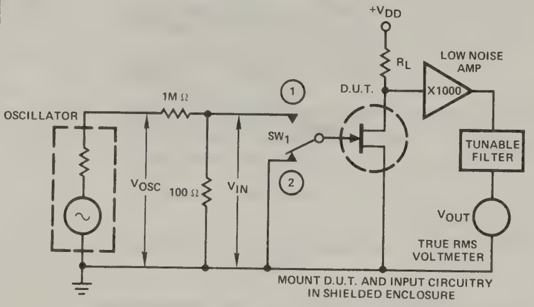
g_{fs} vs Temperature
Figure 9

In connection with the plot of g_{fs} vs temperature, note that the relationship can vary from approximately 0.2% to 1% per degree C. The g_{fs} slope depends upon the basic design of the FET, and upon the proximity of the drain current operating point to I_{DZ}, the zero temperature coefficient point.

The major application for junction FETs at low temperature is in charge-sensitive amplifiers.$^{(5)}$ For best performance in this type of application, a high g_{fs}/C_{iss} ratio is required. Recommended Siliconix FET types for such applications are the 2N4416 (NH geometry) and the U311 (NZA geometry).

Test Measurements

By definition, $\overline{e}_N$ and $\overline{i}_N$ are referred to the input of the device under test. To measure $\overline{e}_N$, the test circuit shown in Figure 10 will prove useful.



Test Circuit to Measure $\overline{e}_N$
Figure 10

The following procedure should be used to make the $\overline{e}_N$ test:

1. Set tunable filter to required f_{low} and f_{high}. Adjust oscillator to mean center frequency ($f_{mean} = [f_{low} \cdot f_{high}]^{1/2}$).
2. Set V_{osc} to 100 mV with Switch 1 in position ①. Compute $V_{in1} = 10^{-1} \times \frac{10^2}{10^6} = 10^{-5}\text{ V} = 10\,\mu\text{V}$.
3. Measure V_{out1}. Compute overall gain as $A_v = \frac{V_{out1}}{V_{in1}} = \frac{V_{out1}}{10\,\mu V}$.
4. Set Switch 1 to position ② and measure V_{out2}. Compute V_{in2}, the equivalent short-circuit input noise voltage ($\overline{e}_N$), using A_v from Step 3. $V_{in2} = \frac{V_{out2}}{A_v} = \overline{e}_N$ in volts over bandwidth f_{low} to f_{high}.

An alternate method of performing the above test is to use a Quan-Tech Transistor Noise Analyzer consisting of a Model 2173 Control Unit and a Model 2181 Filter. The analyzer has provision for measuring $\overline{e}_N$ and determining NF with various values of R_G in FET and bipolar devices with selectable test conditions. The measuring system has a constant gain of 10,000. The analyzer records output noise at selected frequencies between 10 Hz and 100 kHz in the device under test, with the scale shown as the actual output divided by 10,000. This is then the output noise referred to the input. The equivalent bandwidth for testing is 1 Hz.

There are certain instances where the test circuit or the Transistor Noise Analyzer are not adequate to measure $\overline{e}_N$ at certain frequencies over certain bandwidths in the $1/f^n$ region. The rms noise over a bandwidth from f_{low} to f_{high}, where there is a $1/f^n$ characteristic over the entire range, can be computed as

$$\overline{e}_N = \left[\overline{e}_N \text{ known}\right] \cdot \left[f_{known} \cdot \ln\left(\frac{f_{high}}{f_{low}}\right)\right]^{1/2n} \qquad (18)$$

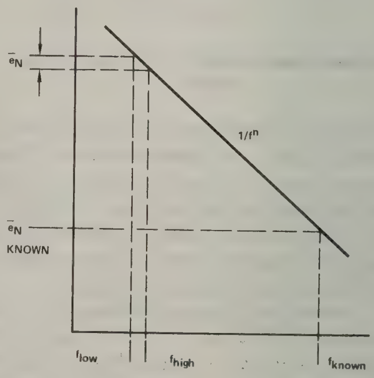
Figure 11 represents this equation graphically. For example, $\overline{e}_N$ known = $70 \times 10^{-9}\text{ V}/\sqrt{\text{Hz}}$ at 10 Hz. How much noise is in the band from 4.5 to 5.5 Hz? The noise has a $1/f^1$ characteristic over the entire range. Thus

$$\overline{e}_N = \left[70 \times 10^{-9}\right] \cdot \left[10 \cdot \ln\left(\frac{5.5}{4.5}\right)\right]^{1/2} \text{ Volts} \qquad (19)$$

or

$$\overline{e}_N = 99.16 \times 10^{-9}\text{ V}/\sqrt{\text{Hz}} \text{ @ } 4.975\text{ Hz}, \qquad (20)$$

4.975 Hz is the mean center frequency where $f_{mean} = (f_{low} \cdot f_{high})^{1/2}$.



Computing rms Noise Over a Bandwidth
Figure 11

$\overline{i}_N$ measurements are difficult to implement at best. At frequencies below f_2 in Figure 2, $\overline{i}_N$ is assumed to have a constant level or "white" noise characteristic which may be correlated to gate current, I_G. From Equation (16) I_G is established as the measured bulk gate current. Because measured gate current (I_G) is the result of all conductances at the gate, the resultant gate current and the computed $\overline{i}_N$ due to bulk material can be assumed to be this value or less.

The total equivalent input noise of the FET can be approximated by$^{(6)}$

$$\overline{e}_{ni}{}^2 = \overline{e}_T{}^2 + \overline{e}_N{}^2 + \overline{i}_N{}^2 \cdot R_G{}^2 \tag{21}$$

where $\overline{e}_T{}^2$ is the thermal noise of the generator resistance R_G and $\overline{e}_{ni}{}^2$ is the total noise referred to the input. This approximation assumes that the equivalent noise voltage and the current generators vary independently. Equation (21) implies that $\overline{i}_N{}^2$ can be calculated if $\overline{e}_N{}^2$, $\overline{e}_T{}^2$ and total noise $\overline{e}_{ni}{}^2$ are known. The difficulty here is that in MOS or junction FETs, the R_G must be very large to detect the anticipated small value of $\overline{i}_N$. However, when R_G is very large $\overline{e}_T{}^2$ is much greater than $\overline{i}_N{}^2 \cdot R_G{}^2$. For example, over a 1 Hz bandwidth at 25°C, if R_G is equal to 100 MΩ, then

$$\overline{e}_T{}^2 = 4kTR_G = 4 \times 1.38 \times 10^{-23} \times 2.95 \times 10^2 \times 10^8 = 1.63 \times 10^{-12}\ \mathrm{V}/\sqrt{\mathrm{Hz}}. \tag{22}$$

Anticipated $\overline{i}_N$ is

$$\overline{i}_N \approx 10^{-15}\ \mathrm{Amperes}/\sqrt{\mathrm{Hz}} \tag{23}$$

and

$$\overline{i}_N{}^2 = 10^{-30}\ \mathrm{Amperes}/\sqrt{\mathrm{Hz}}. \tag{24}$$

Thus

$$\overline{i}_N{}^2 \cdot R_G{}^2 = 10^{-30} \cdot 10^{16} = 10^{-14}\ \mathrm{V}/\sqrt{\mathrm{Hz}}. \tag{25}$$

Therefore, $\overline{i}_N{}^2 \cdot R_G{}^2$ is much less than $\overline{e}_T{}^2$, which renders this method of finding $\overline{i}_N$ impractical for most common MOS FETs or junction FETs.

An improved method of measuring $\overline{i}_N{}^2$ is to substitute a low-loss mica capacitor for resistor R_G. The mica capacitor by definition does not have equivalent thermal noise voltage, and thus Equation (21) becomes

$$\overline{e}_{ni}{}^2 = \overline{e}_N{}^2 + \overline{i}_N{}^2 \cdot X_C{}^2 \tag{26}$$

(where X_C = capacitive reactance)

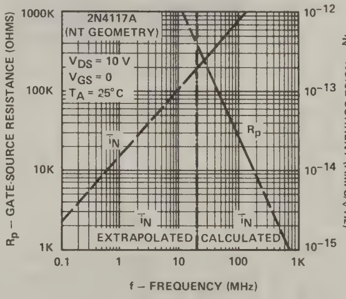
or

$$\overline{i}_N = \frac{(\overline{e}_{ni}{}^2 - \overline{e}_N{}^2)^{1/2}}{X_C} \tag{27}$$

When a 10 pF mica capacitor was used in the evaluation circuit (up to a frequency of 100 Hz) a correlation of from 80 to 90% was obtained when compared to $\overline{i}_N{}^2$ computed from measured gate current readings.

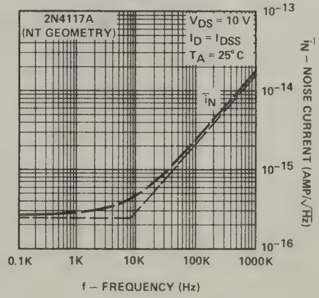
At frequencies above 100 Hz direct computation of $\overline{i}_N$ via the capacitor method becomes unwieldy because of the rapid decrease in capacitor reactance at these frequencies.

In calculating $\overline{i}_N$ at higher frequencies, an alternate method is to measure (R_p) the real part of the gate-source impedance of the FET.$^{(7)}$ When R_p is measured at various frequencies, the equivalent short-circuit input noise current ($\overline{i}_N$) can be computed as a function of frequency (See Equation (17)). A convenient instrument to measure R_p is the Hewlett-Packard Type 250A Rx meter or equivalent. The Type 250A Rx meter can measure R_p accurately up to 200K ohms. As is shown in Figure 12, this establishes the low frequency limit of 20 MHz for $\overline{i}_N$ computed via direct measurement of R_p for the Siliconix FET Type 2N4117A. For frequencies between 100 Hz and 20 MHz, $\overline{i}_N$ must be extrapolated, as is shown in Figures 12 and 13. For FET types with lower R_p (such as the Siliconix 2N4393) $\overline{i}_N$ can be computed down to 2 MHz, and hence extrapolated $\overline{i}_N$ between 100 Hz and 100 kHz is more accurate.



Low Frequency Limit for Calculated $\overline{i}_N$

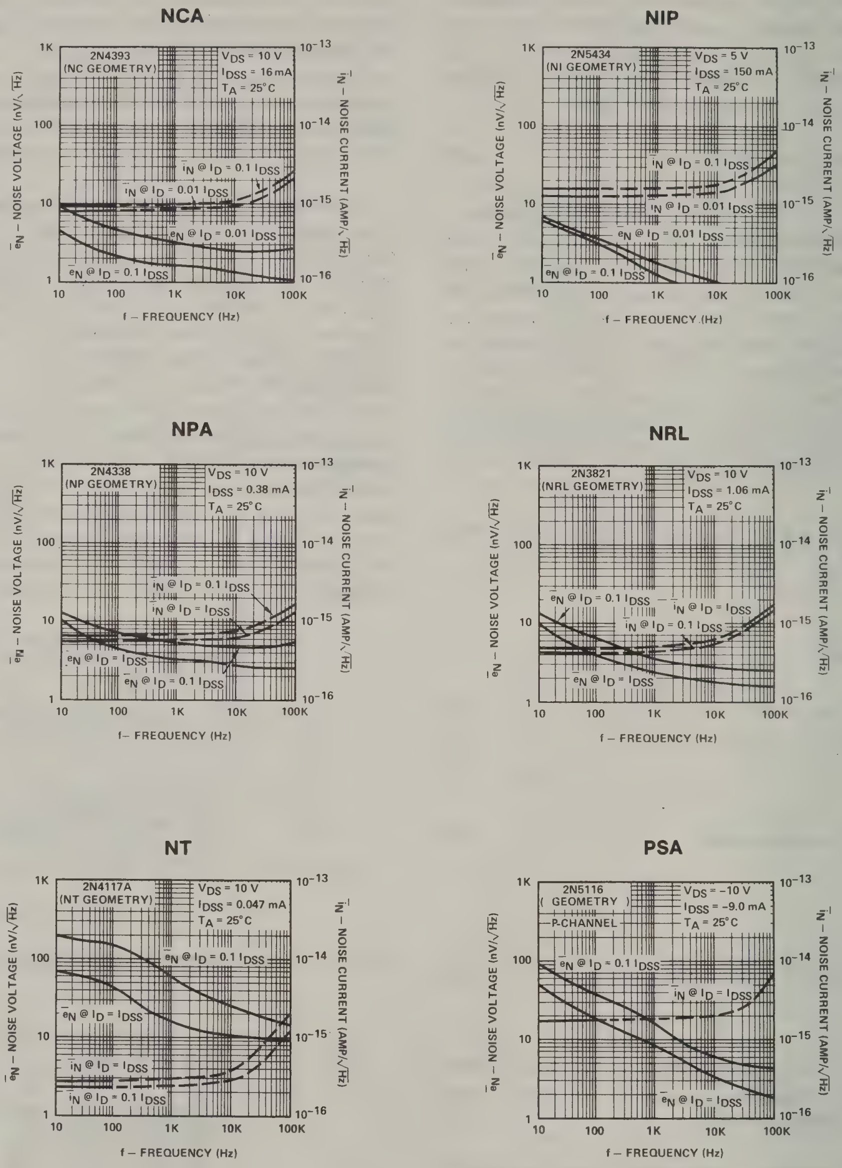
Figure 12



Extrapolated $\overline{i}_N$ vs Frequency

Figure 13

The following are representative $\overline{e}_N$, $\overline{i}_N$ curves for Siliconix J-FET products. Of particular importance is the geometry which by its design governs the basic noise characteristics of product types derived from it.



FET Noise Characteristics by Geometry
Figure 14

CONCLUSION

Contemporary junction FETs have noise voltages ($\overline{e}_N$) equal to those found in low-noise bipolar transistors. Each type of device has a different operating mechanism: the FET is voltage-actuated, while the bipolar transistor is current-actuated. Hence, FETs have an inherently lower noise current ($\overline{i}_N$) and are preferred over bipolar devices in most audio-frequency applications where low-noise performance is a design requirement.

When bias points are properly selected, as described in this Application Note, the excellent low-noise characteristics of high g_{fs} junction FETs can be realized.

The curves shown in Figure 14 are representative of $\overline{e}_N$ and $\overline{i}_N$ performance of Siliconix junction FETs. Of particular importance in these curves is the process geometry by which the basic design of the FET governs the noise characteristics of product types derived from it. Readers are invited to refer to the Siliconix FET catalog for full geometry performance data, and for specific part numbers stemming from the generic process geometries.

In the measurement section of this Application Note, it was shown that direct $\overline{e}_N$ measurements can readily be made. $\overline{i}_N$ can be guaranteed at frequencies below 100 Hz by measuring the DC operating gate current (I_G). When I_G is known, $\overline{i}_N$ can be extrapolated from frequencies below 100 Hz to predict noise performance at frequencies to 100 kHz.

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APPLICATION NOTE

FETs for Video Amplifiers

INTRODUCTION

The field-effect transistor lends itself well to video amplifier applications. Gain bandwidth products in excess of 250 MHz may be easily achieved using simple one or two transistor circuits. DC input resistances in the tens of megohms range may also be easily achieved while input capacitances may be significantly reduced to less than 1 pF by well known circuit techniques. Video amplifiers have applications in communications and pulse amplifying circuits and normally operate up to 100 MHz.

Behavior of FET Input Resistance

A prime FET parameter, input impedance, has a large effect in determining the frequency response of a FET video amplifier. It is not a simple RC network but one in which the real and imaginary parts are a function of frequency.

The voltage generator source resistance R_g and the FET input impedance Z_{in} form a frequency sensitive attenuation network. The larger the R_g, the worse will be the frequency response, and vice versa. Examining this in greater detail, consider the input equivalent circuit of a FET connected in the common source configuration,

where

R_{gs} and R_{gd} = bulk series gate resistance
C_{gs} and C_{gd} = bulk series gate capacitance
G_{oss} = output conductance

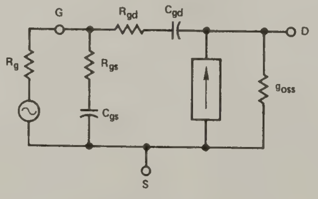


Figure 1

For this analysis the gate source leakage resistance has been ignored due to its high value. Redrawing the input equivalent circuit as a simple parallel RC combination results in

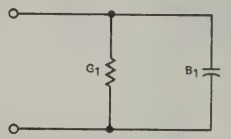


Figure 2

where

$$G_1 = \mathrm{Re}\,|Y_{in}| = \frac{\omega^2[T_1C_1(1+\omega^2T_2{}^2) + T_2C_2(1+\omega^2T_1{}^2)]}{1-(\omega^2T_1T_2)^2+\omega^2(T_1{}^2+T_2{}^2)} \quad (1)$$

and

$$B_1 = \mathrm{Im}\,|Y_{in}| = \frac{\omega[C_1(1+\omega^2T_2{}^2) + C_2(1+\omega^2T_1{}^2)]}{1-(\omega^2T_1T_2)^2+\omega^2(T_1{}^2+T_2{}^2)} \quad (2)$$

where

$$T_1 = C_{gd}R_{gd}$$
$$T_2 = C_{gs}R_{gs} \quad (3)$$

The input resistance varies inversely with the square of the frequency (see Figures 3 and 4) while the input reactance is inversely proportional to the frequency (see Figure 3).

In common-source circuits, $1/G_1$ will typically fall to $< 2\text{K}$ ohms at 100 MHz while C_1 remains substantially constant at least up to 1000 MHz. Figures 3 and 4 below exhibit these relationships.

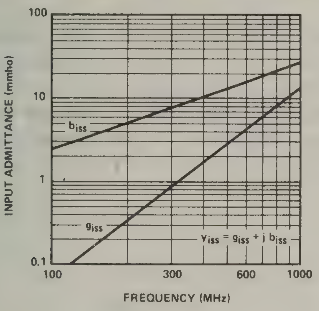
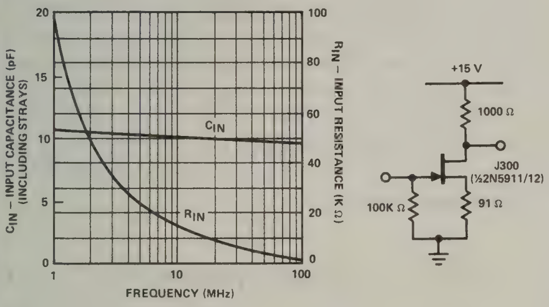


Figure 3



(A) (B)

Figure 4

To maintain low input capacitance, and thus a high input impedance over a wide frequency range, feedback may be applied to most circuits. Such techniques are explored in "FET and Bipolar Cascade" section (page 5). The effect of R_g on the frequency response is shown in Figures 6, 9, 11, 13 where various amplifier configurations are investigated.

Circuits to Consider

Five video amplifier circuits are considered. They are:

- Common-Source Configuration
- Shunt-Peaked Common-Source Configuration
- Source Follower
- Cascode Amplifier
- FET and Bipolar Cascade

Common-Source Circuit[1]

The circuit of Figure 5 features high input impedance and high voltage gain. The drain resistor is set at 560 ohms to maintain good bandwidth which, with 50-ohm generator impedance, is determined primarily by the drain load components. These are:

$$R_D = 560\ \Omega \tag{4}$$

$$C_T = C_{gd} + C_D + C_S \tag{5}$$

C_{gd} = 2.0 pF, C_D the VTVM probe, 2.0 pF, and C_S is circuit stray capacitance of 3 pF.

$$C_T = 2 + 2 + 3 = 7\text{ pF} \tag{6}$$

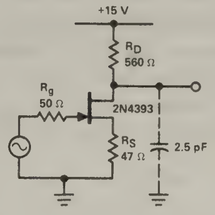


Figure 5

The 3-dB frequency ω_3 is given by:

$$\omega_3 = \frac{1}{C_T R_D} \tag{7}$$

$$= \frac{1}{7 \times 10^{-12} \times 560} \tag{8}$$

$$\omega_3 = 255 \times 10^6 \tag{9}$$

$$f_3 = 39\text{ MHz} \tag{10}$$

The low frequency voltage gain for this configuration is given by:

$$A_V = \frac{g_{fs} R_D}{1 + g_{fs} R_S} \tag{11}$$

$$A_V = 4.9 \tag{12}$$

where

g_{fs} = 15 mmho when I_D = 12 mA, the quiescent current

$$R_D = 560\ \Omega \tag{13}$$

$$R_S = 47\ \Omega \tag{14}$$

Measured Performance

Figure 6 shows the frequency response of the circuit. The low-frequency gain was measured at 4.5 and the 3-dB bandwidth at 44 MHz giving a gain bandwidth product of 197 MHz. This compares with a calculated gain bandwidth of 191 MHz.

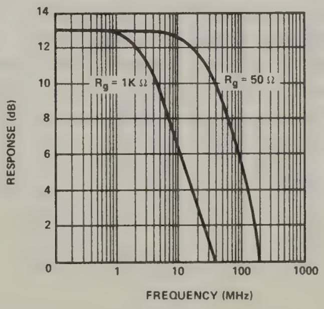


Figure 6

Effect of Increasing Generator Impedance

If the generator resistance R_g is increased to 1K ohm, the input time constant of the FET is increased. The bandwidth of the amplifier is now determined primarily by the input time constant which consists of generator impedance (R_g = 1K ohm) shunted by C_{in} (see Figure 7).

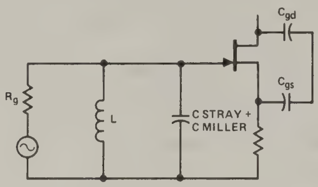


Figure 7

where

$$C_{in} = \left(1 + \frac{g_{fs}R_D}{1 + g_{fs}R_S}\right) C_{gd} + \left(1 - \frac{g_{fs}R_S}{1 + g_{fs}R_S}\right) C_{gs} + \text{Strays}$$

$$= (5.9 \times 3.5) + (0.6 \times 10) + 3. \qquad (15)$$

$$C_{in} = 30 \text{ pF} \qquad (16)$$

where

$$C_{gd} = 3.5 \text{ pF} \qquad (17)$$

$$C_{gs} = 10 \text{ pF} \qquad (18)$$

The corresponding 3-dB frequency is given by:

$$\omega_3 = \frac{1}{C_{in}R_g} \qquad (19)$$

$$= \frac{1}{30 \times 10^{-12} \times 10^3} = \frac{10^9}{30} \qquad (20)$$

$$f_3 = 5.3 \text{ MHz} \qquad (21)$$

which agrees closely with the measured bandwidth as shown in Figure 6.

Shunt-Peaked Common-Source Circuit

The frequency response of the resistance-loaded common-source circuit may be significantly extended by shunt peaking at the gate and/or drain. Consider first the gate circuit. Here an inductor may be connected in shunt with the gate and set to such a value that it forms a tuned circuit with the FET input capacitance. The frequency of resonance is determined by:

$$f_o = \frac{1}{2\pi\sqrt{LC_{in}}} \qquad (22)$$

where

$$C_{in} = C_{iss} + C_{Stray} + C_{Miller} \qquad (23)$$

The response of an input signal of frequency f_o will then be boosted to an extent depending on the loaded Q of the tuned circuit; the loaded Q in turn is dependent on the unloaded Q of inductor L, R_g and the FET input resistance.

Next consider shunt peaking in the drain circuit. In Figure 8 the inductor L is set to such a value that a low Q tuned circuit is formed; the resonating capacitance C is the parallel combination of C_{gd} plus stray and load capacitances. For a flat response, the LC circuit is tuned to the 3-dB frequency of the resistance loaded circuit of Figure 5. (See Appendix.)

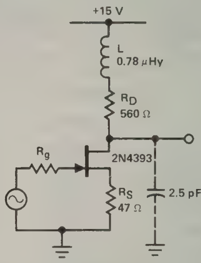


Figure 8

The required value of L is:

$$L = \frac{R_D{}^2C}{2}, \text{ and for the circuit in Figure 8.} \qquad (24)$$

$$= 0.78\ \mu\text{H} \qquad (25)$$

where

$$R_D = 560\ \Omega \qquad (26)$$

$$C = C_{gd} + C_{Stray} + C_{VTVM\ PROBE} \qquad (27)$$

$$C = 1.2 + 1.3 + 2.5 = 5 \text{ pF} \qquad (28)$$

Due to the low circuit Q (about 5), the value of L is not critical.

The 3-dB bandwidth shown in Figure 9 now extends to 67 MHz giving a gain bandwidth product of:

$$67 \times 4.2 = 281 \text{ MHz} \qquad (29)$$

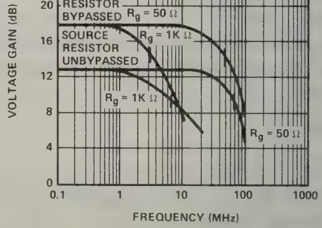


Figure 9

When R_S is bypassed by a 0.1 capacitor, the low frequency voltage gain is given simply by:

$$A_V = g_{fs}R_D \qquad (30)$$

$$= 15 \times 10^{-3} \times 560 \qquad (31)$$

$$= 8.4\ (18.5\ \text{dB}) \qquad (32)$$

The gain bandwidth product tends to remain constant whether R_S is bypassed or not and this effect is shown in Figure 9.

Source-Follower Circuit[2]

A J300 is used in the FET source-follower circuit, Figure 10, because of its low input capacitance and high g_{fs} which remains high at the frequency range of interest. A source follower exhibits a high input impedance and low output impedance. The real part of the output impedance is the reciprocal of g_{fs} which is independent of frequency up to about 600 MHz. The input capacitance is $C_{gd} + C_{gs}(1 - A_V)$ which, in this case, is approximately 1.5 pF maximum. The input capacitance is also independent of frequency and independent of load when the load is larger than the output resistance R_o.

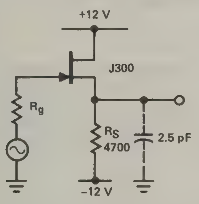


Figure 10

The frequency response is dependent mainly on the generator internal impedance. For example, when R_g is increased to 1K ohm the bandwidth falls to 80 MHz. In this particular circuit, the low-frequency voltage gain is 0.94.

The input resistance is proportional to $1/f^2$ as explained in the section, "Behavior of Input Resistance," and at some high frequency will go negative, particularly if the source resistor is large. For example, with the circuit in Figure 10, the input resistance is high at 10 MHz but in the negative resistance region at 100 MHz. However, when R_S is 1000 ohms, the input resistance is real at this frequency.

The voltage gain of a source follower is given by:

$$A_V = \frac{g_{fs}R_S}{1 + g_{fs}R_S} \qquad (33)$$

Thus A_V is almost independent of R_S when R_S is large. Using typical values for the J300 (or ½ 2N5912) in Figure 10, the drain current is 3 mA, g_{fs} is 5 mmho and R_S 4700 ohms,

$$A_V = 0.96$$

which is near the measured value of 0.94. Measured performance is shown in Figure 11. The output resistance of this source follower is given by:

$$R_o = \frac{1}{g_{fs}} = \frac{1}{5 \times 10^{-3}} = 200\ \Omega \qquad (34)$$

and in this circuit, R_o was measured at 165 ohms. The source follower is a useful versatile circuit which may be used as an impedance converter, level shifter, buffer stage, or as an input circuit to an op amp or feedback amplifier.

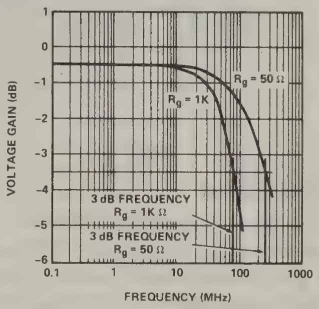


Figure 11

Cascode Circuit

The cascode circuit has applications as a buffer amplifier for use with high stability oscillators or in low level power amplifiers[2] mainly due to its low reverse transfer characteristics. The advantages and considerations of this configuration, Figure 12, are similar to those listed for the common-source circuit. An extra advantage exists in the cascode circuit, namely the low input capacitance:

$$C_{in} = C_{gs} + (1 - A_V)\, C_{dg} \qquad (35)$$

$$C_{in} = C_{iss} + C_{gd} \qquad (36)$$

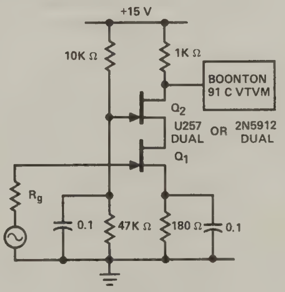


Figure 12

where A_V is the voltage gain from Q_1 gate to Q_1 drain which is essentially unity. C_{iss} for the U257 dual FET is 5 pF and C_{dg} is 1 pF, therefore

$$C_{in} = 5 + 1 = 6\ \text{pF, excluding strays of 4 pF}$$

Thus Miller effect is minimized and a good gain bandwidth product is achieved.

Figure 13 shows cascode frequency response. The voltage gain at low frequency is 15 dB (x 5.6) and the bandwidth is 24.5 MHz with a generator impedance of 50 ohms. Gain bandwidth product is 137 MHz.

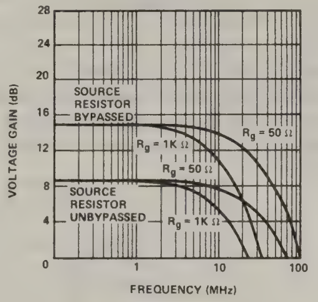


Figure 13

FET and Bipolar Cascade

The FET and bipolar transistor combination of Figure 14 makes a good video amplifier because the FET input provides the voltage gain thus obtaining a superior gain bandwidth product. The feedback capacitor a-c couples the emitter to the drain. The a-c voltage at the gate is nearly equal to that at the source. This source voltage is d-c coupled to the base.

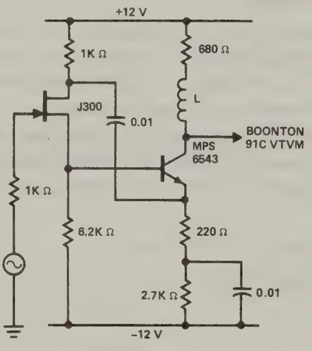


Figure 14

This produces an a-c voltage at the emitter whose amplitude is almost equal to that at the base. Thus at the FET, $v_g \cong v_s \cong v_d$ and all three signals are in phase. In this way Miller effect capacitance is largely eliminated.

The frequency response of this circuit is controlled by the output time constant if f_t of the transistor is much greater than the amplifier bandwidth. In the circuit shown the a-c load is 2.5 pF.

CONCLUSION

The input resistance of a FET is inversely proportional to the frequency squared, while the input capacitance remains constant to at least 1000 MHz.

Several video amplifier configurations are considered. The common-source circuit is considered first: in the example, the low frequency gain is 4.5 and the 30-dB bandwidth 44 MHz (gain bandwidth 197 MHz). By shunt peaking in the drain circuit, gain bandwidth is increased to 260 MHz. The simple source-follower circuit gives a gain near unity with GBW almost 300 MHz and an output resistance of $1/g_{fs}$. The cascode circuit features a low input capacitance and GBW of 137 MHz. The circuit featuring the best gain bandwidth is the FET and bipolar combination. A gain of 11 dB and bandwidth of 90 MHz is achieved.

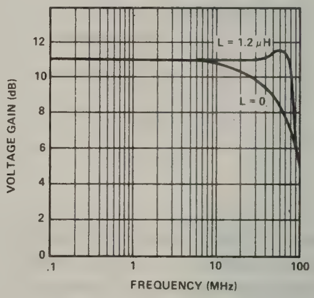


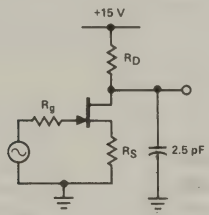
Figure 15

APPENDIX

Selection of Video Amplifier Designs with Performance Summary

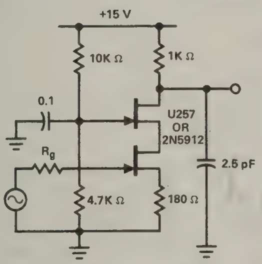
Note. All output voltages measured with Boonton 91C VTVM.

Common Source Stage



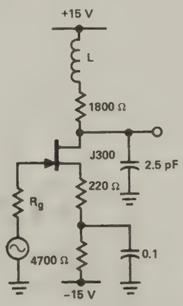
Device	R_g Ω	R_S Bypassed	R_S Ω	R_D Ω	Gain	dB	C_{in} pF	BW MHz	GBW MHz
2N4393	50		47	560	4.5	13.0		44	197
	50	x	47	560	7.5	17.5		40	300
	1K		47	560	4.5	13.0		5.0	22
	1K	x	47	560	7.5	17.5		3.5	26
J300 ½ 2N5912	50		91	1K	3.8	11.6	11.0	27.5	103
	50	x	91	1K	6.3	16.0	14.5	30.0	189
	1K		91	1K	3.8	11.6	11.0	9.5	36
	1K	x	91	1K	6.3	16.0	14.5	6.5	41
2N4416	50		120	1.5K	3.9	11.8	11.5	25	98
	50	x	120	1.5K	6.2	15.8	13	19	118
	1K		120	1.5K	3.9	11.8	11.5	8	31
	1K	x	120	1.5K	6.2	15.8	13	7	44

Cascode



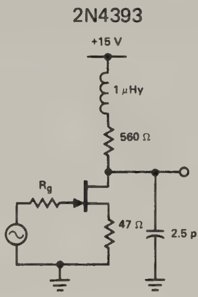
R_g Ω	R_S Bypassed	Gain	dB	C_{in} pF	BW MHz	GBW MHz
50		2.7	8.5	9	27	73
50	x	5.6	15	11.5	27	151
1K		2.7	8.5	9	9.5	73
1K	x	5.6	15	11.5	9.0	51

Common-Source Circuit

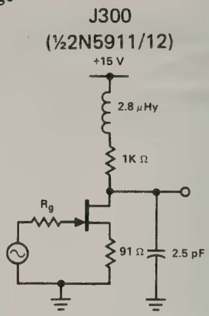


R_g Ω	L µH	Gain	dB	C_{in} pF	BW MHz	GBW MHz
50	0	3.5	11	2	20	70
1K	0	3.5	11	2	11	38.5
50	8	3.5	11	2	37	130
1K	15	3.5	11	2	17	60

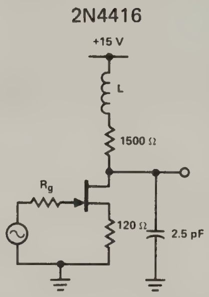
Shunt-Peaked Common-Source Stage



R_g Ω	R_S Bypassed	Gain	dB	BW MHz	GBW MHz
50		4.2	12.5	66	277
50	x	7.5	17.5	54	405
1K		4.2	12.5	6.0	25
1K	x	7.5	17.5	3.5	26

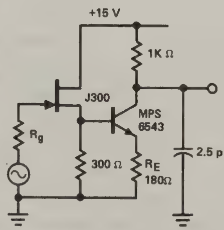


R_g Ω	R_S Bypassed	Gain	dB	BW MHz	GBW MHz
50		3.9	11.8	67	262
50	x	6.3	16.0	67	421

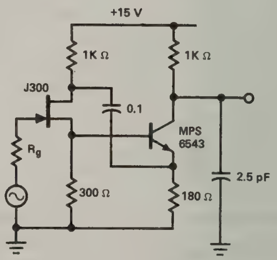


R_g Ω	L μH	R_S Bypassed	Gain	dB	BW MHz	GBW MHz
50	4		3.9	11.8	45	175
50	4	x	6.2	15.8	40	248
50	5	x	6.2	15.8	45	279

Common-Drain Common-Emitter Stage

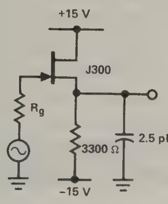


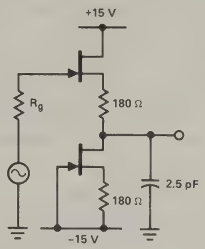
R_g Ω	R_E Bypassed (0.1 μF)	Gain	dB	C_{in} pF	BW MHz	GBW MHz
50		3	9.5	2.0	39	117
50	x	25	28	2.0	21	525
1K		3	9.5	2.0	13	39
1K	x	25	28	2.0	11	275



R_g Ω	Gain	dB	C_{in} pF	BW MHz	GBW MHz
50	5.6	15	1.0	32	179
1K	5.6	15	1.0	15	84

Source-Follower Circuit



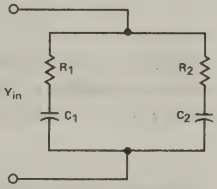


R_g Ω	Gain	C_{in} Stray pF	Total pF	R_o Ω	BW MHz	GBW MHz
50	0.92	2.2	2.7	165	350	326
1K	0.92	2.2	2.7	165	55	50

Note. R_o = output resistance of the source follower.

Dual FET	R_g Ω	Offset (Max) (Input to Output) mV	Gain	BW MHz	GBW MHz
U257	50	100	0.98	70	69
2N5912	1K	100	0.98	15	14.7
U232	50	10	0.98	85	83
	1K	10	0.98	13	12.7

Derivation of Input Admittance Terms



where

$R_1 = R_{gs} \quad C_1 = C_{gs} \quad (1)$

$R_2 = R_{gd} \quad C_2 = C_{gd} \quad (2)$

$s \;= j\omega$

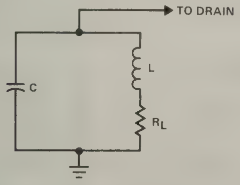
$$Y_{in} = \frac{sC_1}{R_1C_1\,s+1} + \frac{sC_2}{R_2C_2\,s+1} \qquad (3)$$

$$= \frac{-\,\omega^2C_1C_2\,(R_1+R_2) + s(C_1+C_2)}{(1-\omega^2R_1R_2C_1C_2) + s(C_1R_1 + C_2R_2)} \qquad (4)$$

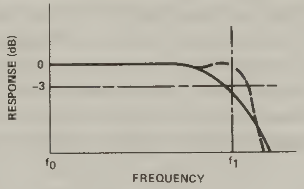
Derivation of Shunt Peaking Formula

The equivalent circuit of the drain load is shown in the Figure below. The total impedance seen by the drain is given by:

$$Z = \left[\frac{R_L{}^2 + \omega^2L^2}{(1-\omega^2LC)^2 + \omega^2C^2R_L{}^2}\right]^{\frac{1}{2}} \qquad (5)$$



The response below shows the "normal" 3-dB frequency without peaking – f_1. It is now required to raise the response at f_1 by 3 dB to achieve a maximally flat response. Therefore, under these conditions the total impedance seen by the drain at f_1 must equal the impedance seen by the drain at f_o. Also at f_1, $X_C = R_L$. Substituting for X_C in Equation 5:



$$R_L{}^2 = \frac{R_L{}^2 + \omega^2L^2}{\left(1 - \frac{\omega L}{R_L}^{2} + 1\right)} \qquad (6)$$

$$R_L{}^2 - 2\omega LR_L + \omega^2L^2 + R_L{}^2 = R_L{}^2 + \omega^2L^2 \qquad (7)$$

$$R_L{}^2 = 2\omega LR_L \qquad (8)$$

$$R_L \;= 2\omega L \qquad (9)$$

$$L \;= \frac{R_L}{4\pi\, f_1} \qquad (10)$$

and

$$f_1 \;= \frac{1}{2\pi\, R_LC}\;,\therefore L = \frac{R_L{}^2C}{2} \qquad (11)$$

REFERENCES

1. Sherwin, J.S., "Liberate Your FET Amplifier," Electronic Design, May 1970.
2. Siliconix Application Tip, "FET Cascode Circuits Reduce Feedback Capacitance," August 1970.

Siliconix

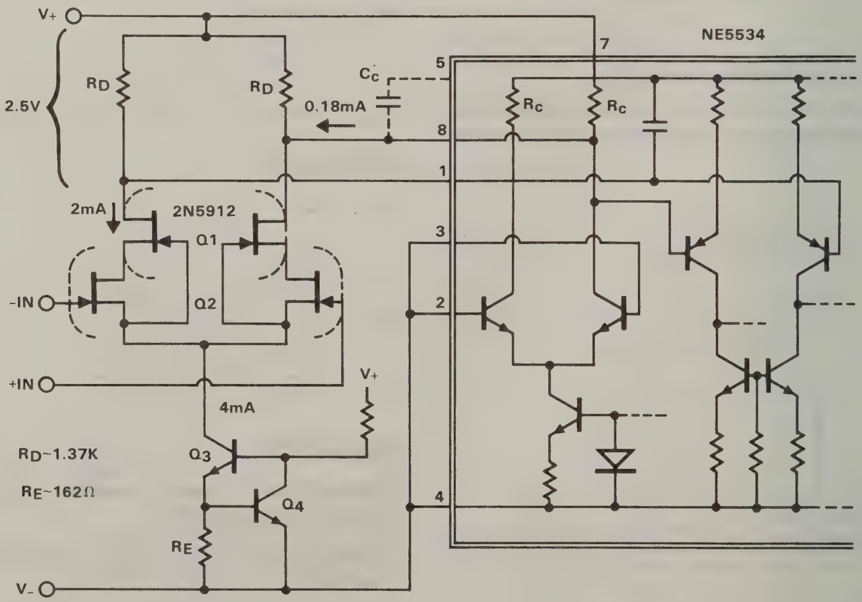
APPLICATION NOTE

Composite Op Amp for High Performance

For op amp applications requiring the best possible performance, consider a composite op amp that takes advantage of differing process technologies. A JFET dual can be combined with a Signetics NE5534 bipolar op amp for outstanding performance. Input bias current can be reduced, yet slew rate can be very high (20V/μsec to 40V/μsec) and the circuit is unity-gain stable. Output swing is a minimum of ±12V into a 600 ohm load when operating from ±15V power supplies. This high output capability combined with a JFET input stage makes this an excellent amplifier for high-speed integrators, SAMPLE/HOLD circuits, peak detectors, and log amplifiers.

The input portion of the circuit is shown in Figure 1. The NPN input stage of the NE5534 IC op amp is biased into cut-off by connecting both inverting and non-inverting inputs to the negative rail. A JFET preamplifier input stage

High Performance Op Amp Using The Siliconix 2N5912



is then connected into the PNP second stage of the NE5534 and the currents that formerly flowed through the NE5534 NPN input pair are now diverted into the JFET input pair. Drain resistors R_D effectively parallel the collector resistors R_C from within the IC op amps and the JFET drain currents will then be the sum of the currents through R_D and R_C. The voltage across the parallel combination of R_D and R_C is nominally 2.5V due to the internal biasing of the NE5534. Going directly into the second stage of the IC op amp rather than into the NE5534 NPN input stage has two distinct advantages:

1. Frequency response is better in that the phase shift of the bipolar input stage is avoided. A high-current JFET input stage, such as the 2N5912 when operated in the 1mA to 8mA drain current range, has excellent frequency response in comparison to an NPN stage operating in the 150μA to 200μA range.
2. The operating level at the JFET drains is only 2.5V below the positive supply rail, therefore the common-mode input range for the JFET input stage can be relatively high. The combination of low input bias current with high frequency response is useful for SAMPLE/HOLD circuits, high-speed integrators, photo-multiplier tube amplifiers, and high-speed data conversion circuits.

Although more expensive than a single monolithic op amp, the combination of a JFET preamp with a bipolar IC second stage can provide substantially better performance than any monolithic alternatives.

A Siliconix 2N5912 JFET dual was chosen for the input stage in this example because of its high operating current range, high gain, and excellent frequency response. The saturation drain current I_{DSS} has a specified range of 7mA to 40mA, but is typically 10mA to 24mA. Gate source cutoff voltage $V_{GS(off)}$ is in the range of –1V to –5V with a typical value of approximately –2V to –4V. The 2N5912 characterization curves indicate that any drain current from 1mA to 8mA will provide good performance, and 2mA was chosen for this application.

The current diverted from the bipolar input stage to the JFET input stage is nominally 180μA on each side; therefore a drain current on each side of 1.82mA is needed from the drain resistors R_D to make up a total drain current of 2.0mA. The drain resistor R_D therefore needs to be approximately 2.5V/1.82mA, or 1370 ohms on each side.

Gain of the JFET input stage can now be calculated. From the 2N5912 characterization curves, forward transconductance g_{fs} will be in the range of 2.6mmhos to 5mmhos for units having I_{DSS} of 10mA to 24mA and when operated at a drain current of 2mA. The differential gain can be approximated by the product $g_{fs}\,R_D$. Using a center value of 4.3mmhos and 1230 ohms, (R_D and R_C in parallel), then the gain will be approximately 6.5, or 16dB. Total amplifier gain was found to closely approximate the gain curve for a 5534 being operated alone.

The cascode configuration using two input pairs as shown has several advantages. Most importantly, the input gate current is dramatically reduced due to the lower drain-to-gate voltage on the input pair. In the cascode configuration, the gate-to-source voltage on the upper pair will be the drain-to-source voltage of the input pair even with the common-mode input variations. All of the common-mode swing is taken up by variations in V_{DS} of the upper pair. Gate leakage of the input pair is primarily dependent on drain-to-gate voltage V_{DG}, which will be a constant $-2V_{GS}$ in this cascode configuration. Drain-to-gate voltage on the input pair will be low, typically in the 3V to 6V range, which is well below the "I_G breakpoint". From the characterization curves on the 2N5912, gate current leakage will be under 2pA for drain-to-gate voltages under 6V. The cascode configuration is very effective in reducing input bias current for JFET input stages. Another advantage of the cascode configuration is a reduction of input capacitance. The input pair drains are "bootstrapped" to the common source point and both must follow the gate voltage. The effective capacitance from gate-to-drain and from gate-to-source is reduced. In addition, output conductance is reduced by the cascode configuration which also helps CMR. Adding the second JFET pair significantly improves both input bias current and common-mode rejection without degrading other parameters.

The constant current source consisting of Q3 and Q4 primarily improves common-mode rejection and rejection of power supply variation. It also establishes the nominal operating voltage at the input (pins 1 and 8) of the 5534 op amp. The current will be a constant V_{BE}/R_E independent of fluctuations in power supply voltage or input voltage level. This current source has very high impedance, therefore common-mode inputs are heavily attenuated.

Common-mode-rejection-ratio (CMRR) is very high due to the use of a constant current source, but can be further improved by matching of drain resistance. The parallel combination of R_D and R_C is the effective drain resistance for this design. The transconductance ratio between the two sides of the input pair also directly affects CMRR. The drain resistors should be well-matched to minimize the CMRR adjustment range since it also affects offset and drift.

Each 1% mismatch in drain resistance will cause approximately 11μV/°C of input offset voltage drift. CMRR can be readily trimmed to over 100dB. CMRR vs. frequency is excellent due to the use of the 2N5912, a wide-bandwidth FET, in a cascode configuration.

A high performance op amp should also have good output characteristics, low noise, and high slew rate. The NE5534 op amp is rated for ±14V mimimum output swing into a 600 ohm load when operating from ±15V power supplies. Output resistance is typically 0.3 ohms. The Siliconix

2N5912 characterization curves show a typical equivalent input noise voltage of only 10nV/$\sqrt{\text{Hz}}$ at 10Hz. There is also a component of noise from the second stage, but its effect is divided by the input stage gain and its contribution is small. Input current noise of this composite op amp is very low due to the typical operating level of 1pA input bias current. For slew rate, this circuit is capable of 50V/μsec when going negative. Positive slew rate is 50V/μsec without use of a compensation capacitor, but drops to 25V/μsec with a 20pF compensation capacitor. Compensation capacitance will generally be needed only when driving capacitive loads. Even the lower value of slew rate, 25V/μsec, corresponds to a full-power (±10V) frequency of 400KHz.

While the vast majority of op amp applications can be satisfied through use of conventional IC op amps, there are applications in high-performance instrumentation systems that require superior performance. This composite op amp, which makes use of precision dual JFET input pairs and a high performance IC op amp, provides a unique combination of low input bias current, high CMR, low noise, excellent frequency response, and high output swing.

APPLICATION NOTE

FETs in Balanced Mixers

Ed Oxner

INTRODUCTION

When high-performance, high-frequency junction field-effect transistors (JFETs) are used in the design of active balanced mixers, the resulting FET mixer circuit demonstrates clearly superior characteristics when compared to its popular passive counterpart employing hot-carrier diodes. Comparison of several types of mixers is made in Table I. The advantages and disadvantages of semiconductor devices currently used in various mixer circuits are shown in Table II.

Why an Active Mixer?

Active mixing suggests high-level mixing capability. High level mixing in turn infers that active mixers outperform passive mixer circuits in terms of wide dynamic range and large-signal handling capability. Additionally, the active mixer offers improved conversion efficiency over the passive mixer, permitting relaxation of the IF amplifier gain requirements and even possible elimination of the customary RF amplifier front end.

Initial evaluation of the active FET mixer will imply a disadvantage because of local oscillator drive requirements; bipolar devices in low-level mixers require very little drive power. However, in high-level mixing this disadvantage is overcome in that drive requirements at such mixing levels are generally the same, no matter whether bipolar or FET devices are used.

Why FETs for Balanced Mixers?

The performance priorities of modern communication systems have stringent requirements for wide dynamic range, suppression of intermodulation products, and the effects of cross-modulation. All of the foregoing parameters must be considered before noise figure and gain are taken into account.

Since FETs have inherent transfer characteristics approximating a square-law response, their third-order intermodulation distortion products are generally much smaller than

Table I

	MIXER TYPE		
Characteristic	**Single-Ended**	**Single Balanced**	**Double Balanced**
Bandwidth	Several decades possible	Decade	Decade
Relative IM Density	1.0	0.5	0.25
Interport Isolation	Little	10-20 dB	>30 dB
Relative L.O. Power	0 dB	+3 dB	+6 dB

Table II

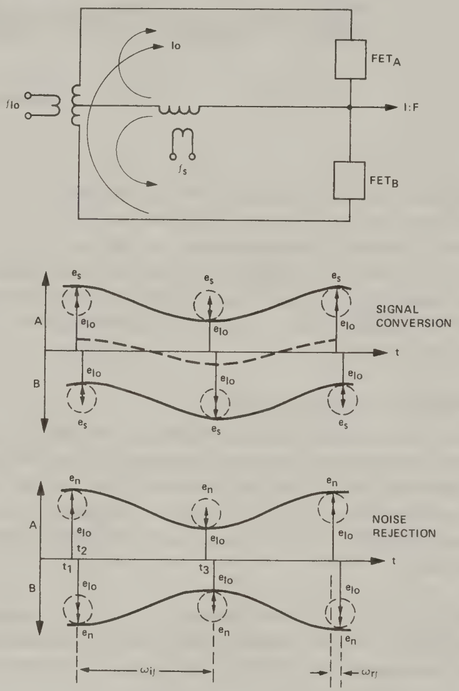
DEVICE	ADVANTAGES	DISADVANTAGES
Bipolar Transistor	Low Noise Figure High Gain Low D.C. Power	High IM Easy Overload Subject to Burnout
Diode	Low Noise Figure High Power Handling High Burn-out Level	High L.O. Drive Interface to I.F. Conversion Loss
JFET	Low Noise Figure Conversion Gain Excellent IM products Square Law Characteristic Excellent Overload High Burn-out Level	Optimum Conversion Gain not possible at Optimum Square Law Response Level High L.O. Power
Dual-Gate MOS FET	Low IM Distortion AGC Square Law Characteristic	High Noise Figure Poor Burnout Level Unstable

those of bipolar transistors. Harmonic distortion and cross-modulation effects are third-order-dependent, and thus are greatly reduced when FETs are used in active balanced mixers.

A secondary advantage derives from available conversion gain, so that the FET mixer becomes simultaneously equivalent to both a demodulator and a preamplifier.

First Order Balanced Mixer Theory

Essential details of balanced mixer operation, including signal conversion and local oscillator noise rejection, are best illustrated by signal flow vector diagrams (Figure 1).



Signal and Noise Vectors
Figure 1

Energy conversion into the intermediate frequency (IF) passband is the major concern in mixer operation. In the following analysis, both the signal and noise vectors are shown progressing (rotating) at the IF rate (ω_{ift}); the resulting wave occurs through vector addition.

The analysis of local oscillator noise rejection (Figure 1) assumes, for simplicity of explanation, that noise is coherent. Thus at some point in time (t_1) the noise component (e_n) is "in phase" with the local oscillator vector (e_{lo}) and FET "A" (the rectifying element) is ON; the JFET mixer acts as a switch, with the local oscillator acting as the switch drive signal. One-half cycle later, at time t_2, the signal flow is reversed for both the local oscillator vector and the noise component, FET "A" is OFF and FET "B" is ON. Moving ahead an additional one-half of the IF cycle, FET "A" is again ON, but the noise component has advanced 180° (ω_{ift}) through the coupling structure, and is now "out of phase". The process continually repeats itself.

The end result of this averaging (detection) is the cancellation of the noise which originated in the local oscillator, providing that the mixer balance is precise.(1)

The analysis of the conversion of the signal to the IF passband is similar, but the signal is injected into the coupling structure at the equipotential tap. Thus at time t_2, the signal vector (e_s) is "out of phase" with the local oscillator vector, e_{lo}. The resulting envelope develops a cyclic progression at the IF rate, since the signal is "demodulated" by the mixing action of the FETs.

A schematic of a *prototype* balanced mixer is shown in Figure 2. Design criteria, in order of priority, include the following:

(1) Intermodulation and Cross-Modulation
(2) Conversion Gain
(3) Noise Figure
(4) Selecting the Proper FET
(5) Local Oscillator Injection
(6) Designing the Input Transformer
(7) Designing the IF Network

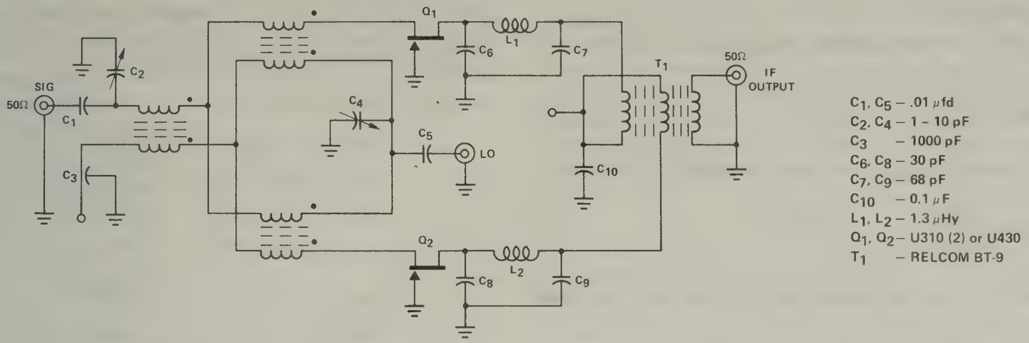
Intermodulation and Cross-Modulation

A basic aim in mixer design is to avoid the effects of intermodulation product distortion and crossmodulation. Part of the problem may be resolved by using a balanced mixer circuit.

The active transfer function of the FET is represented by a voltage-controlled current source. For both crossmodulation and intermodulation, the amount of distortion is proportional to the amplitude of the gate-source voltage. Since input power is proportional to input voltage, and inversely proportional to input impedance, the best FET IM and cross-modulation performance is obtained in the common-gate configuration where the impedance is lowest.(2)

When JFETs are used as active mixer elements, it is important that the devices be operated in their square-law region. Operation in the FET square-law region will occur with the device in the depletion mode. Considerable distortion will result if the FET is operated in the enhancement mode (positive, for an N-channel FET); by analogy, the problems encountered are similar to those which arise when positive drive is placed on the grid of a vacuum tube.

Square-law region operation emphasizes the importance of establishing proper drive levels for both quiescent bias and the local oscillator. The maximum conversion transconductance, g_c, is achieved at about 80% of the FET gate cutoff voltage, $V_{GS(off)}$, and amounts to about 25% of the forward transconductance, g_{fs}, of the FET when used as an amplifier.



Prototype Active Balanced Mixer

Figure 2

Since conversion gain (or loss) must be considered, it is common to equate voltage gain A_v, as:

$$A_v = g_c R_L \qquad (1)$$

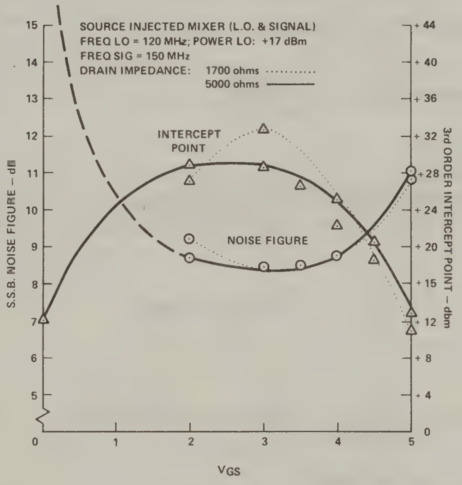
where g_c is the conversion transconductance and R_L is the FET drain load.

An attempt to achieve maximum conversion gain by indiscriminately increasing the drain load resistance will adversely affect any design priority concerning distortion — particularly intermodulation product distortion.

Distortion takes different forms in mixers. Most obvious is that distortion which will occur if the FET is driven into the enhancement mode, as noted earlier. A more pernicious form is drain load distortion. And finally, there is the so-called "varactor effect."

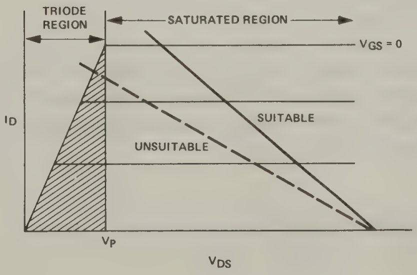
The most frequent cause of poor mixer performance stems from signal overloading in the drain circuit. Excessive drain load impedance degrades the intermodulation characteristics and produces unwanted crossmodulation signals.(3) A characteristic of the FET balanced mixer is that the correct drain load impedance is inversely proportional to the value of the conversion transconductance. Figure 3 shows the improvement in IM characteristics obtained in the prototype mixer with the drain load impedance reduced to 1700 Ω from 5000 Ω. Specifically, the dynamic load line must be plotted so that the signal peaks of the instantaneous peak-to-peak output voltage are not permitted to enter into the non-saturated ("triode") region of the FET. Suitable and unsuitable drain load lines are shown in Figure 4. Load impedance selection is quantified in Equations 18 through 20.

Distortion from the "varactor effect" is of secondary importance, and arises from an excessive peak voltage signal swing, where the changing drain-to-sorce voltage can cause a change in parasitic capacitance, C_{rss}, and give rise to harmonics.(4) A FET tends to be voltage-dependent when the drain voltage falls appreciably below 6 volts. If the source voltage (from the power supply) is also low and the drain load impedance is high, then distortion will develop. However, if proper steps are taken to prevent drain load distortion, the varactor effect will also be inhibited.



Comparison of Mixer IM Characteristics

Figure 3



Plotting Drain Load Lines

Figure 4

Conversion Gain

In a FET, forward transconductance is defined as$^{(5)}$

$$g_{fs} = \frac{dI_D}{dV_{gs}} \tag{2}$$

and conversion transconductance is defined as$^{(6)}$

$$g_c = \frac{dI_{D(\omega i)}}{dV_{gs(\omega r)}} \tag{3}$$

where ωi = the intermediate frequency and ωr = the signal frequency.

The effects of time-varying local oscillator voltage, V_2, and the much smaller signal voltage, V_1, must be considered:

$$v_{gs} = V_1 \cos \omega_1 t + V_2 \cos \omega_2 t \tag{4}$$

For square law operation$^{(7)}$

$$V_2 + V_{GS} \leqslant V_{GS(off)} \tag{5}$$

Drain current is approximately defined by $^{(8)}$

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 \tag{6}$$

or $^{(9)}$

$$I_D \approx \frac{g_{fso}\, V_{GS(off)}}{2} \left[1 - \frac{v_{gs}}{V_{GS(off)}}\right]^2 \tag{7}$$

or

$$I_D \approx \frac{g_{fso}}{2V_{GS(off)}} \left[V_{GS(off)} - v_{gs}\right]^2 \tag{8}$$

then $^{(10)}$

$$I_D \approx \frac{g_{fso}}{2V_{GS(off)}} \quad \text{(complex Taylor expansion)} \tag{9}$$

which can be reduced to

$$I_{D(IF)} \approx \frac{g_{fso}}{2V_{GS(off)}} \quad V_1\, V_2 \cos(\omega_1 - \omega_2)t \tag{10}$$

and the conversion transductance is

$$g_c = \frac{g_{fso}}{2V_{GS(off)}} \;|V_2| \tag{11}$$

Equation 11 suggests that g_c increases without limit as V_2 increases without limit. However, to avoid operation of the FET in the "triode" region, the peak-to-peak swing of V_2 should not exceed $V_{GS(off)}$.

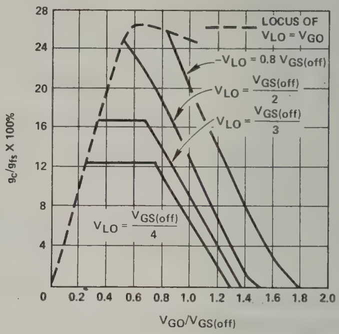
Thus

$$2\, V_2 \text{ peak} \leqslant V_{GS(off)} \tag{12}$$

or

$$V_2 \text{ peak} \leqslant \frac{V_{GS(off)}}{2} \tag{13}$$

Figure 5 shows plots of normalized conversion transconductance, g_c/g_{fs} versus normalized quiescent bias, $V_{GS}/V_{GS(off)}$, for different oscillator injections.

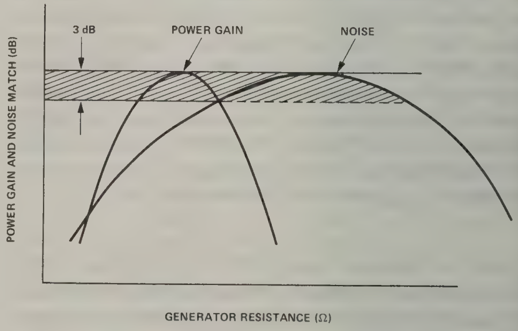


Normalized g_c/g_f vs. $V_{GS}/V_{GS(off)}$
(from "FET RF Mixer Design Technique", S.P. Kwok, WESCON Convention Record (1970) 8/1, p.2.)
Figure 5

Noise Figure

Like the common-gate FET amplifier, the common-gate FET balanced mixer is sensitive to generator resistance, R_g.$^{(11)}$ A change of a decade in R_g can produce a noise figure variation of as much as 3 dB.

In the design of the prototype FET active balanced mixer, the generator resistance of the FETs is established by the hybrid coupling transformer. Two important criteria for the FETs in the circuit are high forward transconductance, and a value of power-match source admittance, g_{igs}, which closely matches the output admittance of the coupling transformer. In the common-gate configuration, match points for optimum power gain and noise do not occur at the same value of generator resistance (Figure 6). Optimum noise match can only be achieved at the sacrifice of bandwidth.



Power Gain and Noise Matching
Figure 6

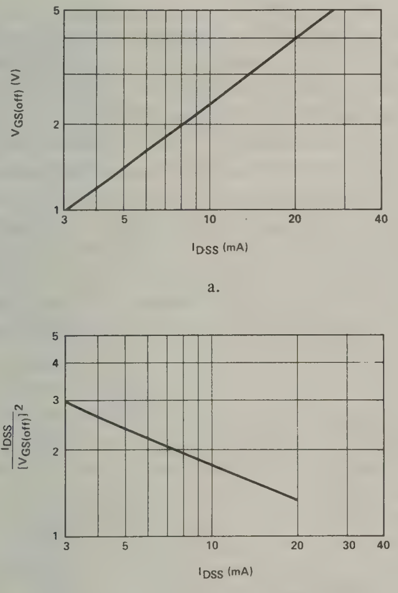
How to Select the Proper FET

Conversion efficiency is determined by conversion transconductance, g_c, which in turn is directly related to such FET parameters are zero-bias saturation current, I_{DSS}, and the gate cutoff voltage, $V_{GS(off)}$:

$$g_c = \frac{I_{DSS}}{V_{GS(off)}{}^2}\ |V_2| \qquad (14)$$

$$\approx \frac{g_{fso}}{2V_{GS(off)}} \qquad (15)$$

Equation 15 appears to indicate that FETs with high I_{DSS} are to be preferred. However, I_{DSS} and $V_{GS(off)}$ are related, and Figures 7A and 7B show that devices from a family selected for high I_{DSS} do *not* provide high conversion transconductance, but actually produce a lower value of g_c.



a.

b.

Relationship of I_{DSS} and $V_{GS(off)}$
Figure 7

Best mixer performance is achieved with "matched pairs" of JFETs. Basic considerations in selecting FETs for this application are gate cutoff voltage, $V_{GS(off)}$, for good conversion transconductance, and zero-bias saturation current, I_{DSS}, for dynamic range. A match to 10% is generally adequate. Among currently available devices, the Siliconix U310 and the dual U431 offer excellent performance in both categories; common-gate forward transconductance is 20,000 μmhos max at V_{DS} = 10 V, I_D = 10 mA, and f = 1 kHz.

There is, of course, the possibility that FET cost is a major consideration in evaluating the active balanced mixer approach – the familiar price/performance tradeoff. If this is the case, there are a number of other Siliconix FETs which will provide suitable alternatives to the U310. Remember, however, that conversion transconductance, g_c, can never be more than 25% of forward transconductance. Thus as tradeoff considerations begin, the first sacrifice to be made will be the degree of achievable conversion gain. Intermodulation performance will follow with the third tradeoff being available noise figure. Table III lists a number of possible alternatives to the U310.

Table III

Typical Characteristic	DEVICE TYPE			
	U310*	2N5912	2N4416*	2N3823
g_m	14K	6K	5K	3.5K
I_{DSS}	40 mA	15 mA	10 mA	10 mA

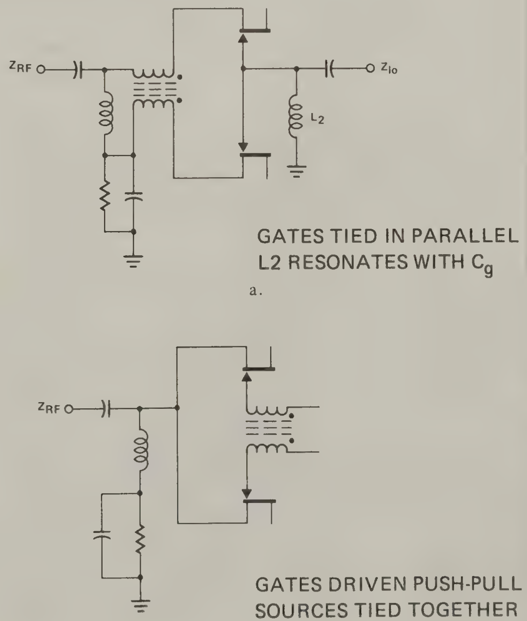
*Similar devices are also available in plastic packages:

U310 (J310)
2N4416 (2N5486, J304-18)

Local Oscillator Injection

Low IM distortion products and noise figure, plus best conversion gain, will be achieved if the voltage swing of the local oscillator across the gate-to-source junction is held to the values presented in Figure 5. V_{LO} is expressed in terms of peak-to-peak voltage, while $V_{GS(off)}$ is a d.c. voltage.

Local oscillator injection can be made either through a brute-force drive into the JFET source through the hybrid input transformer, or through a direct-coupled circuit to the JFET gates where less drive will be required for the desired voltage swing, Two circuits to obtain direct gate coupling are suggested in Figure 8.



a.

b.

Alternate Forms of L.O. Injection
Figure 8

The source-injection method is used in the design of the present mixer to maintain the inherent stability of a common-gate circuit. A minor disadvantage with the direct-drive method is that the required gate-to-source voltage swing requires considerable local oscillator input power. For source injection through the transformer, best mixer performance is obtained with a local oscillator drive level of +12 to +17 dBm across a 50-ohm load.

Conversely, direct coupling to the FET gates occurs at a higher impedance level and less local oscillator drive power is required. The functional tradeoff resulting when the gates are tied together is that shunt susceptance requires some form of conjugate matching, and thus brings about an undesirable reduction of instantaneous mixer bandwidth.

Designing the Input Transformer

Five criteria are important to the design of the hybrid input coupling transformer for best mixer performance. The impedance transformer must

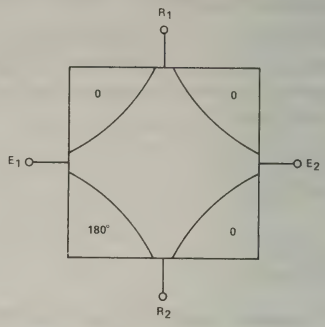
(1) Consist of four single-ended terminals, for the local oscillator, the input signal and FETs A and B

(2) Offer a match between either input to a symmetrical balanced load

(3) Provide as much isolation as possible between the signal and local oscillator ports (Figure 9)

(4) Maintain a differential phase of 180° across the symmetrical balanced loads

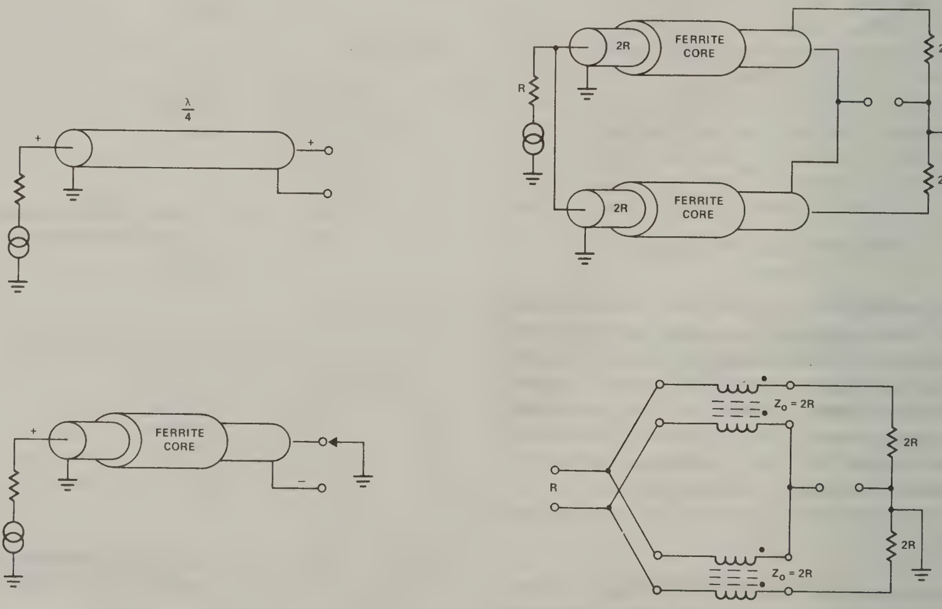
(5) Introduce the least possible amount of loss



4-Port Hybrid with Phase and Isolation

Figure 9

A transformer using ferrite cores and meeting these five requirements is derived from elementary transmission-line theory (Figure 10). Transmission line transformers have a low-frequency cutoff determined by the falloff of primary reactance as frequency is decreased. This reactance is determined by the series inductance of the transmission line conductors. On the other hand, high-frequency performance is enhanced by minimizing the physical length of the transmission line. Minimizing overall line length while maintaining suitable reactance can be accomplished by using a high-permeability core material such as a ferrite.(12) The transformer constructed for the balanced FET mixer closely resembles the balanced 4-port unsymmetrical 180° hybrid device described by Ruthroff.(13)



Hybrid Input Coupling Transformer

Figure 10

Although Ruthroff does not discuss the method of determining the winding length of bifilar wire, a solution is offered by Pitzalis.(14) The Pitzalis definitions for wire length are as follows (Figure 11):

$$\text{max length} = \frac{7200n}{f_{upper}} \text{ (inches)} \qquad (16)$$

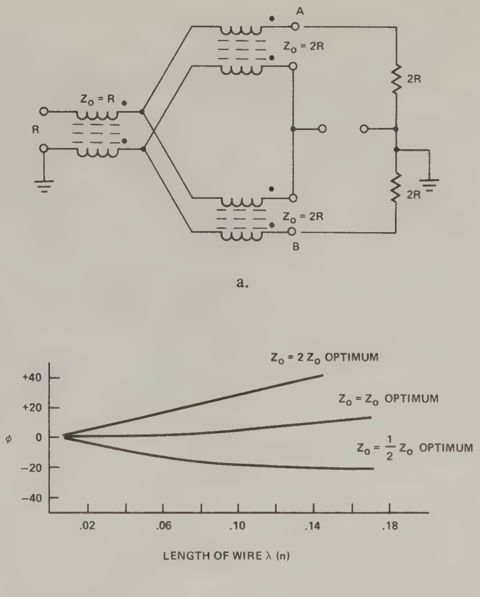
$$\text{min length} = \frac{20\,R_L}{(1 + \mu/\mu_o)\,f_{lower}} \text{ (inches)} \qquad (17)$$

where R_L = the load impedance, μ/μ_o = the relative permeability of the ferrite at the lower frequency, and n = a fractional wavelength determined by the amount of allowable phase error.

Selection of the ferrite core material is determined mainly by performance requirements. A prime consideration for wideband performance is the temperature coefficient of the ferrite, which must have a low loss tangent over the required temperature range, i.e., high Q.

In addition, an important design factor involves the relative permeability of the core, since inductance of a conductor is proportional to the permeability of the surrounding medium.(15) A high permeability material placed close to the transmission line conductors acts upon the external fringe field present, appreciably magnifying the inductance and providing a lower cutoff frequency. Power transferred from input to output is coupled directly through the dielectric medium separating the transmission line condcutors; thus a relatively small cross-section of ferrite material can operate in an unsaturated state at impressively high power levels. For the FET balanced mixer, ferrite core material with a permeability of 40 provides satisfactory operation from 50 to 250 MHz. Figure 11 also demonstrates that a lower transmission line impedance, Z_o, is to be preferred over a higher Z_o. Both 50-ohm and 100-ohm transmission lines are required for the mixer transformer; twisted pairs will provide satisfactory results. A characteristic impedance of 45 Ω is obtained from 3 turns-per-inch of Belden No. 24 AWG enamel wire, while 3½ turns-per-inch of No. 24 (7X32) Belden plastic covered wire provide Z_o = 100 ohms. Each core is wound with 2 inches of the proper twisted pair, with min/max lengths calculated from Pitzalis' data (Formulae 16, 17).

As with all broadband transformers, the coil has an inherent parasitic inductance which must be capacitor-compensated (C_2, C_4, Figure 2).(16) A trim capacitor is required at the two input terminals, and is adjusted *only once* to optimize the differential phase shift across the symmetrical balanced FETs. Phase match of the hybrid structure may be tracked to within ±2 degrees (about 180°) to 250 MHz. Effective resistance transformation is useful from 50 to 550 MHz (Figure 12) – but phase track beyond 250 MHz *may* show too much deterioration.



a.

b.

Toroid Coil Winding Data

Figure 11

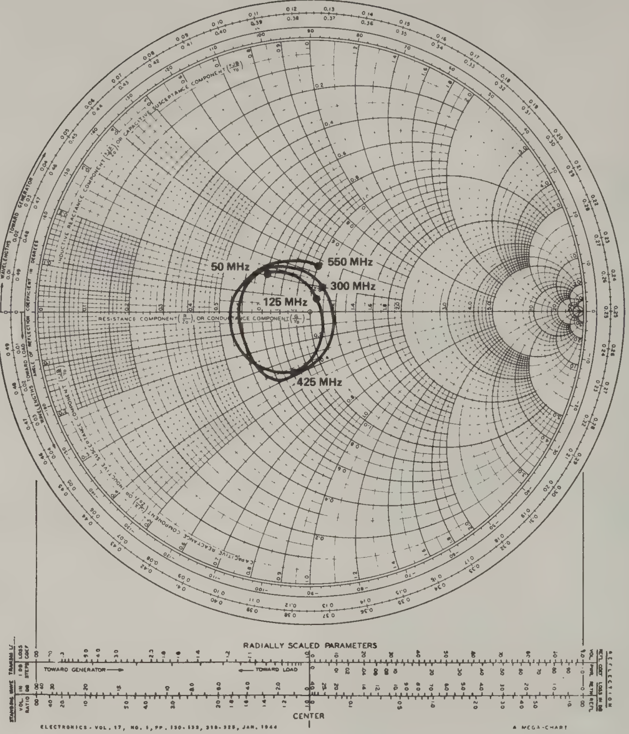
Designing the IF Network

The IF network performs two important functions in the FET balanced mixer circuit. It provides for optimum match between the FETs and the IF amplifier, and it effectively bypasses the circuit RF components (signal and local oscillator).

In network design, it is essential that the RF and local oscillator signals be sufficiently isolated from the intermediate frequency signal to maintain rejection levels of at least 20 dB. If this isolation is not maintained, conversion gain and noise figure are degraded.

The simplest technique for design of the IF network is to use the well-known pi (π) match structure from each FET drain to a common balanced output transformer network.(17) This pi match technique is especially suitable for a narrow-band intermediate frequency output, serving three useful functions. First, it serves to achieve the proper drain load match between the FETs and the IF structure. Second, it provides the very necessary isolation of the intermediate frequency signal. And third, it serves as a simple filter to provide a monotonic decrease in impedance as frequency departs from the IF center frequency, f_o.(18, 19) This third function, shown in Figure 13, prevents the drain load impedance from skyrocketing out of control and giving rise to distortion products.

Selection of the dynamic drain impedance value in the IF network is a critical point in design of the structure. Intermodulation product distortion and crossmodulation will be



50Ω – 200Ω Balun
Figure 12

both affected by the instantaneous peak-to-peak output voltage of the FETs, if the value of the dynamic drain impedance allows these signal peaks to enter either the pinch-off voltage or breakdown voltage regions of the transistors.(20) If the impedance is too high, the dynamic range of the mixer will be severely limited; if the impedance is too low, useful conversion gain will be sacrificed.

A first-order approximation to establish the proper load impedance may be obtained when

$$R_L = \frac{V_{DD} - 2\,V_{GS(off)}}{i_d} \qquad (18)$$

where

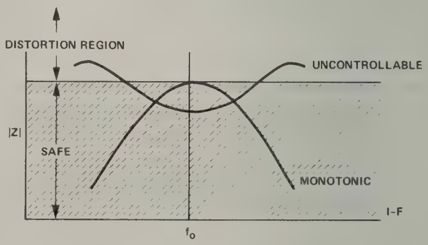
$$i_d = I_{DSS}\left[1 - \frac{v_{gs}}{V_{GS(off)}}\right]^2 \qquad (19)$$

and

$$v_{gs} = V_{GS} + V_1 \sin \omega_1 t \qquad (20)$$

For the U310 FET, the optimum drain load impedance is established at slightly less than 2000 ohms, with sufficient local oscillator drive and gate bias determined from the conversion transconductance curve in Figure 5.

The output IF coupling structure is an 800-ohm CT to 50-ohm trifilar-wound transformer (Relcom BT-9 or equivalent). The pi (π) match into this transformer provided a dynamic drain load impedance of 1700 ohms on each FET; excellent



Pi (π) Match Filter Function
Figure 13

IM performance was obtained. Value of operating Q was established at 10 as the best compromise to insure that the tolerance of the pi match components would permit the IF output to peak within the allowable bandwidth at the associated IF amplifier. A Q of more than 10 would result in a greatly restricted bandwidth, while a Q of less than 10 would result in excessively high capacitance, excessively low inductance, and unsatisfactory filter performance.

Mixer Performance

Tests of the operational prototype FET balanced mixer demonstrated that the active mixer has several characteristics superior to those of passive mixer counterparts. These comparisons are made in Table IV (measurements of all three mixers were made under laboratory conditions).

Insertion loss measurements on the IF network amounted to 3 dB in the center of the passband, while insertion loss on the hybrid assembly measured 1.2 dB. The network exhibited a Q of 10. Gain and noise figures were measured over the full 50-250 MHz bandwidth, with a single-sideband noise figure ranging from 7.2 dB at 50 MHz to 8.6 dB at 250 MHz. Conversion gain was a flat +2.5 dB.

Two-tone third-order intermodulation is expressed in terms of the intercept point.(21) With two signals 300 kHz apart, the balanced mixer suppressed third-order products –89 dB with both signals at –10 dBm, representing an intercept point of +32 dBm.

Table IV

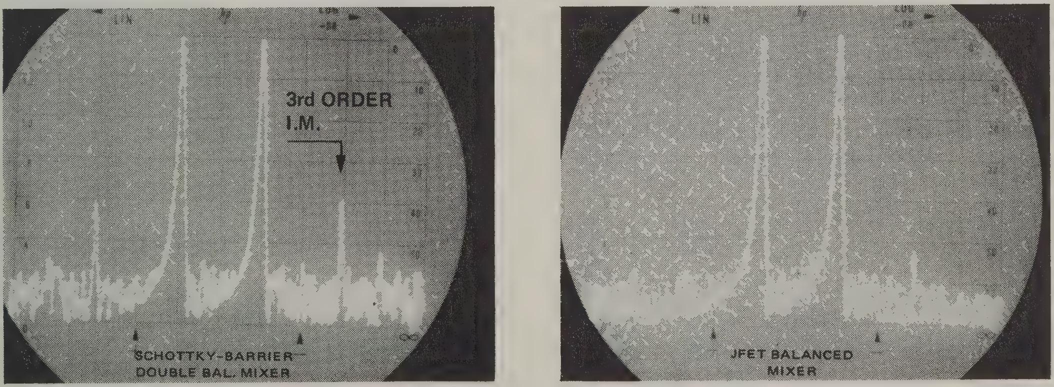
50-250 MHz Mixer Performance Comparison

Characteristic	JFET	Schottky	Bipolar
Intermodulation Intercept Point	+32 dBm	+28 dBm	+12 dBm†
Dynamic Range	100 dB	100 dB	80 dB†
Desensitization Level (the level for an unwanted signal when the desired signal first experiences compression)	+8.5 dBm	+3 dBm	+1 dBm†
Conversion Gain	+2.5 dB*	–6 dB	+18 dB
Single-sideband Noise Figure @ 50 MHz	7.2 dB	6.5 dB	6.0 dB

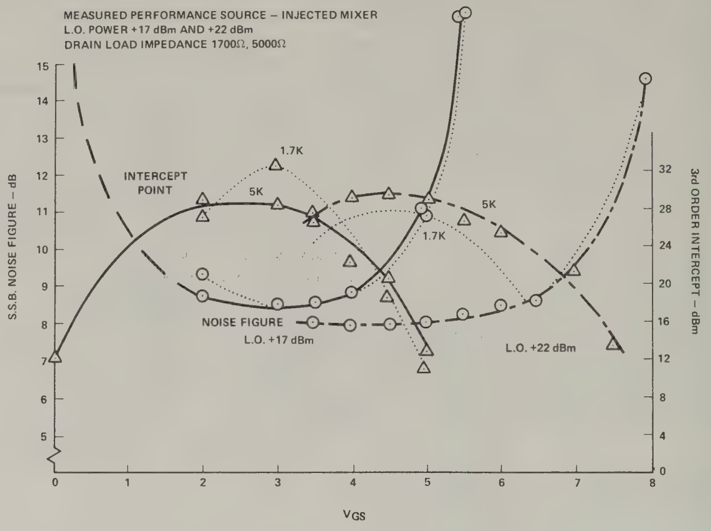
†Estimated *Conservative minimum

Figure 14 shows a comparison of third-order IM products emanating from both the JFET balanced mixer and a typical low-level double-balanced diode mixer, under similar operating conditions. Noise figure and intercept point are shown at various bias and local oscillator drive levels in Figure 15.

The performance of the active mixer is clearly superior to that of the diode mixers, contributing overall system gain in areas critical to telecommunications practice, and reducing associated amplifier requirements.



Comparison of 3rd Order IM Products
Figure 14



Noise Figure and Intercept Point Performance

Figure 15

CONCLUSION

The reason for using the three-core bifilar transformer (Figure 11A) in this tutorial article stemmed from the relative analytical simplicity of such a design. An alternative transformer is the single-core trifilar-wound design. The definitions for wire lengths (Equations 16 and 17) are equally applicable to trifilar as they are for bifilar.

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APPLICATION NOTE

FETs As Voltage-Controlled Resistors

INTRODUCTION

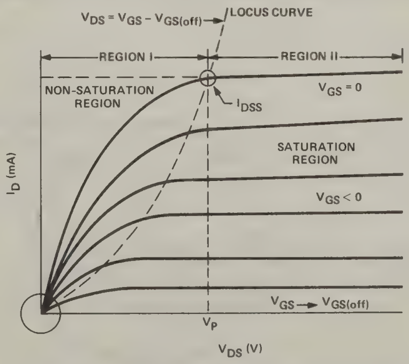
The Nature of VCRs

A voltage-controlled resistor (VCR) may be defined as a three-terminal variable resistor where the resistance value between two of the terminals is controlled by a voltage potential applied to the third.

A junction field-effect transistor (JFET) may be defined as a field-controlled majority carrier device where the conductance in the channel between the source and the drain is modulated by a transverse electric field. The field is controlled by a combination of gate-source bias voltage, V_{GS}, and the net drain-source voltage, V_{DS}.

Under certain operating conditions, the resistance of the drain-source channel is a function of the gate-source voltage alone and the JFET will behave as an almost pure ohmic resistor.(1) Maximum drain-source current, I_{DSS}, and minimum resistance, $r_{DS(on)}$, will exist when the gate-source voltage is equal to zero volts ($V_{GS} = 0$). If the gate voltage is increased (negatively for N-Channel JFETs and positively for P-Channel) the resistance will also increase. When the drain current is reduced to a point where the FET is no longer conductive, the maximum resistance is reached. The voltage at this point is referred to as the pinchoff or cutoff voltage and is symbolized by $V_{GS} = V_{GS(off)}$. Thus the device functions as a voltage-controlled resistor.

Figure 1 details typical operating characteristics of an N-Channel JFET. Most amplification or switching operations of FETs occur in the constant-current (saturated) region, shown as Region II. A close inspection of Region I (the unsaturated or pre-pinchoff area) reveals that the effective slope indicative of conductance across the channel from drain to source is different for each value of gate-source bias voltage.(2) The slope is relatively constant over a range of applied drain voltages, so long as the gate voltage is also constant and the drain voltage is low.

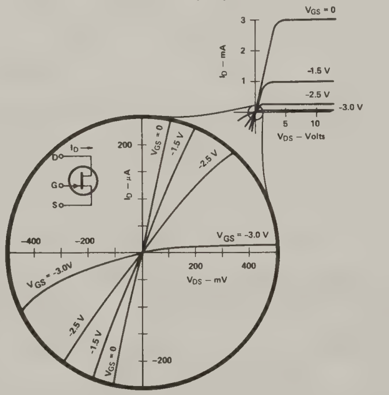


Typical N-Channel JFET Operating Characteristics
Figure 1

Resistance Properties of FETs

The unique resistance-controlling properties of FETs can be deduced from Figure 2, which is an expanded-scale plot of the encircled area in the lower left-hand corner of Figure 1. The output characteristics all pass through the origin, near which they become almost straight lines so that the incremental value of channel resistance, r_{ds}, is essentially the same as that of d.c. resistance, r_{DS}, and is a function of V_{GS}.(3)

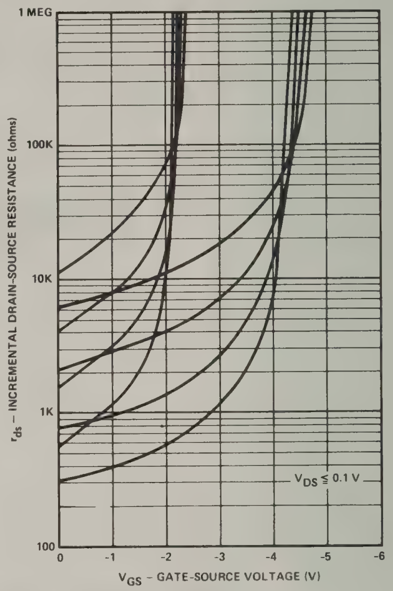
Figure 2 shows extension of the operating characteristics into the third quadrant for a typical N-Channel JFET. While such devices are normally operated with a positive drain-source voltage, small negative values of V_{DS} are possible. This is because the gate-channel PN junction must be slightly forward-biased before any significant amount of gate current flows. The slope of the V_{GS} bias line is equal to $\Delta I_D/\Delta V_{DS} = 1/r_{DS}$. This value is controlled by the amount of voltage applied to the gate. Minimum r_{DS}, usually expressed as $r_{DS(on)}$, occurs at $V_{GS} = 0$ and is dictated by the geometry of the FET. A device with a channel of small cross-sectional area will exhibit a high $r_{DS(on)}$ and a low I_{DSS}. Thus a FET with high I_{DSS} should be chosen where design requirements indicate the need for a low $r_{DS(on)}$.



N-Channel JFET Output Characteristic Enlarged Around $V_{DS} = 0$
Figure 2

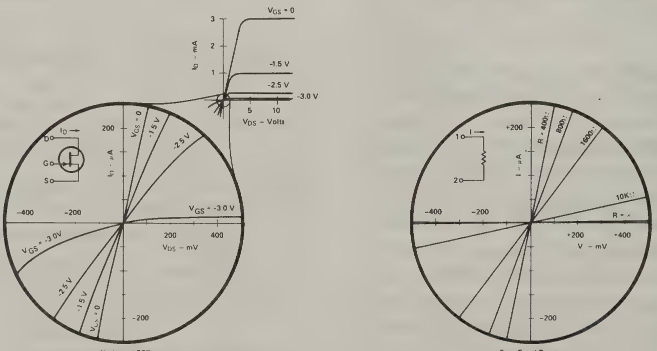
Figure 3 extends the r_{ds} characteristics of a FET to a comparison with the performance of 4 fixed resistors. Note the pronounced similarity between the two types of devices.

Typical r_{DS} curves for several Siliconix N-channel JFETs are plotted in Figure 4.(4) The graphs are useful in estimating r_{DS} values at any given value of V_{GS}. All quantities given in Figure 4 are for typical units, so some variation should be expected for the full range of production devices. It is therefor deisrable to convert Figure 4 to a normalized plot. This has been done in Figure 5. The resistance is normalized to its specific value at $V_{GS} = 0$ V. The dynamic range of r_{DS} is shown as greater than 100:1, although for best control of r_{DS} a range of 10:1 is normally used.



Incremental Drain-Source Resistance for Typical N-Channel FETs
Figure 4

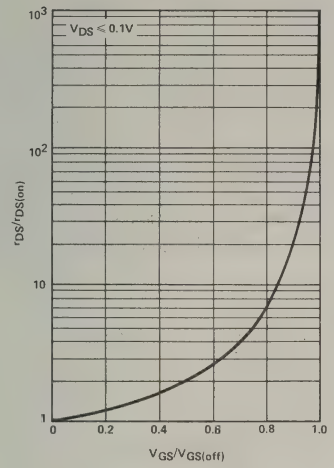
Siliconix offers a family of FETs specifically intended for use as voltage-controlled resistors. The devices are available in both N-Channel and P-Channel configurations (Figures 6A and 6B) and have $r_{DS(on)}$ values ranging from 20 Ω to 4,000 Ω (Figure 7).



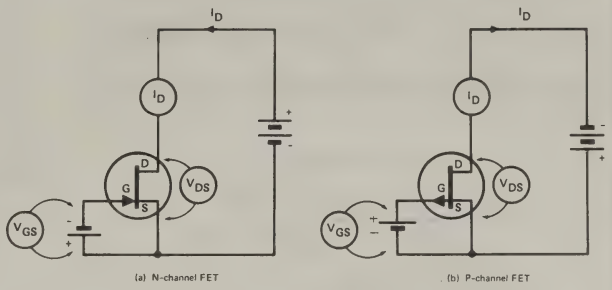
N-channel FET

Four Fixed Resistors

Comparison of FET and Resistor Characteristics
Figure 3



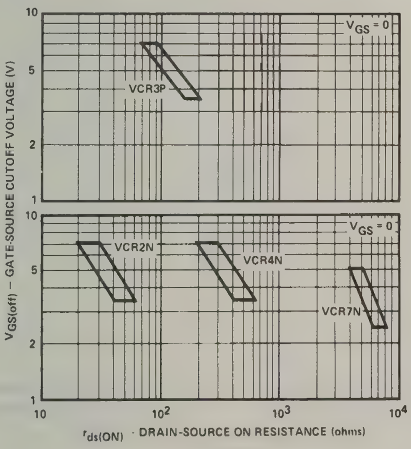
Normalized r_{ds} Data
Figure 5



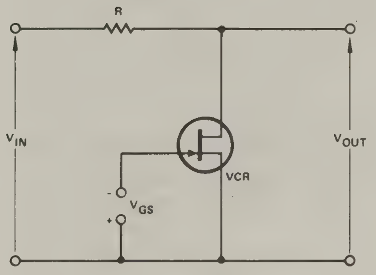
(a) N-channel FET

(b) P-channel FET

Circuit Arrangement for Both an N and P Channel FET
Figure 6



$r_{ds(on)}$ (Drain-Source Resistance at $V_{DS} = V_{GS} = 0$)
Varies as an Inverse Function of $V_{GS(off)}$
Figure 7



Simple Attenuator Circuit
Figure 8

Applications for VCRs

The FET is ideal for use as a voltage-controlled resistor in applications requiring high reliability, minimum component size, and circuit simplicity. The FET VCR will conveniently replace numerous elements of conventional resistance control systems, such as servomotors, potentiometers, idler pulleys, and associated linkage. FET power consumption is minimal, packages are very small, and cost comparisons with conventional control schemes are most favorable.

A simple application of a FET VCR is shown in Figure 8, the circuit for a voltage divider attenuator.(5)

The output voltage is

$$v_{OUT} = \frac{V_{in}\, r_{DS}}{R + r_{DS}} \qquad (1)$$

It is assumed that the output voltage is not so large as to push the VCR out of the linear resistance region, and that the r_{DS} is not shunted by the load.

The lowest value which v_{OUT} can assume is

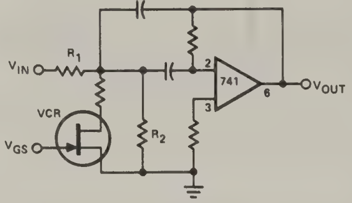
$$v_{OUT(min)} = \frac{V_{in}\, r_{DS(on)}}{R + r_{DS(on)}} \qquad (2)$$

The highest value is

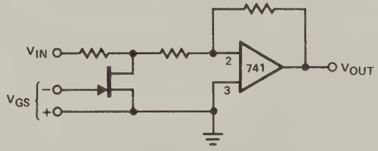
$$v_{OUT(max)} = v_{in} \qquad (3)$$

since r_{DS} can be extremeley large.

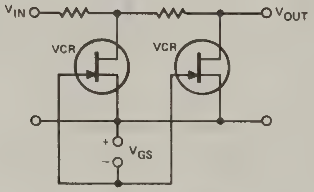
A number of other FET VCR applications are shown in Figures 9-16.



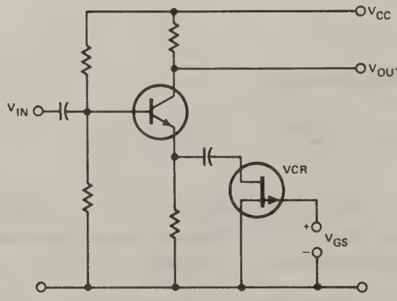
Voltage-Tuned Filter Octave Range with Lowest Frequency at JFET $V_{GS(off)}$ and Tuned by R_2. Upper Frequency is Controlled by R_1
Figure 9



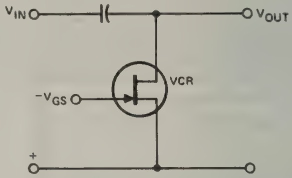
Electronic Gain Control
Figure 10



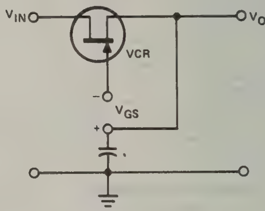
Cascaded VCR Attenuator
Figure 11



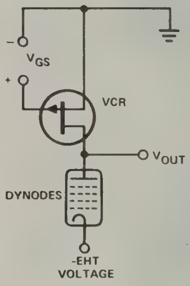
Wide Dynamic Range AGC Circuit. No Gain through FET with Distortion Proportional to Input Signal Level
Figure 12



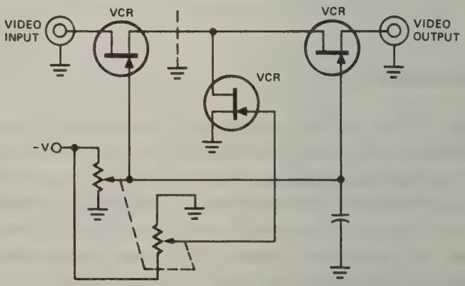
VCR Phase Advance Circuit
Figure 13



VCR Phase Retard Circuit
Figure 14



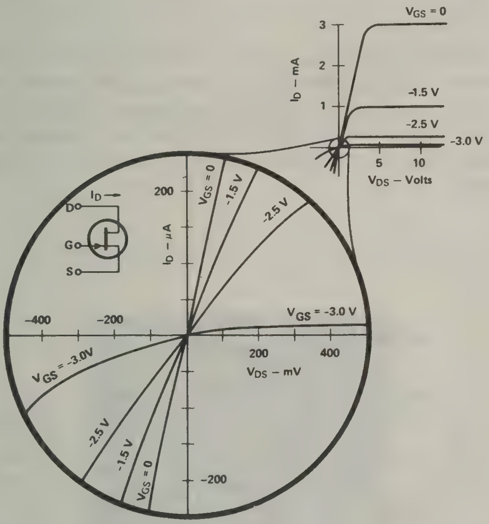
P-Channel VCR Photomultiplier Load. Required Low Photomultiplier Anode Current (Usually < 1 μA) Implies that VCR will Always Perform in Linear Region Near Origin
Figure 15



Voltage Controlled Variable Gain Amplifier. The Tee Attenuator Provides for Optimum Dynamic Linear Range Attenuation
Figure 16

Signal Distortion: Causes

Figure 17A repeats the FET output characteristic curves of Figure 2, to show that the bias lines bend down as V_{DS} increases in a positive direction toward the pinch-off voltage of the FET. The bending of the bias lines results in a change in r_{DS}, and hence the distortion encountered in VCR circuits; note that the distortion occurs in both the first and third quadrants. Distortion results because the channel depletion layer increases as V_{DS} reduces the drain current, so that a pinch-off condition is reached when $V_{DS} = V_{GS} - V_{GS(off)}$. Figure 17B shows how the current has an opposite effect in the third quadrant, rising negatively with an increasingly negative V_{DS}. This is due to the forward conduction of the gate-to-channel junction when the drain signal exceeds the negative gate bias voltage.



N-Channel JFET Output Characteristic Enlarged Around $V_{DS} = 0$
Figure 17A

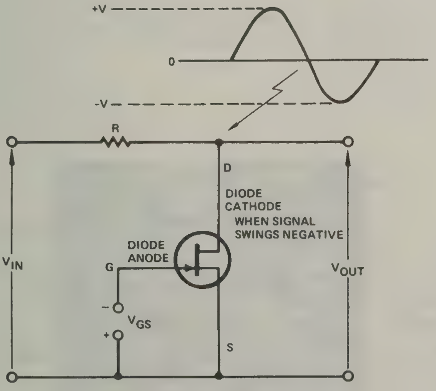


Figure 17B

Reducing Signal Distortion

The majority of VCR applications require that signal distortion be kept to a minimum. Also, numerous applications require large signal handling capability. A simple feedback technique may be used to reduce distortion while permitting large signal handling capability; a small amount of drain signal is coupled to the gate through a resistor divider network, as shown in Figure 18.

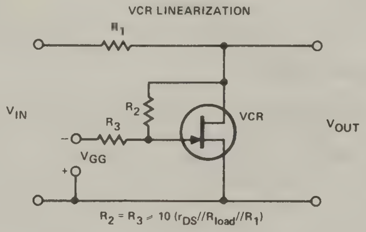


Figure 18

The application of a part of the positive drain signal to the gate causes the channel depletion layer to decrease, with a corresponding increase in drain current. Increasing the drain current for a given drain voltage tends to linearize the V_{GS} bias curves. On the negative half-cycle, a small negative voltage is coupled to the gate to reduce the amount of drain-gate forward bias. This in turn reduces the drain current and linearizes the bias lines. Now the channel resistance is dependent on the DC gate control voltage and not on the drain signal, unless the $V_{DS} = V_{GS} - V_{GS(off)}$ locus is approached. Resistors R_2 and R_3 in Figure 18 couple the drain signal to the gate; the resistor values are equal, so that symmetrical voltage-current characteristics are produced in both quadrants. The resistors must be sufficiently large to provide minimum loading to the circuit:

$$R_2 = R_3 \geqslant 10\ [R_1 \,||\, r_{ds}(\max) \,||\, R_L] \qquad (4)$$

Typically, 470K Ω resistors will work well for most applications. R_1 is selected so that the ratio of $r_{DS(on)} || R_L$ to $[(r_{DS(on)} || R_L) + R_1]$ gives the desired output voltage, or:

$$e_o = e_i \frac{r_{DS(on)} \,||\, R_L}{(r_{DS(on)} \,||\, R_L) + R_1} \qquad (5)$$

The feedback technique used in Figure 18 requires that the gate control voltage, V_{GG}, be twice as large as V_{GS} in Figure 17B for the same r_{DS} value. Use of a floating supply between the resistor junction and the FET gate will overcome this problem. The circuit is shown in Figure 19, and allows the gate control voltage to be the same value as that voltage used without a feedback circuit, while preserving the advantages to be gained through the feedback technique.

Appendix A to this Application Note is an analytical approximation of VCR FET distortion characteristics, both calculated and measured.

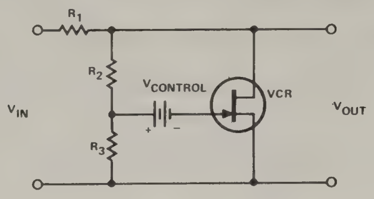


Figure 19

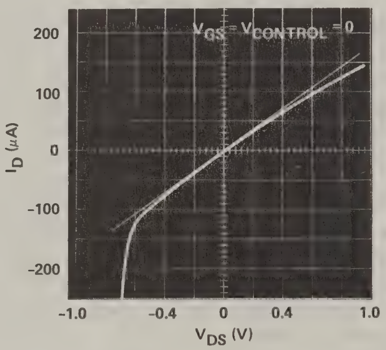
Experimental Results

Figures 20 through 23 show low voltage output characteristic curves for a typical Siliconix N-Channel voltage-controlled resistor, VCR7N. Bias conditions are shown both with and without feedback. Figure 20 shows a two-volt peak-to-peak signal on the $V_{GS} = 0$ V bias curve, with the VCR operating in the first and third quadrants. The VCR is operated without feedback.

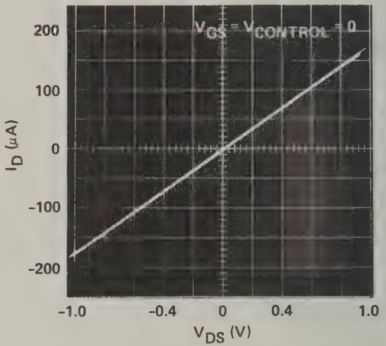
The forward-biased gate-drain PN junction may be seen at approximately −0.6 V, and bending of the bias curve is apparent in the third quadrant. The photo also demonstrates the comparison between a fixed resistor (the linear line superimposed on the bias curve) and the distortion apparent in the VCR without feedback compensation; the VCR signal is unusable with the indicated amount of distortion.

In Figure 21, the same VCR7N FET is shown operating with the addition of the feedback resistors. Distortion has been reduced to less than 0.5%, and the characteristics of the VCR are now closely comparable to those of a fixed resistor.

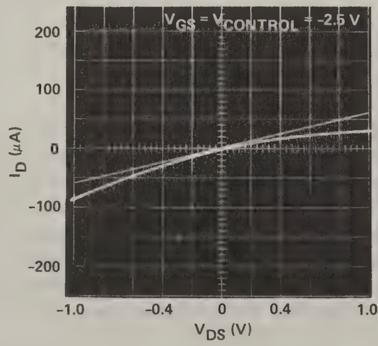
In Figures 22 and 23, the same VCR FET characteristics are shown, with V_{GS} adjusted for higher r_{DS}. No feedback network is employed in Figure 22, and measured distortion is greater than 8%. In Figure 23, the feedback resistors have been added and distortion has been reduced to less than 0.5%.



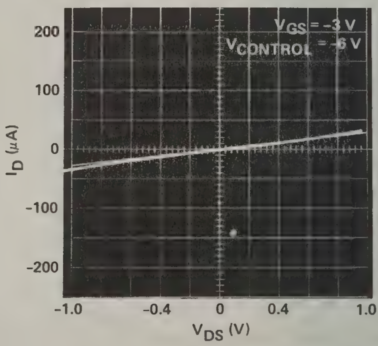
VCR7N with No Feedback
Figure 20



VCR7N with Feedback
Figure 21

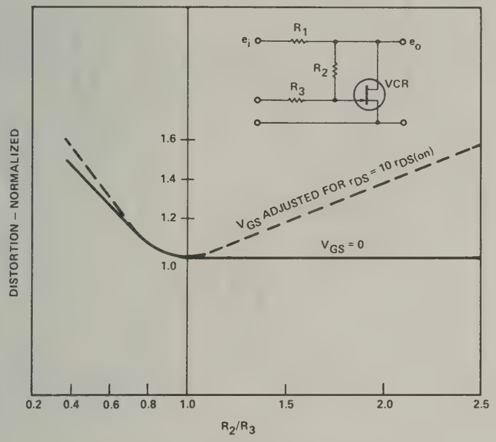


VCR7N with No Feedback
Figure 22



VCR7N with Feedback
Figure 23

Some degree of non-linearity will be experienced in both the first and third quadrants as V_{GS} approaches the FET cut-off voltage. For this reason, it is important that the feedback resistors be of equal value so that the non-linearities likewise will be equal in both quadrants. Figure 24 shows a curve of distortion vs R_2/R_3, in both quadrants.



Distortion vs R_2/R_3
Figure 24

Distortion resulting from changes in temperature are also minimized by the feedback resistor technique. r_{DS} will change with temperature in an inverse manner to the behavior of FET drain current. Table I presents the result of VCR laboratory performance tests of distortion vs temperature. The VCR7N again was employed. Signal level was 2 V peak-to-peak.

Table I

Temperature (°C)	Without Feedback		With Feedback	
	$r_{DS} = r_{DS(on)}$	$r_{DS} = 10\ r_{DS(on)}$	$r_{DS} = r_{DS(on)}$	$r_{DS} = 10\ r_{DS(on)}$
+125	>13%	>6%	<0.5%	<0.5%
+ 25	>10%	>5%	<0.5%	<0.5%
− 55	3.9%	3.2%	<0.5%	<0.5%

SUMMARY

This Application Note has presented a brief description of the use of junction field-effect transistors as voltage-controlled resistors, including details of operation, characteristics, limitations, and applications. The VCR is capable of operation as a symmetrical resistor with no DC bias voltage in the signal loop, an ideal characteristic for many applications.

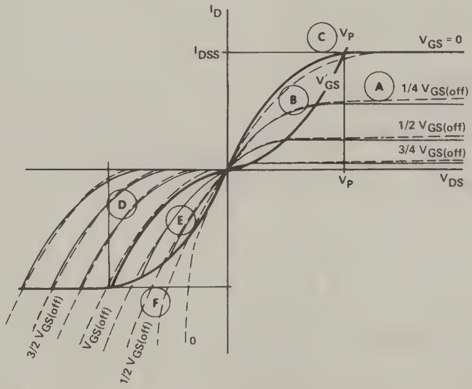
Where large signal-handling capability and minimum distortion are system requirements, the feedback neutralization technique for VCRs is an important tool in achieving either or both ends.

It has also been shown that FETs with high pinch-off voltage require larger drain-to-source voltages to produce drain current saturation. Therefore, FETs with high $V_{GS(off)}$ will have a larger dynamic range in terms of applied signal amplitude, while maintaining a linear resistance. It is advantageous to select FETs with high $V_{GS(off)}$ (compatible with the desired r_{DS} value) if large signal levels are to be encountered.

APPENDIX A — From proceedings of the IEEE, October, 1968, pp. 1718-1719.

Abstract — An analytical approximation of FET characteristics for positive and negative voltages is presented. The distortion in an application as a controlled attenuator is calculated, and a method of reducing distortion by a factor of more than 50 is described.

Controlled resistors are used in oscillators, controlled amplifiers, and attenuators.(6,7) The possible control range is much larger for field-effect transistors (FET) than for other elements with comparable time constants (e.g., diodes). The signal-to-noise ratio is considerably improved.



Comparison Between Mathematical Approximation of FET Characacteristics (Solid Lines) and Measured Curves (Broken Lines) for a Typical N-Channel JFET
Figure 25

Figure 25 shows idealized and real FET characteristics. In region A (above pinch-off) I_D is independent of V_{DS}:(8)

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (1)$$

Region B, where $V_{DS} < (V_{GS} - V_P)$, is the so-called triode region. (In the following discussion all the signs (+, −) will be valid for N-Channel FETs.) The characteristics can be approximated by a quadratic function, of which the maximum and a second point (the origin) are known. The approximation is

$$I_D = I_{DSS}\left[\left(1-\frac{V_{GS}}{V_P}\right)^2 - \left(1-\frac{V_{GS}-V_{DS}}{V_P}\right)^2\right]$$

$$= \frac{2I_{DSS}}{(V_P)^2}\; V_{DS}\left(V_{GS}-V_P-\frac{V_{DS}}{2}\right) \tag{2}$$

This is the same function that can be found by a simple analysis based on semiconductor theory. The less negative of the two voltages across the junction (V_{GS}, V_{GD}) controls the channel conductance. Under the condition that the FET is symmetrical (drain and source interchangeable), the following consideration is true. If V_{GD} were the controlling voltage and $V_{DS} < 0$, $I_D < 0$, then the characteristics would be the same as in the first quadrant:

$$-I_D = -\frac{2I_{DSS}}{V^2_P}\; V_{DS}\left(V_{GD}-V_P+\frac{V_{DS}}{2}\right) \tag{3}$$

Since the controlling voltage for both regions (B and E) is V_{GS},

$$V_{GD} = V_{GS} - V_{DS} \tag{4}$$

Substituting (4) into (3), we get (2); the same approximation can be used in B and E. The limits of region E where (2) is valid are $V_{GD} = 0$ and $V_{GD} = V_P$. The characteristics in region D can be found from (1) with the same consideration:

$$I_D = -I_{DSS}\left(1-\frac{V_{GS}-V_{DS}}{V_P}\right)^2 \tag{5}$$

The mathematical approximation is compared with the measured characteristic in Figure 25. In the regions C and F the junction is forward biased. The characteristics are dependent on the internal resistance of the gate voltage source since gate current flows.

The FET as a controlled resistor works in region B and E. The higher the resistance, the more non-linear are the characteristics. For most applications this is undesirable. Based on the simple approximation (2), the relation between distortion, control range, and maximum to minimum attenuation will be described for a simple voltage divider [Figure 26(a)]. Most applications can be based on this simple example. The conductance in any point of region B or E is

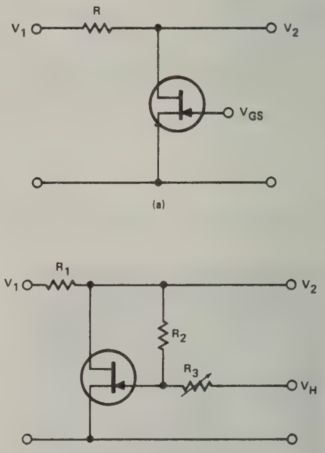
$$G_{DS} = \frac{I_D}{V_{DS}} = -\frac{2I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$$

$$-\frac{I_{DSS}}{(V_P)^2}\; V_{DS} = g_{DS} + \frac{g_{DSS}V_{DS}}{2V_P} \tag{6}$$

where g_{DS} is the differential conductance at the origin; when $V_{GS} = 0$, then $g_{DS} = g_{DSS}$. The attenuation for the circuit of Figure 26(a) is

$$\frac{V_2}{V_1} = \frac{1}{1+Rg_{DS}}$$

$$= \left[1+Rg_{DS} + \frac{Rg_{DSS}\,V_1}{2V_P\left(1+Rg_{DS}+\frac{2Rg_{DS}\,V_1}{2V_P\,(1+Rg_{DS})}\right)}\right]^{-1} \tag{7}$$



(a)

(b)

(a) Controlled JFET Attenuator. (b) Controlled Attenuator with "Feedback" Making Characteristics Linear and Symmetrical
Figure 26

To reduce (7) to a more tractable form, the following inequality is introduced:

$$\frac{V_1\,Rg_{DSS}}{2V_P\,[1+Rg_{DS}]^2} \ll 1$$

so that (7) can now be approximated by the expansion

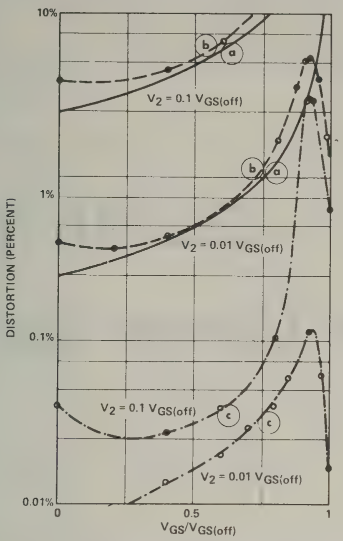
$$V_2 = \frac{V_1}{1+g_{DS}R}\left(1-\frac{Rg_{DS}\,V_1}{2V_P\,[1+Rg_{DS}]^2}+\ldots\right) \tag{8}$$

Only the second harmonic will be considered for the distortion since the third is much smaller. For small distortion ($d \ll 1$ and $Rg_{DSS} \gg 1$),

$$d = \frac{V_1\,Rg_{DSS}}{4\,|V_P|\;[1+Rg_{DS}]^2} \tag{9}$$

If V_2 is held constant,

$$d = \frac{V_2\,Rg_{DS}}{4\,|V_P|\;[1+Rg_{DS}]} \approx \frac{V_2}{4\,|V_P-V_{GS}|} \tag{10}$$



Distortion as a Function of $V_{GS}/V_{GS(off)}$ for Two Different $V_2/V_{GS(off)}$. (a) Theoretical for Figure 26(a). (b) Measured with Circuit of Figure 26(a). (c) Measured with Circuit of Figure 26(b)

Figure 27

Figure 27 shows a comparison of measured and calculated distortion. If V_{GS} approaches V_P, the above restrictions are violated; the expression for the distortion can no longer be applied. If $V_{DS} < 0$, $V_{GS} = 0$, then the FET works in region F; the distortion will be higher than predicted. From (10) we get for a prescribed maximum distortion a maximum amplitude as a function of V_{GS}:

$$V_{2max} = 4d_{max}\,|V_P - V_{GS}| \tag{11}$$

For a given d_{max} and V_{2max} the ratio of minimum to maximum attenuation is.

$$\frac{A_{min}}{A_{max}} = m = \frac{1 + Rg_{DSS}}{1 + Rg_{DSS}\,\dfrac{V_{2max}}{4d_{max}\,|V_P|}} \approx \frac{4d_{max}\,|V_P|}{V_{2max}} \tag{12}$$

valid only for $m > 1$. Note that the maximum distortion is reached only for minimum attenuation. Examples:

$d_{max} = 10$ percent $V_{2max} = 0.001\ V_P$ $m = 400$

$d_{max} = 1$ percent $V_{2max} = 0.01\ V_P$ $m = 4$

Although these relations are only first-order approximations, they give a good estimate of FET attenuator characteristics. The maximum amplitude is proportional to V_P. FETs with high V_P are desirable for attenuator applications. Unfortunately, the majority of commercially available FETs are made with low V_P for use in amplifiers.

There are several means of reducing distortion. By connecting two identical FETs in antiparallel or antiseries, nonlinearities can be cancelled out to a certain extent. A better linearization is possible by using one FET with "feedback". It has been shown above that the characteristics would be symmetrical if V_{GD} were the control voltage in the third quadrant. By adding 0.5 V_{DS} to the control voltage, the two voltage V_{GS} and V_{GD} interchange when V_{DS} changes sign:

$$\begin{aligned} V_{GS} &= V_H + 0.5\ V_{DS} \\ V_{GD} &= V_H - 0.5\ V_{DS} \end{aligned} \tag{13}$$

then (13) used in (2) gives

$$I_D = \frac{2I_{DSS}}{V^2_P}\ V_{DS}\,(V_H - V_P) \tag{14}$$

The resulting characteristic is linear and symmetrical in B and E. The improvement in distortion performance can be seen in Figure 27. A distortion of 12 percent for $V_2 = 0.1$ V_P at $V_{GS} = 0.8\ V_P$ is reduced through linearization to 0.1 percent. Figure 26(b) shows a possible circuit. The frequency range of the controlled signal must be much higher than that of the controlling signal V_H to keep the direct interference of V_H on V_2 small. R_3 is set for minimum distortion. If V_2 and V_H are in the same frequency range, a high impedance amplifier must be used. V_2 is at the input; the output is connected to the FET gate. The amplification is approximately 0.5 (adjustable). The control voltage is introduced through a second input so that no direct interference with V_2 occurs.

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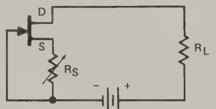
Siliconix

DESIGN IDEA

The FET Constant Current Source

INTRODUCTION

The combination of low associated operating voltage and high output impedance make the FET attractive as a constant current source. An adjustable current source may be built with a FET, a variable resistor and a small battery, Figure 1. For good thermal stability, the FET should be biased near the zero T.C. point.[1]



Field-Effect Transistor Current Source
Figure 1

Whenever the FET is operated in the saturated region, its output conductance is very low. This occurs whenever the drain-source voltage V_{DS} is significantly greater than the cut-off voltage $V_{GS(off)}$. The FET may be biased to operate as a constant current source at any current below its saturation current I_{DSS}.

For a given device where I_{DSS} and $V_{GS(off)}$ are known, the approximate V_{GS} required for a given I_D is

$$V_{GS} = V_{GS(off)} \left[1 - \left(\frac{I_D}{I_{DSS}}\right)^{1/k}\right] \tag{1}$$

where k can vary from 1.7 to 2.0, depending upon device geometry. The series resistor R_S required between source and gate is

$$R_S = \frac{V_{GS}}{I_D} \tag{2}$$

A change in supply voltage, or change in load impedance, will change I_D by only a small factor because of the low output conductance g_{oss}.

$$\Delta I_D = \Delta V_{DS} g_{oss} \tag{3}$$

The value of g_{oss} is an important consideration in the accuracy of a constant current source. As g_{oss} may range from less than 1 μmho to more than 50 μmho according to the FET type, the dynamic impedance can be greater than 1 megohm to less than 20K. This corresponds to a current stability range of 1 μA to 50 μA per volt. The value of g_{oss} depends also on the operating point, being highest at I_{DSS} and at low V_{DS}. Output conductance g_{oss} decreases approximately linearly with I_D, becoming less as the FET is biased toward cut-off. The relationship is

$$\frac{I_D}{I_{DSS}} = \frac{g_{oss}}{g'_{oss}} \tag{4}$$

where

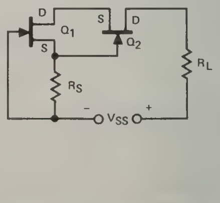
$$g_{oss} = g'_{oss} \tag{5}$$

when

$$V_{GS} = 0 \tag{6}$$

So as $V_{GS} \rightarrow V_{GS(off)}$, $g_{oss} \rightarrow$ zero. For best regulation, I_D must be considerably less than I_{DSS}.

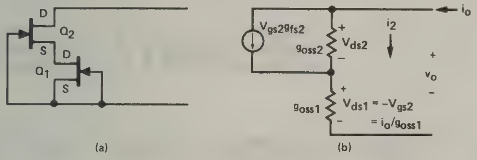
It is possible to achieve much lower g_{oss} per unit I_D by cascading two FETs as shown in Figure 2.



Cascade FET Current Source
Figure 2

Now, I_D is regulated by Q_1 and $V_{DS1} = -V_{GS2}$. The d-c value of I_D is controlled by R_S and Q_1. However, Q_1 and Q_2 both affect current stability. The circuit output conductance is derived as follows:

Figure 2 is redrawn in Figure 3 for the condition $V_{GS1} = 0$.



(a) (b)

Figure 3

$$i_o = i_2 + v_{gs2}g_{fs2} = v_{ds2}g_{oss2} - i_o \frac{g_{fs2}}{g_{oss1}} \qquad (7)$$

$$i_o = \frac{v_{ds2}g_{oss2}g_{oss1}}{g_{oss1} + g_{fs2}} \qquad (8)$$

$$v_o = v_{ds1} + v_{ds2} = v_{ds2} + \frac{i_o}{g_{oss1}} \qquad (9)$$

$$v_o = v_{ds2}\frac{g_{oss1} + g_{oss2} + g_{fs2}}{g_{oss1} + g_{fs2}} \qquad (10)$$

$$g_o = \frac{i_o}{v_o} = \frac{g_{oss1}g_{oss2}}{g_{oss1} + g_{oss2} + g_{fs2}} \qquad (11)$$

If $g_{oss1} = g_{oss2}$ (12)

$$g_o = \frac{g_{oss}}{2 + g_{fs}/g_{oss}} \qquad (13)$$

When

$R_S \neq 0$ as in Figure 2 (14)

$$g_o = \frac{g_{oss}^2}{2g_{oss} + g_{fs} + R_S\left(g_{fs}^2 + g_{oss}g_{fs} + g_{oss}^2\right)} \qquad (15)$$

$$\approx \frac{g_{oss}^2}{g_{fs}\left(1 + R_S g_{fs}\right)} \qquad (16)$$

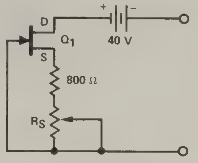
In either case ($R_S = 0$ or $R_S \neq 0$), the circuit output conductance is considerably less than the g_{oss} of a single FET.

In designing any cascaded FET current source, both FETs must be operated with adequate drain-gate voltage V_{DG}. That is,

$$V_{DG} > V_{GS(off)}, \text{ preferably } V_{DG} > 2\,V_{GS(off)} \qquad (17)$$

If $V_{DG} < 2\,V_{GS(off)}$, the g_{oss} will be significantly increased, and circuit g_o will deteriorate. For example: A 2N4340 has typical $g_{oss} = 4$ µmho at $V_{DS} = -20$ V and $V_{GS} = 0$. At $V_{DS} \approx -V_{GS(off)} = 2$ V, $g_{oss} \approx 100$ µmho.

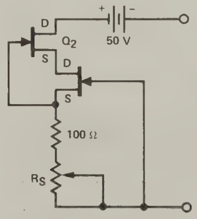
The best FETs for current sources are those having long gates and consequently very low g_{oss}. The Siliconix 2N4869 exhibits typical $g_{oss} = 1$ µmho at $V_{DS} = 20$ V. A single 2N4869 in the circuit of Figure 4 will yield a current source adjustable from 5 µA to 1 mA with internal impedance greater than 2 megohms.



$R_S = 1M\Omega$, 2W

Adjustable Current Source
Figure 4

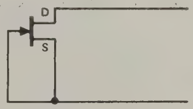
The cascade circuit of Figure 5 provides a current adjustable from 2 µA to 1 mA with internal resistance greater than 10 megohms.



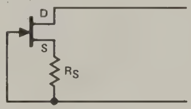
$Q_1 = 2N4340$
$Q_2 = 2N4341$
$R_S = 1M\Omega$, 2W

Cascade FET Current Source
Figure 5

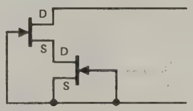
For each circuit discussed, g_{oss} is represented by the following equations:



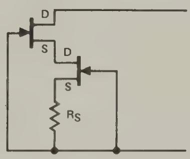
$$g_o = g_{oss}$$



$$g_o \approx \frac{g_{oss}}{1 + R_S g_{fs}}$$



$$g_o \approx \frac{g_{oss}^2}{g_{fs}}$$



$$g_o \approx \frac{g_{oss}^2}{g_{fs}\left(1 + R_S g_{fs}\right)}$$

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Siliconix

DESIGN IDEA

Wideband UHF Amplifier with High-Performance FETs

Ed Oxner

INTRODUCTION

A new freedom in UHF amplifier design is possible with high-performance "Super FETs" such as the Siliconix U310 Junction FET. Typical advantages include a closely-matched 75 ohm input for extremely low return loss in cable systems, and high spurious response rejection with the 3rd order IM intercept measured at +29 dB.(1)

Additionally, the high common-gate forward transconductance of the U310 (20,000 μmho maximum) makes it possible to design an amplifier with wide bandwidth and good gain, since the figure of merit (g_m/C) of the FET is 2.35 x 10^9 typical – higher than any other known UHF Junction FET.

The amplifier circuit in Figure 1 is designed for 225 MHz center frequency, 1 dB bandwidth of 50 MHz, low input VSWR in a 75-ohm system, and 24 dB gain. Three stages of U310 FETs are used, in a straight forward design.

Typical parameters are taken from the U310 data sheet:

Forward Transconductance		14 mmhos
Input Admittance at 225 MHz	g_{igs}	13 mmhos
	b_{igs}	4 mmhos
Output Admittance at 225 MHz	g_{ogs}	0.27 mmhos
	b_{ogs}	2.6 mmhos

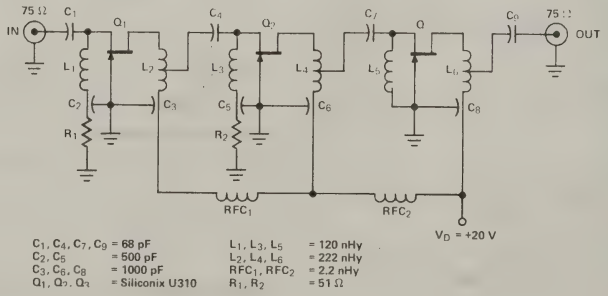


Figure 1

Input match is simplified because the FET input (real) impedance is nearly 77 ohms. A coupling capacitor is used in the amplifier, rather than a tuned circuit, and thus the values may be determined:

$$R_s\sqrt{\frac{R_{ig}}{R_s}-1} = X_s = 75\sqrt{\frac{77}{75}-1} = 11.85\ \Omega$$

$$C_s = \frac{1}{\omega X_s} \approx 68\text{ pF}$$

$$X_P = \frac{R_s R_p}{X_s} = \frac{75 \times 77}{11.85} = 488\ \Omega$$

$$C_P = 1.47\text{ pF}$$

$$C_T = 4.4\text{ pF } (C_T = C_P + C_{igs})$$

$$L_s = \frac{1}{\omega^2 C_T} = 120\text{ nHy}$$

Figure 2 shows that the measured input VSWR in the 75-ohm system indicated an available bandwidth considerably greater than that required for the amplifier design criteria.

Three cascaded synchronous single-tuned stages are used to achieve the desired gain, and thus stage bandwidth and Q are determined:(2)

$$\frac{B/W}{f} = \frac{1}{Q}\sqrt{\left(\frac{E_o}{E}\right)^2 - 1}$$

where:

$$\frac{\text{Bandwidth of 3 Stages}^{(3)}}{\text{Bandwidth of 1 Stage}} = \sqrt{2^{1/3} - 1}$$

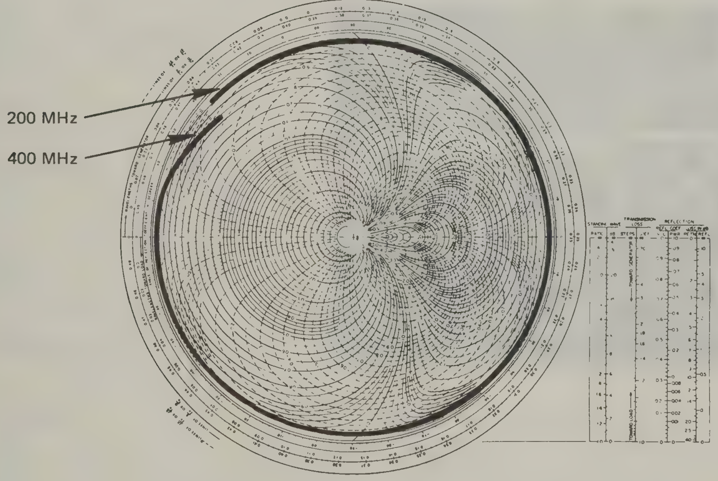
and

$$\left(\frac{E_o}{E}\right) = 1.122\ (1\text{ dB})$$

giving

B/W (1 dB) = 98 MHz

Q = 1.15



Blanchard Chart (Inverted Circle Impedance Chart)
Figure 2

With a FET output impedance of 3700 ohms shunted by approximately 2.5 pF (with 0.5 pF allowed for stray capacitance), the total parallel resistance necessary to obtain the desired bandwidth is:

$$Q = \omega C R_t$$

$$R_t = \frac{1.15}{1.415 \times 10^9 \times 2.5 \times 10^{-12}} = 330\ \Omega$$

The tank circuit impedance appearing in shunt with the FET, is therefore calculated to be about 365 ohms. From this, the inductance is:

$$L = \frac{R}{\omega Q} = \frac{365}{\omega 1.15} = 222 \text{ nHy}$$

with a turns ratio of 2.3:1 to match to 75 ohms. Since each stage is designed for 75 ohm input and output, three cascaded stages complete the amplifier design.

The computed voltage gain per stage is approximately $g_{fs}\ R_{t/n}$ or 2.22 (7 dB). Measured gain for all three stages is 24 dB. The U310 FET in the final stage operates at I_{DSS}, and thus accounts for the higher measured gain. The gain/bandwidth response of the amplifier is shown in Figure 3.

The 3rd order spurious intercept point is plotted graphically in Figure 4.(4) The importance of a high intercept point becomes apparent in a crowded high-level area of the spectrum where signal purity is of utmost priority.

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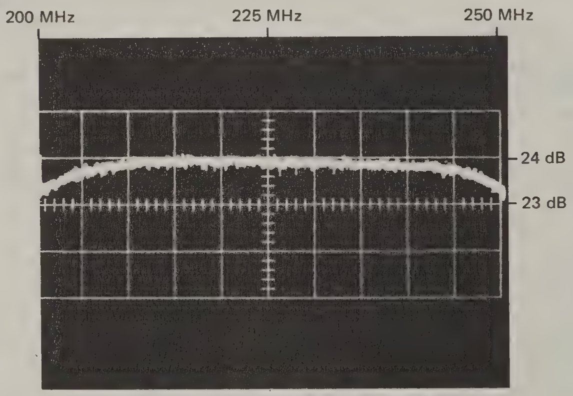


Figure 3

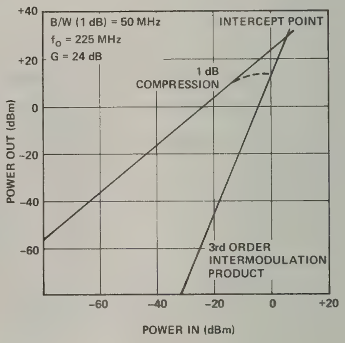


Figure 4

DESIGN IDEA

High-Performance FETs In Low-Noise VHF Oscillators

Ed Oxner

Most communications receivers are limited in their dynamic range because of saturation in the early stages of RF amplifiers or mixers. However, some receiver designs are available which overcome this limitation by using parametric amplifiers and converters to achieve spectacular increases in dynamic range. There still remain certain limitations in dynamic range which cannot be remedied by parametric devices. In these cases, the problem lies in the heterodyning of noise sidebands which appear on the receiver local oscillator, entering the passband through strong interfering signals.

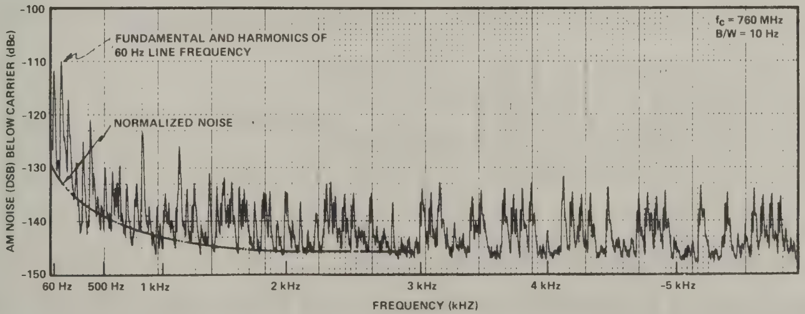
Common Types of Noise

Although noise is often difficult to characterize because of its random or nondeterministic nature, it is possible to differentiate various forms of noise through an understanding of the Gaussian distribution of noise about an RF carrier. Briefly stated, the three major forms of noise are (1) low-frequency noise (1/f); (2) thermal noise (4kTRB); and "shot" noise (i_n). Further, these types of noise can be identified from their relationship to the main RF carrier. For example, low-frequency noise predominates very close to the carrier, and falls to insignificant levels when it is displaced more than 250 Hz from the carrier. Low-frequency noise is associated with surface contamination and other irregularities, such as gate current leakage.

Thermal noise plays the predominant role in the region from the 1/f decay point to approximately 20 kHz from the carrier, and is commonly associated with equivalent resistance where the rms value of noise voltage of the Thevenin generator becomes the classic $(4kTBR)^{1/2}$. Noise appearing beyond the 20 kHz is known as Shot noise, and is directly attributable to noise current. Because of the typically uniform distribution of shot noise it is also referred to as "white noise."

Origins of Oscillator AM Noise

Although an oscillator tends to produce a wave that is nearly sinusoidal, there are other fluctuations present. When the energy in the frequency domain close to the carrier is observed on a spectrum analyzer, noise appears as a modulation phenomenon. This observation would be greatly enhanced if the noise contribution was coherent and consisted of discrete sideband frequencies. Without a doubt, the major component of AM noise is the contribution of low-frequency noise (1/f). Both thermal and shot noise are relatively insignificant segments of AM noise when compared to 1/f. A graph of AM noise vs frequency removed is shown in Figure 1.

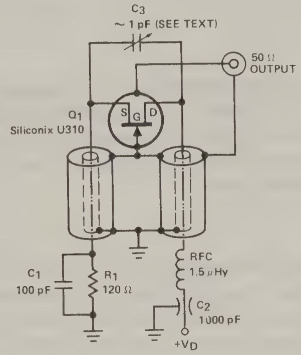


AM Noise vs Frequency Removed from the Carrier
Figure 1

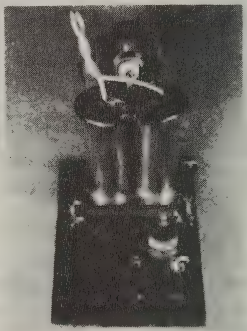
Design of a VHF Oscillator

The important design considerations for best oscillator performance include using a FET with high forward transconductance, maintaining the gate at ground potential, and keeping a high unloaded tank Q. The high transconductance is necessary to reduce the effective noise resistance. The grounded gate reduces the noise voltage contributions to those of the gate leakage current and the series gate resistance. The high tank circuit Q serves as an effective filter for the sideband noise energy.

The oscillator design is somewhat extraordinary for a circuit employing a FET. The FET chosen was the Siliconix U310, which has a forward transconductance value higher than 18 mmho at zero bias ($V_{GS} = 0$). The oscillator basically consists of two coaxial resonators, one for the FET source and the other for the drain. Oscillation is established by capacity coupling between the two resonators; output coupling is derived from the magnetic coupling which exists at the open ends of the resonators. Optimum resonator Q is achieved by designing the coaxial resonators for a characteristic impedance of 75 ohms. The oscillator circuit is shown in Figure 2, and construction details are shown in Figure 3.



Oscillator Circuit
Figure 2



Oscillator Construction Details
Figure 3

The technique to establish the proper resonator length for the desired frequency is somewhat tricky, and requires a first-order approximation of the anticipated capacitive fringing which derives from both the FET and the feedback network. A short circuited coaxial transmission line is theoretically resonant at a quarter-wave length of the resonating frequency, except for the effects of fringe field capacitance. At resonance

$$X_L = X_C \tag{1}$$

If the fringe capacitance is known, X_C can be calculated as

$$X_C = \frac{1}{\omega C} \tag{2}$$

From this, the resonator length can be determined as

$$X_C = \tan \beta \ell \tag{3}$$

In making these calculations, a Smith chart is invaluable, as is shown in the following illustration:

Frequency of oscillation = 760 MHz
FET b_{igs} (from data sheet) = 16 mmho
Capacitance from b_{igs} $C_{gs} = 3.4$ pF
Allow for stray capacitance and
the feedback network $C_s = 1.5$ pF
4.9 pF

Thus $X_C = j\ 0.57$ (normalized to 75 Ω)

Locate 0.57 on the Smith chart. The wavelength toward the load = 0.081 λ. Since a wavelength at 760 MHz is 39.5 cm., then the resonator cavity length is simply

$$39.5 \times 0.081 = 3.20 \text{ cm } (1.26 \text{ inches}) \tag{4}$$

In the completed FET coaxial oscillator circuit, the output coupling loop consists of a single turn made fast to the cavity by the BNC flange and the FET itself. Although the feedback network appears somewhat crude, it can be replaced by a small trimmer capacitor for similar operation.

Conclusions

Measured performance of the oscillator is shown in Table IA; AM noise measurements in a 10 Hz bandwidth are shown in Table IB.

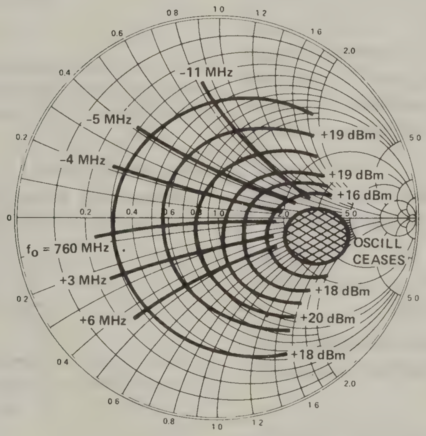
TABLE IA
Oscillator Measured Performance @ 25°C

V_{DD}(V)	+10	+15	+20	+25
I_D (mA)	15	16.2	18.2	21
P_{out} (dBm)	+6.6	+15.2	+18.3	+20
Frequency (MHz)	725	742.7	754.7	762.9

TABLE IB
AM Noise Measurement

Frequency Displaced From Carrier	dBc
50 Hz	-130
500 Hz	-139
1 kHz	-143.5
5 kHz	-146

The Reike diagram shown in Figure 4 makes possible the accurate prediction of expected power output and operating frequency with the oscillator feeding directly into a mismatched load. Expansion of the Reike diagram to show frequency vs transmission line length (in degrees) will allow prediction of the long-line effect on oscillator stability.



Reike Diagram
Figure 4

TECHNICAL ARTICLE

FET Biasing

James Sherwin

INTRODUCTION

Engineers often design FET amplifiers that are unnecessarily sensitive to device characteristics because they may not be familiar with proper biasing methods.

One way to obtain consistent circuit performance in spite of wide device variations is to use a combination of constant-voltage and self biasing. The combined circuit configuration turns out to be the same as that generally used with bipolar transistors, but its operation and design are quite different.

Three Basic Circuits

Let's examine three basic common-source circuits that can be used to establish a FET's operating point (Q-point) and then see how two of them can be combined to provide greatly improved performance. The three basic biasing schemes are:

- Constant-voltage bias, which is most useful for rf and video amplifiers employing small dc drain resistors.
- Constant-current bias, which is best suited to low-drift dc amplifier applications such as source followers and source-coupled differential pairs.
- Self bias (also called source bias or automatic bias), which is a somewhat universal scheme, particularly valuable for ac amplifiers.

The Q-point established by the intersection of the load line and the $V_{GS} = -0.4$ V output characteristic of Figure 1 provides a convenient starting point for the circuit comparison. The load line shows that a drain supply voltage, V_{DD}, of 30 V and a drain resistance, R_D, of 39K Ω are being used.

The quiescent drain-to-source voltage, V_{DSQ}, is 15 V, allowing large signal excursions at the drain. Maximum input signal variations of ±0.2 V will produce output voltage swings of ±7.0 V – a voltage gain of 35.

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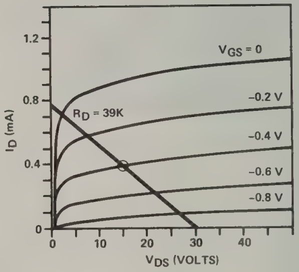


Figure 1. A large dynamic range is provided by the operating point at $V_{DSQ} = 15$ V, $I_{DQ} = 0.39$ mA and $V_{GSQ} = -0.4$ V. The output characteristics are for a typical 2N4339.

The constant-voltage bias circuit (Figure 2) is analyzed by superimposing a line for V_{GG} = constant on the transfer characteristic of the FET.

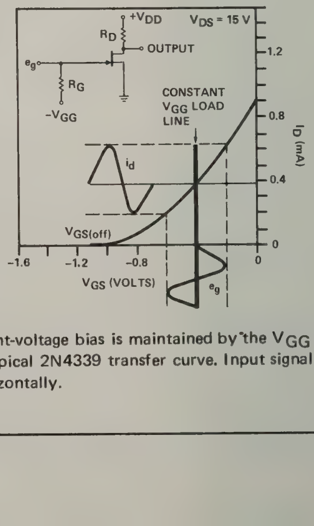


Figure 2. Constant-voltage bias is maintained by the V_{GG} supply as shown on this typical 2N4339 transfer curve. Input signal e_g moves the load line horizontally.

The transfer characteristic is a plot of I_D vs V_{GS} for constant V_{DS}. Since the curve doesn't change much with changes in V_{DS}, it is quite useful in establishing operating bias points. In fact, it is probably more useful than the output characteristics because its curvature clearly warns of the distortion to be expected with large input signals. Furthermore, when a bias load line is superimposed, allowable signal excursions become evident and input voltage, gate-source signal voltage, and output signal current calculations may be made graphically.

The heavy vertical line at $V_{GS} = -0.4$ V establishes the Q-point of Figure 1. No voltage is dropped across resistor R_G because the gate current is essentially zero. R_G serves mainly to isolate the input signal from the V_{GG} supply.

Excursions of the input signal, e_g, combine in series with V_{GS} so that they add algebraically to the fixed value of −0.4 V. The effect of signal variation is to instantaneously shift the bias line horizontally without changing its slope. The shifting bias line then develops the output signal current as shown in Figure 2.

The constant-current bias approach (Figure 3) for establishing the Q-point of Figure 1 requires a 0.39-mA current source. For an ideal constant-current generator, input signal excursions merely shift the bias line horizontally and produce no resultant gate-source voltage excursion. This bias technique is therefore limited to source followers, source-coupled differential amplifiers, and to ac amplifiers where the source terminal is bypassed to ground at the signal frequency.

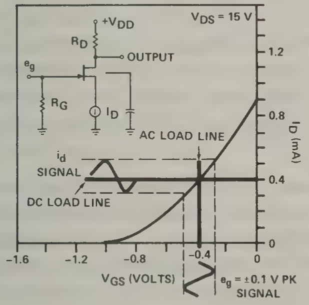


Figure 3. Constant-current bias fixes the output voltage for any R_D. Hence, input signals cannot affect the output unless the current source is bypassed.

If an ac ground is provided by a bypass capacitor across the current source, a vertical ac bias line will be established. Input signal variations will then translate the ac bias line horizontally, and signal development will proceed as with constant-voltage biasing (Figure 3).

Should the bypass capacitor not provide a sufficiently low reactance at the signal frequency, the ac bias line will not be vertical. It will still intersect the transfer curve at the Q-point but with a slope equal to $-(1/X_C) = -\omega C$ (Figure 4).

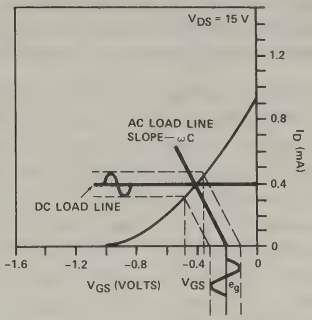


Figure 4. Partial bypassing of the current source (Figure 3) lowers the circuit gain by tilting the ac load line from the vertical. The capacitor drop subtracts from e_g.

This will lower the gain of the amplifier because of signal degeneration at the source. The input signal, e_g, is reduced by the drop across the capacitor:

$$v_{gs} = e_g - v_S = e_g - i_S X_C \qquad (1)$$

It is clear from Figure 4 that the input signal only shifts the operating point by an amount equal to V_{gs}, the effective input signal. As the signal frequency is decreased, the slope of the ac bias line decreases, causing the effective input signal to approach zero.

Self Bias Needs No Extra Supply

The self-bias circuit (Figure 5) establishes the Q-point by applying the voltage dropped across the source resistor, R_S, to the gate. Since no voltage is dropped across R_S when $I_D = 0$, the self-bias load line passes through the origin. Its slope is given by $-1/R_S$. Therefore, the desired Q-point is established by setting $-1/R_S = I_{DQ}/V_{GSQ}$.

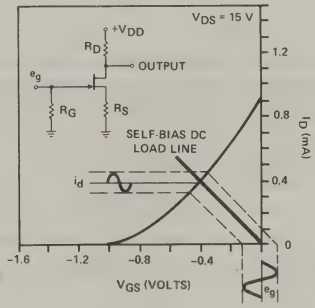


Figure 5. The self-bias load line passes through the origin with a slope $-1/R_S$. Bypassing R_S will steepen the slope and increase the gain of the circuit.

Signal development is the same as in the case of the partially bypassed constant-current scheme except that the load line is a dc bias line. Signal degeneration is described by Equation 1 with X_C replaced by R_S. The ac gain of the circuit can be increased by shunting R_S with a bypass capacitor, as in the constant-current case. The ac load line then passes through the Q-point with a slope $-(1/Z_S) = -(\omega C + 1/R_S)$.

The circuit is biased automatically at the desired Q-point, requires no extra power supply and provides a degree of current stabilization not possible with constant-voltage biasing.

A fourth biasing method, combining the advantages of constant-current biasing and self biasing, is obtained by combining the constant-voltage circuit with the self-bias circuit (Figure 6). A principal advantage of this configuration is that an approximation may be made to constant-current bias without any additional power supply. The bias load line may be drawn through the selected Q-point and given any desired slope by properly choosing V_{GG}. (The bias line intercepts the V_{GS} axis at V_{GG}.) The larger V_{GG} is made, the larger R_S will be and the better will be the approximation to constant-current biasing.

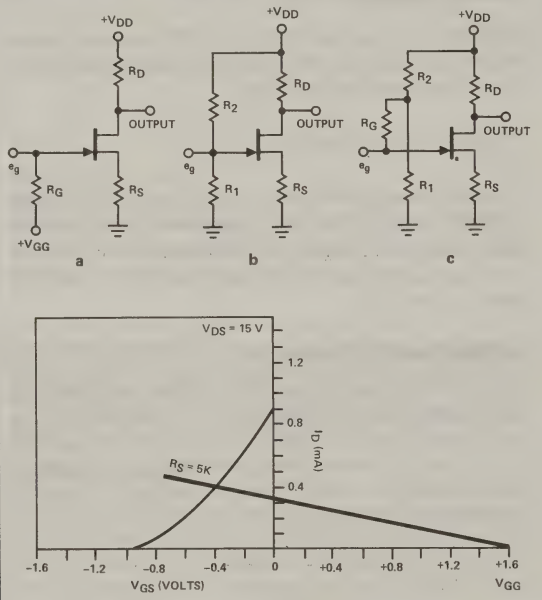


Figure 6. All three combination-bias circuits are equivalent. They add constant-voltage biasing to the self-bias circuit to establish a reasonably flat load line without sacrificing dynamic range.

All three circuits in Figure 6 are equivalent. Circuit 6(a) requires an extra power supply. The need for an additional supply is avoided in 6(b) by deriving V_{GG} from the drain supply. R_1 and R_2 are simply a voltage divider. To maintain the high input impedance of the FET, R_1 and R_2 must both be very large.

Very large resistors cannot always be found in the exact ratio needed to derive the desired V_{GG} in every circuit application. Circuit 6(c) overcomes this problem by placing a large R_G between the center point of the divider and the gate. This allows R_1 and R_2 to be small, without lowering the input impedance.

One point of caution worth remembering is that as V_{GG} is increased, V_S increases, and V_{DS} decreases. Therefore with low V_{DD}, there may be a significant decrease in the allowable output voltage swing.

Biasing for Device Variations

The value of the combination-bias technique becomes apparent when one considers the normal production spread of device characteristics. The problem is illustrated in Figure 7 where two limiting sets of output characteristics, representing the actual min-max spread of the Siliconix 2N4339, are presented. Limiting characteristics like these are not normally available. Even if they were, however, they'd be of little help in establishing operating points suitable for all devices with output characteristics lying between the two extremes. The problem is much more easily approached by using the set of limiting transfer characteristics of Figure 8. (See next page.)

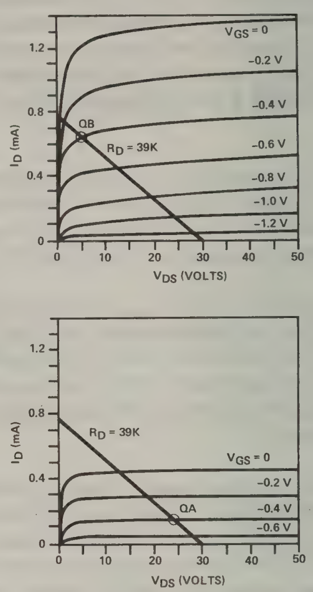


Figure 7. The wide variations in device performance shown by this pair of output characteristics make clear the disadvantages of constant-voltage biasing.

Attempting to establish suitable constant-voltage bias conditions for a production spread of devices is practical only for circuits with very small values of dc drain resistance – for example, circuits with inductive loads. As the constant-voltage bias plot of Figure 8 reveals, constant gate bias causes a significant difference in operating I_{DQ} for the extreme limit devices. At $V_{GS} = -0.4$ V, the range of I_{DQ} is 0.13 to 0.69 mA, and V_{DSQ} for a given R_D will vary greatly for most resistance-loaded circuits. For the example of Figure 1, with $R_D = 39\text{K}\ \Omega$ and $V_{DD} = 30$ V, V_{DSQ} varies from near saturation (5 V) to 25 V.

An apparently excellent method of biasing is the constant-current method of Figure 3. Biasing in this manner fixes the operating drain current for all devices and sets V_{DSQ} to $V_{DD} - I_{DQ}R_L$ for any device in the production spread. V_{GS} automatically finds a value to set the appropriate I_{DQ} = constant for all devices. For the constant-current bias plot of Figure 8, with $I_{DQ} = 0.39$ mA, V_{GS} would range from –0.11 to –0.67 V.

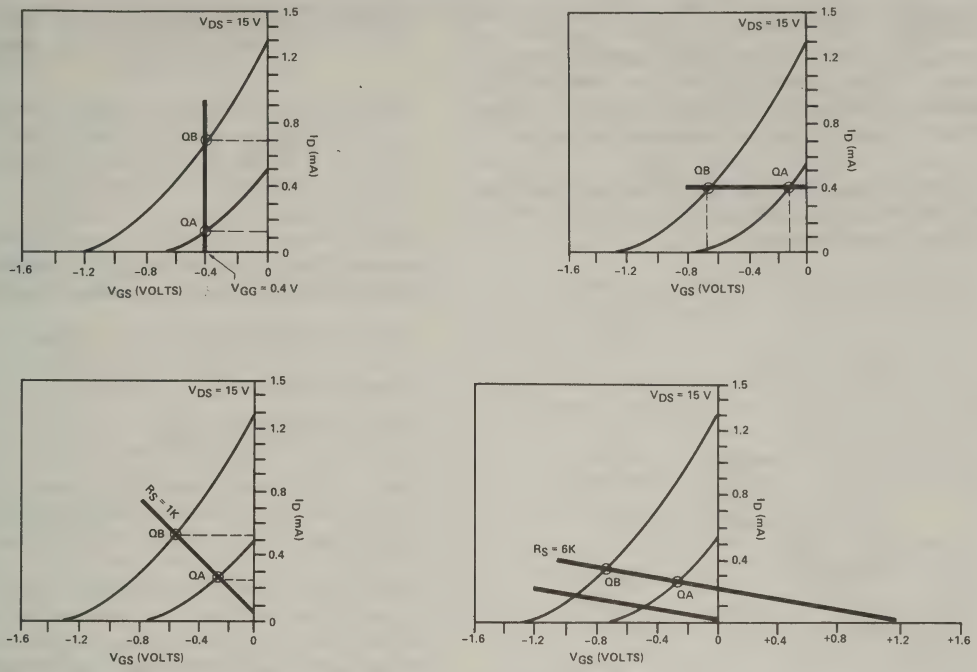


Figure 8. The advantages of combination biasing, when one is working with a spread of device characteristics, are made obvious by plotting the load lines for the various types of biasing on a pair of limiting transfer curves.

Output characteristics are not needed as long as I_{DQ} is chosen to be below the minimum I_{DSS}. With $R_D = 39K\ \Omega$ and $V_{DD} = 30$ V, V_{DSQ} is 14.8 V for all devices.

The disadvantages of the constant-current method are that it allows no signal to be developed unless the current source is bypassed and, as we shall see, it lacks the flexibility to provide constant gain despite variations in the forward transconductance, g_{fs}, of the devices.

The self-bias scheme is a reasonable choice for single-ended dc amplifiers and for ac amplifiers. In unbypassed or dc circuits, some compromise must be made between the gain loss due to current feedback degeneration and the advantage of current stabilization achieved with high R_S.

An appropriate choice of I_{DQ} limits can be made by using the pair of limiting transfer curves. For example, for $R_S = 1K\ \Omega$, the load line shown on the self-bias curve of Figure 8 is established. The maximum I_D is 0.52 mA, and the minimum I_D is 0.24 mA. The operating range of V_{DSQ} may be calculated for any value of V_{DD} and R_D. Clearly, for $R_D = 39K\ \Omega$, the maximum-limit device (device B) would operate with $V_{DSQ} = 9.8$ V and the minimum-limit device (device A) would operate with $V_{DSQ} = 20.6$ V. This results in fairly satisfactory operation for all devices. However, such a variation in I_{DQ} imposes severe limitations on the circuit design.

A better approach is illustrated by the combination-bias curve of Figure 8 with $V_{GG} = 1.2$ V. The range of I_{DQ} for this bias condition is 0.25 mA to 0.32 mA. A similar minimum difference in I_{DQ} could be achieved with $R_S = 6K\ \Omega$ and $V_{GG} = 0$, (a self-bias condition) but the operating points would be pushed toward the toe of the transfer characteristics and allowable signal input would be reduced.

The upper load line allows $v_{gs} = \pm 1.8$ V (limited by I_{DSSA}), while the lower line allows a v_{gs} of only ±0.7 V (limited by $V_{GS(off)A}$). (The subscript letters A and B refer to the minimum and maximum devices, respectively.) The combination circuit allows almost ideal operation over the full production spread of devices. Even with $R_D = 62K\ \Omega$, the V_{DSQ} would range only between 10 and 15 V.

For this circuit, R_D should be chosen to allow the largest output signal swing for I_{DQ} midway between the two extremes of 0.25 and 0.32 mA; namely 0.285 mA. Setting the voltage drop across R_D at one-half of ($V_{DD} - 2V_{GS(off)typ}$) or 14 V, yields $R_D = (14\text{ V}/0.285\text{ mA}) = 49K\ \Omega$.

It is helpful, in any design, to know the effect of temperature variations on the transfer curves and transconductance characteristics. Ideally, minimum and maximum transfer characteristics would be plotted at three temperatures: above, below, and at room temperature. Then the design would take all types of variation into account.

Minimize the Gain Variations

Leaving R_S unbypassed helps reduce gain variations from device to device by providing degenerative current feedback. However, this method for minimizing gain variations is only effective when a substantial amount of gain is sacrificed.

A better approach is to use the combination-bias technique with the bias point selected from the transfer and transconductance curves (Figure 9).

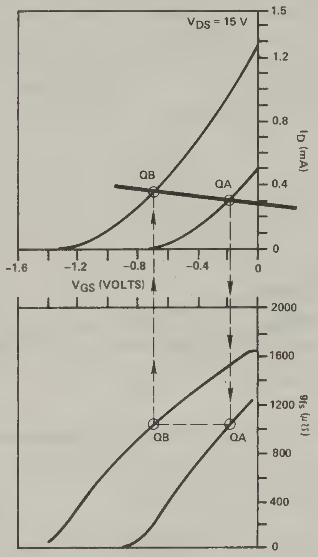


Figure 9. Gain variations are minimized when the load line is designed to intersect the pair of limiting transfer curves (top) at points of equal g_{fs} (bottom).

As Figure 9 shows, it is possible to find an R_S and a V_{GG} that will set I_{DQA} and I_{DQB} to values so that g_{fsQ} will be the same for both devices. The g_{fsQ} of all intermediate devices will be approximately equal to the limiting values. Thus, a constant, or nearly constant, stage gain is obtained even with a bypass capacitor.

The design procedure is as follows:

Step 1. Select a desired I_{DQA} below I_{DSSA}. A good value, allowing for temperature variations, is 60% of I_{DSSA}. This will allow for decreasing I_{DSS} due to temperature variation and for reasonable signal excursions in load current.

Step 2. Enter the transfer curves at $I_{DQA} \cong 0.6\ I_{DSSA}$ (0.3 mA) to find V_{GSQA}. This $V_{GSQA} \cong 0.2$ V for the 2N4339.

Step 3. Drop vertically at V_{GSQA} to the minimum limit transconductance curve to find g_{fsQA}. The value as read from the plot is approximately 1000 μmho.

Step 4. Travel across the g_{fs} plot to the maximum curve to find V_{GSQB} at the same value of g_{fs}. This is $V_{GSQB} \cong -0.7$ V.

Step 5. Travel vertically up to the maximum limit transfer curve to find I_{DQB} at V_{GSQB}. This is $I_{DQB} \cong 0.36$ mA.

Step 6. Construct an R_S bias line through points Q_A and Q_B on the transfer curves. The slope of the line is $1/R_S$, and the intercept with the V_{GS} axis is the required V_{GG}.

As Figure 9 demonstrates, it may be somewhat inconvenient to perform Step 6 graphically. An algebraic solution can then be employed instead. The source resistance is given by

$$R_S = (V_{GSQA} - V_{GSQB})/(I_{DQB} - I_{DQA}) \qquad (2)$$

and the bias voltage is

$$V_{GG} = R_S\, I_{DQB} + V_{GSQB} \qquad (3)$$

Care should be taken to maintain the proper algebraic signs in Equations 2 and 3. (For n-channel FETs, V_{GS} is negative and I_D is positive. For p-channel units, the signs are reversed.)

If the transconductance curves of Figure 9 are not available, g_{fs} can be determined by simply measuring the slope of the transfer curve at the desired operating point. Just place a straight-edge tangent to the curve at the Q-point and note the points at which it intercepts the I_D and V_{GS} axes. The slope and g_{fs} are given by:

$$\text{slope} = g_{fs} = I_{D(\text{intercept})}/-V_{GS(\text{intercept})} \qquad (4)$$

In designing a constant-gain circuit, simply set the straight-edge tangent to the transfer curve of device A at point Q_A and slide it, without changing its slope, until it is tangent to the curve of device B. The tangency point is Q_B.

Designing Without Output Curves

Although the transfer characteristic has been seen to be extremely valuable in designing a bias circuit, it cannot be used to graphically establish V_{DSQ}. However, if a set of output curves is not available, V_{DSQ} can be determined or selected from the transfer curve by using the following procedure:

Step 1. Establish R_S and limiting values of I_{DQ}, V_{GSQ} and g_{fsQ} from the transfer curve.

Step 2. Establish V_{DD} as available, but in no case greater than BV_{GSS} nor less than several times $V_{GS(off)}$. There are special cases where V_{DD} will be below this limit, but in no case should instantaneous v_{dg} be allowed to fall below $2 \times V_{GS(off)}$ if minimum distortion is to be achieved.

Step 3. Set V_{DSQ} approximately midway between V_{DD} and $2 \times V_{GS(off)}$; lower if large output signals will not be handled.

Step 4. Select R_D to give the appropriate V_{DSQ}. The formula is:

$$R_D = [(V_{DD} - V_{DSQ})/0.5\ I_{DQA} + I_{DQB}] - R_S \qquad (5)$$

In the example of Figure 8, this procedure would have yielded $V_{DSQ} = (30\text{-}3)/2 = 13.5$ V and $R_D = (30 - 13.5)/0.5\,(0.52 + 0.24)$ mA – 1K Ω = 42.5K Ω.

Step 5. Check to ensure that with this R_D, device B is not in a saturated condition – $V_{DQB} = V_{DD} - I_{DBQ}\,R_D > 2V_{GS(off)} + R_S\,I_{DBQ}$.

Decrease R_D if this condition is not met.

An alternate method, that selects R_D to provide a specified voltage gain, follows Steps 1 and 2 above and then proceeds as follows:

Step 3. Determine required stage gain, A_v, and set $R_D = A_v/g_{fsQ}$.

Step 4. Calculate V_{DSQ} to ensure that the criteria of Step 2 are not violated:

$$V_{DSQ} = V_{DD} - (R_D + R_S)\,I_{DQ} \qquad (6)$$

Step 5. If necessary, change I_{DQ}, V_{DD}, A_v and/or R_D to obtain an optimum compromise. ■■

FET SOURCE-FOLLOWER CIRCUITS

Too little knowledge of biasing methods for FET amplifiers sometimes keeps engineers from making maximum use of FETs in circuit designs. The common-drain amplifier, or source follower, is a particularly valuable configuration; its high input impedance and low output impedance make it very useful for impedance transformations between FETs and bipolar transistors.

By considering 10 circuits, which represent virutally every source-follower configuration, the designer can obtain consistent circuit performance despite wide device variations.

There are two basic connections for source followers: with and without gate feedback. Each connection comes in several variations (Figure 10). Circuits 10(a) through 10(e) have no gate feedback; their input impedances, therefore, are equal to R_G. Circuits 10(f) through 10(k) employ feedback to their gates to increase the input impedance above R_G.

Before getting into the details of bias-circuit design, note several general observations that can be made about the circuits of Figure 10:

- Circuits a, d and f can accept only positive and small negative signals, because these circuits have their source resistors connected to ground. The other circuits can handle large positive and negative signals limited only by the available supply voltages and device breakdown voltage.
- Circuits c, d, e, h, j, and k employ current sources to improve drain-current (I_D) stability and increase gain.
- Circuits d, e and k employ FETs as current sources. In circuit d, Q_2 must have a lower cut-off voltage, $V_{GS(off)}$, and a lower zero gate-voltage drain current, I_{DSS}, than Q_1.
- Circuits e, g, h and k employ a source resistor, R_S, which may be selected to set the quiescent output voltage equal to zero.
- Circuits e and k use matched FETs. R_S is selected to set I_D near the specified low-drift operating current. The input-output offset is zero.

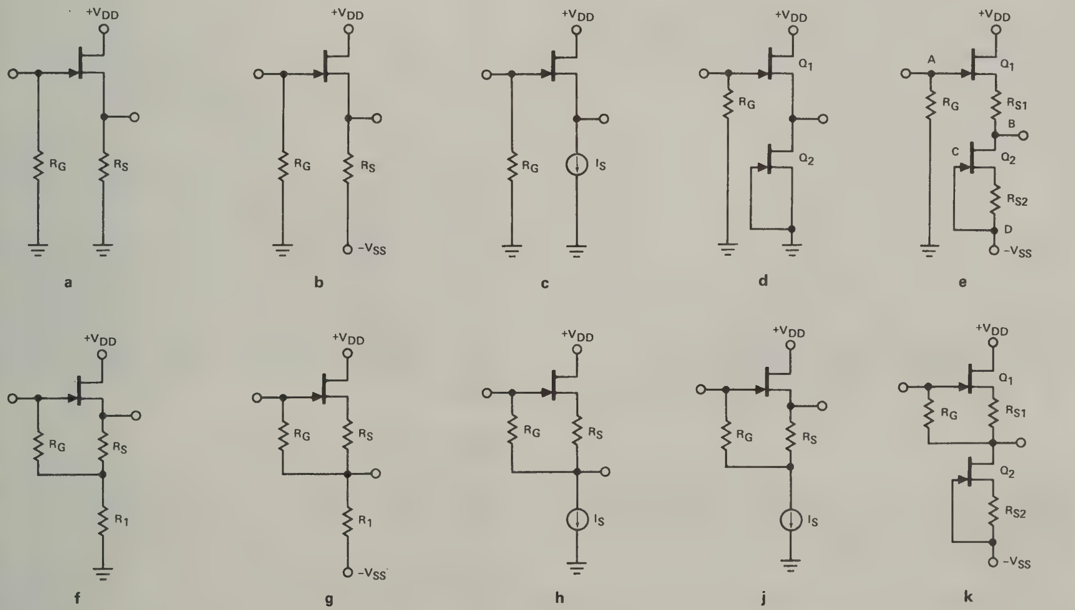


Figure 10. Virtually every practical source-follower configuration is represented in this collection of ten circuits. The configurations in the top row do not employ gate feedback; the corresponding ones in the bottom row do.

Biasing Without Feedback is Simple

The no-feedback circuits of Figure 10 (circuits 10(a) through 10(e) use simple biasing techniques (see the earlier article). Circuit 10(a) is a self-bias configuration; the voltage drop across R_S biases the gate (which draws essentially zero current) through resistor R_G. Since no gate-to-source voltage, V_{GS}, can be developed when $I_D = 0$, the self-bias load line passes through the origin (Figure 11). For the 2N4339 FET, whose limiting transfer characteristics are used throughout this article, the quiescent drain current is seen to lie between about 0.25 and 0.55 mA when a 1K Ω source resistor is used. The quiescent output voltage lies between +0.25 and +0.55 V.

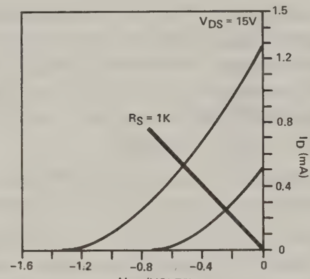


Figure 11. Self biasing (Figure 10a) uses the voltage dropped across the source resistor, R_S to bias the gate. The load line passes through the origin and has a slope of $-1/R_S$.

Circuit 10(b) is another example of source-resistor biasing with a $-V_{SS}$ supply added. The advantage over circuit 10(a) is that the signal voltage can swing negative to approximately $-V_{SS}$. Two bias lines are shown in Figure 12, one for $V_{SS} = -15$ V and the other $V_{SS} = -1.6$ V. For the first case, the quiescent output voltage lies between +0.18 and +0.74 V. For the second, it lies between +0.3 and +0.82 V.

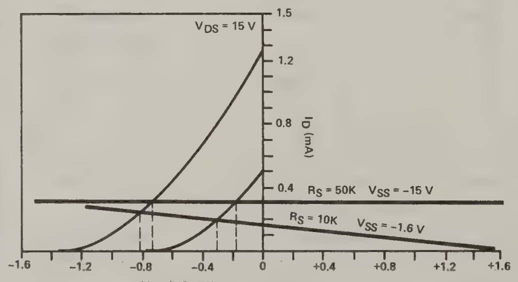


Figure 12. Adding a V_{SS} supply to the self-bias circuit (Figure 10b) allows it to handle large negative signals. The load line's intercept with the V_{GS}-axis is at $V_{GS} = -V_{SS}$. Bias lines are shown for $V_{SS} = -15$ V and $V_{SS} = -1.6$ V.

The bias load line for circuit 10(c) is just a horizontal line (I_D = constant). The quiescent output voltage is between +0.15 and 0.7 V for $I_D = 0.3$ mA.

Circuit 10(d) is similar to 10(c) except that the $V_{GS} = 0$ output characteristic of FET Q_2 is used as a current source. As seen in Figure 13, Q_2 does not supply constant current when its V_{DS} gets very small. This technique should therefore be used only to bias FETs whose $V_{GS(off)}$ is significantly higher than the equivalent $V_{GS(off)}$ of the current-source FET diode.

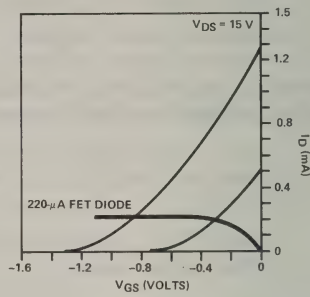


Figure 13. FET Q_2 doesn't behave like an ideal current source when its V_{DS} gets very small (Figure 10d). Therefore, Q_1 should have a significantly larger $V_{GS(off)}$ than Q_2 does.

A pair of matched FETs is used in the circuit of Figure 10(e), one as a source follower and the other as a current source. The operating drain current (I_{DQ}) is set by R_{S2}, as indicated by the load line of Figure 14. The drain current may be anywhere from 0.20 to 0.42 mA, as shown by the limiting transfer characteristic intercepts; however, $V_{GS1} = V_{GS2}$ because the FETs are matched.

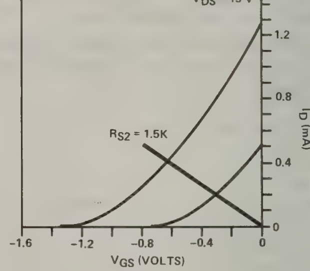


Figure 14. This load line is set by R_{S2} and Q_2 which acts as a current source (Figure 10e). If its components are properly matched, the circuit will have zero or near-zero offset.

Since $I_{D1} = I_{D2}$ and $V_{GS1} = V_{GS2}$, choosing $R_{S1} = R_{S2}$ will ensure that the voltage from point A to B equals the voltage point from point C to D (Figure 10(e)). This source follower, therefore, exhibits zero or near-zero offset. If the FETs are temperature-matched at the operating I_D, the source follower will exhibit zero or near-zero temperature drift.

Biasing With Feedback Increases Z_{in}

Each of the feedback-type source followers (Figure 10(f) through 10(k)) is biased by a method similar to that used with the nonfeedback circuit above it. However, in each case, R_G is returned to a point in the source circuit that provides almost unity feedback to the lower end of R_G. If R_S is chosen so that R_G is returned to zero dc volts (except in circuit 10(f), then the input/output offset is zero. R_1 is usually much larger than R_S.

Circuit 10(f) is useful principally for ac-coupled circuits. R_S is usually much less than R_1 to provide near-unity feedback. The bias load line is set by R_S (Figure 15). The output load line, however is determined by the sum of $R_S + R_1$. The feedback voltage V_{FB}, measured at the junction of R_S and R_1, is determined by the intercept of the $R_S + R_1$ load line with the V_{GS} axis. The quiescent output voltage is $V_{FB} - V_{GS}$.

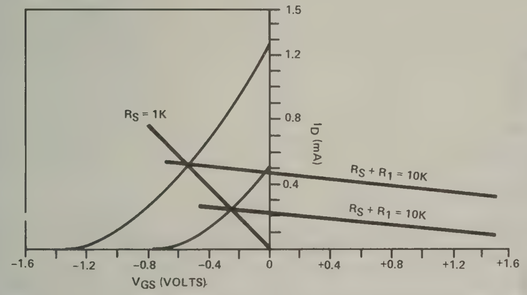


Figure 15. The bias load line is set by R_S but the output load line is determined by $R_S + R_1$ when gate feedback is employed (Figure 10f). The feedback V_{fb} is determined by the intercept of the $R_S + R_1$ load line and the V_{GS} axis.

In the circuit of Figure 10(g), R_S can be trimmed to provide zero offset. As the curves show (Figure 16), R_S will be between 670 ohms and 2.5K Ω. R_S is much less than R_1. The source load line intercepts the V_{GS} axis at $V_{SS} = -V_{GG} = -15$ V.

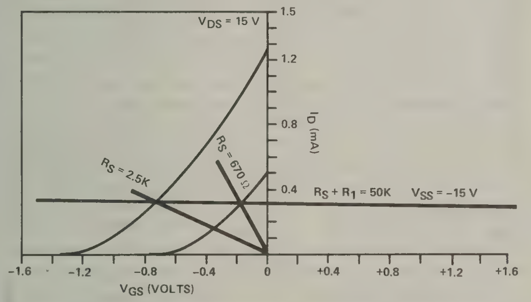


Figure 16. R_S can be trimmed to provide zero offset at some point between 670 ohms and 2.5K Ω (Figure 10g). The source load line intercepts the V_{GS} axis at $V_{SS} = V_{GG} = -15$ V. Note that this load line is not perfectly flat. It has a slope of −1/50K, because the current source is not perfect; it has a finite impedance.

Circuit 10(h) is almost the same as 10(g); the difference is that resistor R_1 is replaced by a current source. Since an ideal current source has infinite impedance, the bias curve of circuit 1(h) differs from that of Figure 10(g) (Figure 16) in that the load line is perfectly flat. In Figure 16 the load line is almost, but not quite, flat; it has a slope of −1/50k.

Circuit 10(j) is similar to 10(h) except that the output is taken from the top of R_S to reduce the output impedance. R_S must be trimmed if the circuit is to work at all properly.

In Figure 17, the constant-current load line represents a 0.3-mA current source, and the effect of a 1K Ω source resistor is shown. The offset voltage is seen to lie between 0.2 and 0.75 V. The intercept of the R_S load line and the V_{GS} axis sets the voltage at the junction of R_S and the current source (V_{FB}). For R_S = 1K Ω, V_{FB} will be between −0.1 V and +0.45 V. Since V_{FB} appears at the gate, it must be zero if the dc input impedance of the circuit is to be preserved.

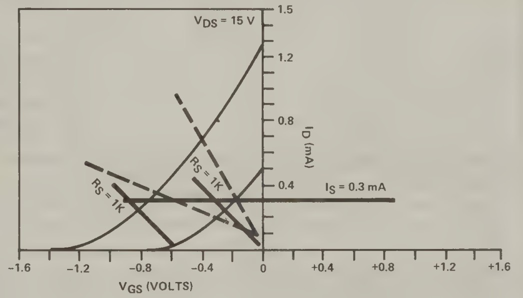


Figure 17. If R_S is not trimmed so that the load line passes through the origin, a voltage will appear at the gate causing a reduction in dc input impedance. The incremental input impedance will not be affected.

This can be done by trimming R_S, as shown dashed in Figure 17. The biasing then becomes the same as for circuit 10(h).

Biasing for circuit 10(k) is identical to that for circuit 10(e) (Figure 14) except that feedback is added to raise the input impedance.■■

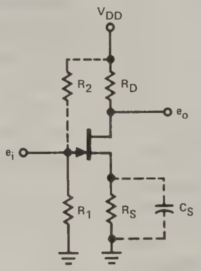
REFERENCES

(1) Sherwin, J.S., "How, Why and Where to Use FETs," *Electronic Design,* May 17, 1966, p. 94.

(2) Sherwin, J.S., "Knowing the Cause Helps to Cure Distortion in FET Amplifiers," *Electronics,* Dec. 12, 1966, pp. 99-105.

Amplifier Charts

For convenience this chart offers the designer circuit values for a variety of commonly used J-FET amplifiers.

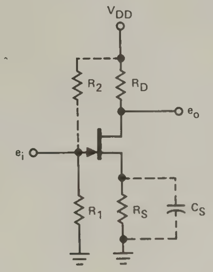


Amplifier Design Chart
(C_S for 3 dB Point at 50 Hz)

V_{DD} (V)	R_S (Ω)	R_1 (MΩ)	R_2 (MΩ)	C_S (μF)	I_{DD} (mA)	R_D (Ω)	e_o Max (V)	A_V
J111								
30	560	1	∞	100	11	1K	3	9
	2.7K	3.3	10	100	6	1K	2.5	8
V_{DD} = 15 V_{SS} = -15	3K	1	Source Follower		7	0	8.5	0.96
	7.5K	1			6	0	8.5	0.96
V_{DD} = 15 V_{SS} = -15	7.5K	1	Source Follower		6	0	15	0.97
J112								
20	2K	4.7	11	100	5	1K	1.5	8-11
	330	1	∞	100	8	820	1.5	9
	330	1	∞	0	8	820	3	1.9
30	2K	4.7	11	100	6	2.7K	5	18-24
	330	1	∞	100	8	1.5K	2.5	15
	330	1	∞	0	8	1.5K	5.5	3.3
V_{DD} = 15 V_{SS} = -15	4.7K	1	Source Follower		5	0	11	0.97
J113								
10	220	1	∞	0	5	1.2K	1.5	3.5
20	220	1	∞	0	5	2.2K	3.5	7
30	1K	1	12	100	4	3.9K	5	38
	1K	1	12	100	4	5.6K	3.5	40-55
V_{DD} = 15 V_{SS} = -15	4.7K	1	Source Follower		2.5	0	13	0.98
	7.5K	1			1.5	0	13	0.98

V_{DD} (V)	R_S (kΩ)	R_1 (MΩ)	R_2 (MΩ)	C_S	I_{DD} (μA)	R_D (kΩ)	e_o Max (pK V)	A_V
2N4117								
10	10	1M	∞		45	120	1	5.7
20	10	1M	∞		45	270	1.5	12
						360	1	15
30	10	1M	∞		45	420	4	17
						620	1	22
V_{DD} = +15 V_{SS} = -15	510	1M	∞	Source Follower	35	0	8	0.97
2N4118								
10	8.2	1M	∞		120	36	0.6	2.2
						50	0.2	3.5
20	8.2	1M	∞		120	120	1	7.5
30	8.2	1M	∞		120	180	2	10
V_{DD} = +15 V_{SS} = -15	510	1M	∞	Source Follower	35	0	8	0.97
2N4119								
20	56	1	∞	5 μF* at 5 V	70	150	1	10
30	56	1	∞		70	240	3	17
						330	1	17-23
20	6.8	1	∞		300	27	1	1.8
30	6.8	1	∞		300	68	2	4.5
V_{DD} = +15 V_{SS} = -15	510	1	∞	Source Follower	40	0	10	0.97

*AC Amplifier



Amplifier Design Chart

V_{DD} (V)	R_S (Ω)	R_1 (Ω)	R_2 (Ω)	C_S (μF)	I_{DD} (mA)	R_D (KΩ)	e_o Max (pk V)	A_V
2N4338								
15	1500	1M	∞	0	0.25	36	2.5	9-12
				30		36	1.5	16-24
						47	2.0	20-30
	5100	1M	∞	0	0.12	82	3.0	10-10.5
				25		82	1.5	24-37
	36K	1M	2M	30	0.15	27	1.0	13-18.5
30	1500	1M	∞	0	0.25	82	4.0	21.5-27
				30		82	2.5	32-49
						100	3.0	43-64
	5100	1M	∞	0	0.12	150	4.5	14.5-16
				25		150	2.5	38-54
						200	1.5	40-50
	36K	1M	5M	30	0.15	82	5.0	37-52
45	1500	1M	∞	0	0.25	120	6.5	27-33
				30		120	4.0	45-68
	5100	1M	∞	0	0.12	270	10	28-31
				25		270	5.0	76-105
	36K	1M	8.2M	0	0.15	120	14	2.8
				30		120	7.0	54-76
V_{DD} = +15 V_{SS} = −15	100K	1M	∞	0	0.15	0	9.0	0.98
2N4339								
15	1800	1M	∞	0	0.42	20	3.0	7-7.5
				40		20	2.0	17-22
						27	2.0	23-27
	9100	1M	6.8M	35	0.32	18	2.0	17-19
						30	2.5	26-28
	27K	1M	3M	25	0.2	22	1.0	16-18
						43	2.0	28-30
30	1800	1M	∞	0	0.42	47	6.5	15-17
				40		47	4.0	38-47
						51	4.5	40-50
	9100	1M	13M	0	0.32	43	8.0	4.5
				35		43	5.0	40-43
						68	4.5	53-60
	27K	1M	7.5M	25	0.2	68	4.0	49-52
						100	7.0	66-70
45	1800	1M	∞	0	0.42	75	7.5	23-25
				40		75	5.0	58-70
						100	7.0	73-77
	9100	1M	22M	0	0.32	68	7.0	7.0
				25		68	6.5	59-64
						120	7.0	80-85
	27K	1M	12M	0	0.2	100	12	3.3
				25		100	5.0	65-68
						180	8.0	100-115
V_{DD} = +15 V_{SS} = −15	75K	1M	∞	0	0.22	0	10	0.98

V_{DD} (V)	R_S (Ω)	R_1 (Ω)	R_2 (Ω)	C_S (μF)	I_{DD} (mA)	R_D (KΩ)	e_o Max (pk V)	A_V
2N4340								
15	680	1M	∞	0	1.5	5.1	3.0	3.5-4
				65		5.1	1.5	7-8.5
						6.8	2.0	9-10.5
	1200	1M	∞	0	1.1	7.5	2.5	3.5-4
				60		7.5	2.0	9-11
						10	2.0	11-13
	3900	1M	∞	0	0.4	18	4.0	3.5-4
				40		18	1.5	15-18
						22	1.0	19-22
30	680	1M	∞	0	1.5	12	6.0	9.5-10
				65		12	3.0	17-22
						18	1.0	24-26
	1200	1M	∞	0	1.1	18	6.0	9-9.5
				60		18	4.0	21-26
						24	2.0	29
	3900	1M	∞	0	0.4	39	7.0	7.5-8
				40		39	7.0	30-36
						62	0.5	34-45
	20K	1M	6.8M	35	0.35	30	3.0	25-27
						56	6.5	40
45	680	1M	∞	0	1.5	20	10.5	14-15.5
				65		20	8.0	27-32
						27	4.0	35
	1200	1M	∞	0	1.1	27	12.5	16-18
				60		27	5.0	30-37
						39	2.0	39-42
	3900	1M	∞	0	0.4	68	12	12-13
				40		68	7.0	52-61
						91	3.0	56-63
	20K	2M	3M	55	1.0	10	5.0	15
						20	4.0	27-28
V_{DD} = +15 V_{SS} = −15	22K	1M	∞	0	0.75	0	12	0.96
2N4341								
15	1000	1M	∞	70	2.7	2	1.0	3-3.5
						2.7	2.0	4-4.5
	1200	1.2M	7.5M	80	3.5	1.2	2.0	2.5
						2.2	3.0	3-4.5
	2000	1M	∞	65	1.8	3	2.0	4-4.5
						4.7	1.5	6-6.5
30	1000	1M	∞	0	2.7	6.2	7.0	4.0
				70		6.2	3.5	10
						9.1	1.5	11-13
	1200	1.1M	15M	80	3.5	3.9	4.0	7.5-8
	2000	1M	∞	0	1.8	9.1	6.0	3.0
				65		9.1	4.0	12
						15	1.0	13-19
	15K	1M	3.3M	50	0.7	18	3.0	16-21
45	1000	1M	∞	0	2.7	10	8.5	6.3
				70		10	6.0	16
	1200	1M	22M	80	3.5	6.8	7.0	13
	2000	1M	∞	0	1.8	15	8.5	5.5
				65		15	5.0	20-21
	15K	1M	5.6M	50	0.7	30	9.0	28-35
V_{DD} = +15 V_{SS} = −15	10K	1M	∞	0	1.9	0	13.5	0.94

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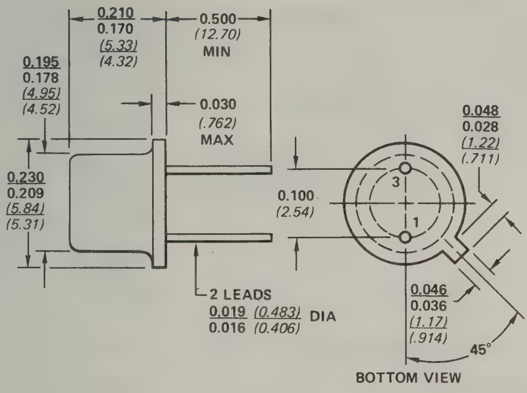
Mechanical Data

At Siliconix' option, lead finish will be either Gold Plate or Tin Plate. Electrical Characteristics are not affected.



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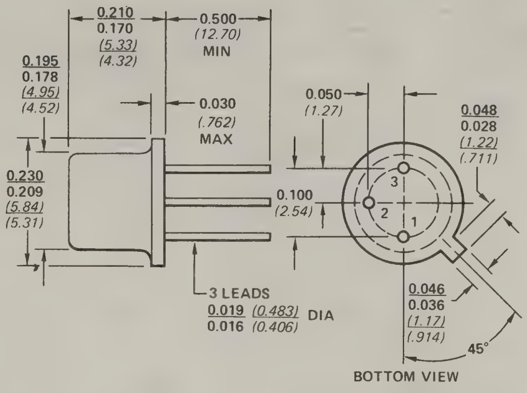
(2 PIN)



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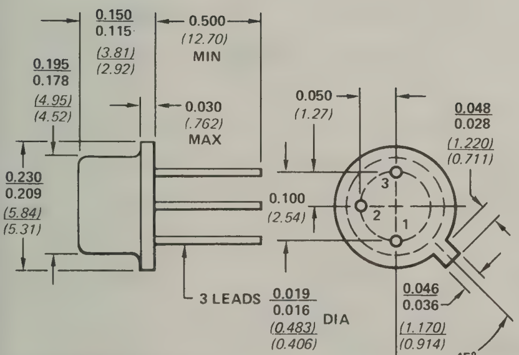
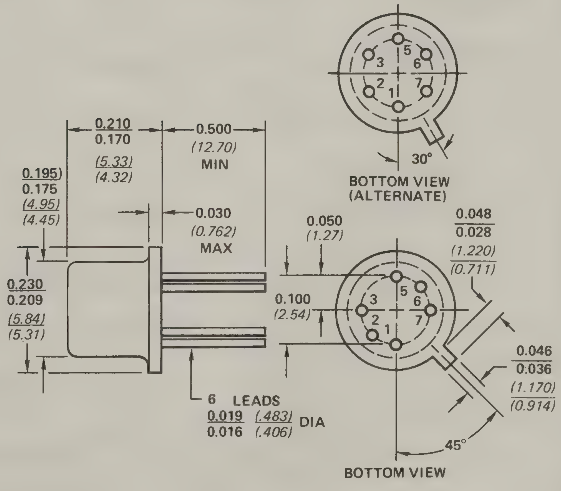


ALL DIMENSIONS IN INCHES.
(ALL DIMENSIONS IN MILLIMETERS.)

TO-52



TO-71

Mechanical Data (Cont'd)

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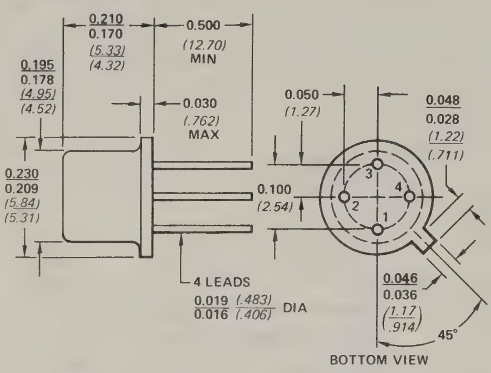

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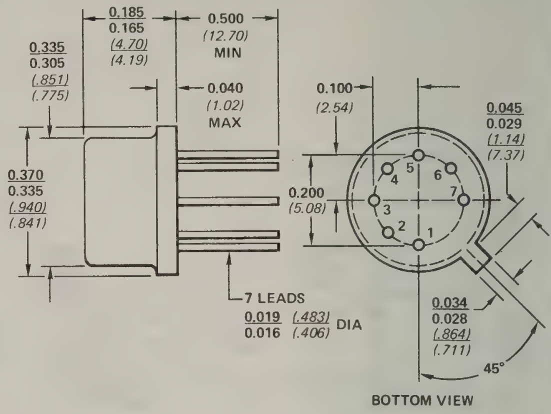

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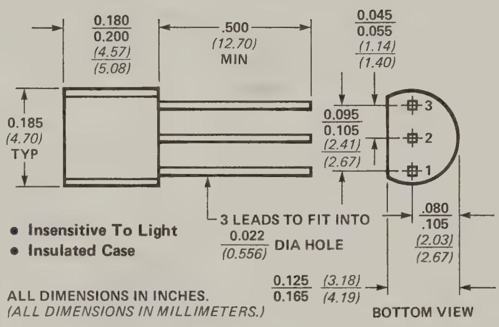
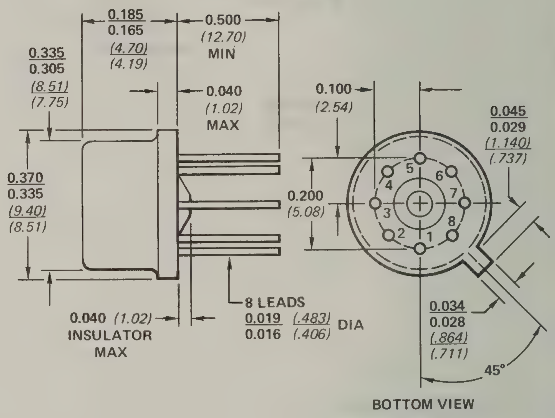


- **Insensitive To Light**
- **Insulated Case**

ALL DIMENSIONS IN INCHES.
(ALL DIMENSIONS IN MILLIMETERS.)

TO-92



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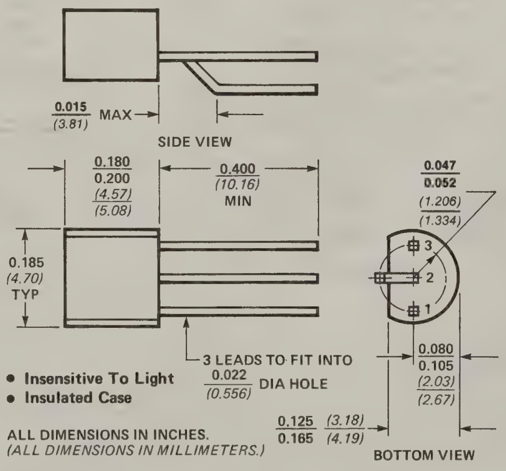

- **Insensitive To Light**
- **Insulated Case**

ALL DIMENSIONS IN INCHES.
(ALL DIMENSIONS IN MILLIMETERS.)

TO-92 LEAD FORM
(–18)

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Application Notes

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	AN70-1	FET Cascode Circuits Reduce Feedback Capacitance
F	AN70-2	FETs for Video Amplifiers
	AN71-1	A High Resolution CMRR Test Method
F	AN72-1	FETs in Balanced Mixers
A	AN72-2	FETs as Analog Switches
F	AN73-1	FETs as Voltage-Controlled Resistors
A	AN73-2	IC Multiplexer Increases Analog Switching Speeds
A	AN73-3	Switching High-Frequency Signals With FET Integrated Circuits
	AN73-4	Junction FETs in Active Double-Balanced Mixers
A	* AN73-5	Driver Circuits for the JFET Analog Switch
AIC	AN73-6	Function/Application of the L144 Programmable Micro-Power Triple Op Amp
F, A	* AN73-7	An Introduction to FETs
AIC	* AN74-1	Function/Application of the LD110/LD111 3½ Digit A/D Converter Set
A	AN74-2	Analog Switches in Sample and Hold Circuits
	AN74-3	Designing Junction FET Input Op Amps
F	* AN74-4	Audio-Frequency Noise Characteristics of Junction FETs
A	* AN75-1	CMOS Analog Switches—A Powerful Design Tool
	AN76-1	Measuring High Frequency S-Parameters on the Dual Gate MOSFET
A	* AN76-6	DG300 Series Analog Switch Applications
AIC	* AN76-7	Function/Application of the L161 Micropower Comparator
AIC	* AN77-1	Function/Application of the LD120/LD121 4½ Digit A/D Converter Set in Measurement Systems
M	* AN77-2	Don't Trade Off Analog Switch Specs. VMOS — A Solution to High Speed, High Current, Low Resistance Analog Switches
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M	* AN79-3	Dynamic Input Characteristics of a VMOS Power Switch
M	* AN79-4	Driving VMOS FETs
	AN79-5	Using the VN64GA High Current, High Power VMOS Power FET
M	* AN79-6	Using Power MOSFET Transistors to Interface from IC Logic to High Power Loads
	AN79-7	Applications of the VN10KM VMOS Power FET
M	* AN80-1	A Key to the Advance of Switching Power Supplies
M	AN80-2	Meet the VMOS FET Model
	AN80-3	Ultralinear Broadband Amplifier
	AN80-4	Enjoy VHF Power Amplifier Design
	AN80-6	AGC for the VMOS RF Power Amplifier
AIC	AN80-8	Function/Application of the LD122/LD121A ±4½ Digit A/D Converter Set in Measurement Systems
AIC	AN81-1	Microprocessor Interface Techniques As Applied to the Siliconix A/D Converter Family
AIC	AN81-2	Introduction to Quantized Feedback
F	* AN81-3	Composite Op Amp for High Performance

Design Aids

Catalog (See Key)	Document Number	Title
AIC	* DA77-2	Design Aid of the LD120/LD121 4½ Digit DVM
	DA78-4	Build a Smoke Detector With the SM110 IC
M	* DA80-1	A Low Cost Regulator for Microprocessor Applications
	DA81-1	Logic Interfacing Made Easy with the DG308
	DA81-2	Logic Interfacing Made Easy with the DG308

Design Ideas

Catalog (See Key)	Document Number	Title
F	* DI71-1	The FET Constant Current Source
	DI71-4	Wideband Mixer-Preamplifier Using FETs
	DI71-5	A FET Frequency Doubler
	DI71-6	Using FETs in Selective VHF Amplifiers
	DI71-8	Using JFETs in Ultra-Wideband UHF Amplifiers
F	DI71-9	Wideband UHF Amplifier with High Performance FETs
F	* DI73-2	High Performance FETs in Low-Noise VHF Oscillators
	DI80-1	A 5 Watt, Parallel-Mode Crystal Oscillator

Technical Articles

Catalog (See Key)	Document Number	Title
	TA70-1	High Frequency Junction FET Characterization and Application
F	* TA70-2	FET Biasing
A	* TA73-1	Multiplexer Adds Efficiency to 32-Channel Telephone System
A	TA73-2	Designing with Monolithic FET Switches
	TA76-1	VMOS Power FETs in Your Next Broadband Driver

Publications Index (Cont'd)

Catalog (See Key)	Document Number	Title
		Technical Articles (Cont'd)
	*TA76-2	A New Technology: Application of VMOS Power FETs for High Frequency Communications
M	*TA82-1	The Autobias Amplifier
M	*TA82-2	MOSPOWER Semiconductor
M	*TA82-3	Bipolar and MOS Transistors: Emerging Partners for the 1980s
	TA83-1	Using Power MOSFETs as High-Efficiency Synchronous and Bridge Rectifiers in Switch-Mode Power Supplies.

Catalogs

Analog Switch & IC Product Data Book
Analog Switches and Their Applications
Small Signal FET Design Catalog
MOSPOWER Design Catalog
OEM Pricing with Cross Reference
RF MOSPOWER Short Form Catalog
Siliconix Short Form Selector Guide

Key

Catalogs

AIC = Analog Switch & IC Product Data Book
A = Analog Switches and Their Applications
F = Small Signal FET Design Catalog
M = MOSPOWER Design Catalog
*Available in bound catalog only.

Reprints & Reports

- Siliconix, Inc. Annual Report.
- Designing a VMOS 250 Watt Off-Line Inverter. David C. Hoffman, *Powercon* 3/78
- Designing with CODECs: Know Your A's and μ's. Thomas J. Mroz, *EDN* 5/76
- Log Data under μ Control, Gary Grandbois, *Electronic Design* 5/76
- Higher Power Ratings Extend VMOS FETs' Dominion, Arthur D. Evans, David C. Hoffman, Edwin S. Oxner, Walter Heinzer and Lee Shaeffer. *Electronics* 6/78
- CODEC has On-Chip Signaling for Phone Applications, Walter Heinzer and Steve Bolger, *Electronics* 6/7/79
- A Microprocessor Controlled VMOS Power Supply, David C. Hoffman
- Control Analog Signals with Voltage, Stephen Moore, *Electronic Design*, 1978
- Exploit VMOS FETs' Advantages to Drive Bipolar Power Transistors, F. Michael Barlage, *Powercon* 5/78
- Rely on IC Analog Switches for Fast Small-Signal Control, *EDN*, August 5, 20, Sept. 5, 1980
- Composite Op Amp Outperforms FET-Input ICs, *EDN*, May 27, 1981
- MOSFET's for Stepper-Motor Control, *Machine Design,* February 24, 1983

Books

Designing with Field-Effect Transistors, Edited by Arthur D. Evans. Available at your technical bookstore or write to Suite 26-1; McGraw-Hill Book Co., 1221 Avenue of the Americas, New York, NY 10020.

Power FETs and Their Applications, by Edwin S. Oxner. Available at your technical bookstore or write to: Mail Order Billing, Prentice-Hall, Inc., Tappan Road, Old Tappan, NJ 07675.

Glossary of Terms and Abbreviations

Siliconix

1. Upper case letters indicate DC voltages and currents.
2. Lower case letters indicate AC voltages and currents.
3. Subscripts can refer to the terminals used in the measurements, i.e., V_G = Gate Voltage; or simply help define the symbol, i.e., t_f = Fall Time, t_r = Rise Time.
4. Triple subscripts are used for terminal references only. The first subscript is the object terminal. The second subscript is the common terminal. The third gives the condition of the remaining terminal(s). S = Short, 0 = open and X = neither open nor short (refer to the test conditions). Example: BV_{GSS} = Breakdown Voltage from gate to source with the drain shorted to the source.

b_{fg} = Common-Gate Forward Susceptance

b_{fs} = Common-Source Forward Susceptance

b_{igs} = Common-Gate Input Susceptance

b_{iss} = Common-Source Input Susceptance

b_{ogs} = Common-Gate Output Susceptance

b_{oss} = Common-Source Output Susceptance

b_{rg} = Common-Gate Reverse Susceptance

b_{rs} = Common-Source Reverse Susceptance

BV_{DGO} = Drain-Gate Breakdown Voltage

BV_{DSS} = Drain-Source Breakdown Voltage

BV_{SDX} = Drain-Source Breakdown Voltage

BV_{G1SS} = Gate 1 to Source Breakdown Voltage

BV_{G2SS} = Gate 2 to Source Breakdown Voltage

BV_{GSS} = Gate-Source Breakdown Voltage

BV_{SDS} = Source-Drain Breakdown Voltage

BV_{SGO} = Source-Gate Breakdown Voltage

C_{db} = Drain-Body Capacitance

C_{dgo} = Drain-Gate Capacitance

C_{gb} = Gate-Body Capacitance

C_{gd} = Gate-Drain Capacitance

C_{gs} = Gate- Source Capacitance

C_{iss} = Common-Source Input Capacitance

C_{oss} = Common-Source Output Capacitance

C_{rss} = Common-Source Reverse Transfer Capacitance

C_{sb} = Source-Body Capacitance

C_{sd} = Source-Drain Capacitance

C_{sgo} = Source-Gate Capacitance

D = Drain

$\bar{e}_N$ = Equivalent Short Circuit Input Noise Voltage

f_m = Figure of Merit

G = Gate

g_{fg} = Common-Gate Forward Transconductance

g_{fs} = Common-Source Forward Transconductance

g_{fso} = Common-Source Forward Transconductance @ $V_{GS} = 0$

g_{fs1}/g_{fs2} = Common-Source Forward Transconductance Ratio

g_{ig} = Common-Gate Input Conductance

g_{is} = Common-Source Input Conductance

g_{og} = Common- Gate Output Conductance

g_{os} = Common-Source Output Conductance

g_{oss} = Common Source Output Conductance @ $V_{GS} = 0$

$g_{os1}-g_{os2}$ = Differential Output Conductance

G_{pg} = Common-Gate Power Gain

G_{ps} = Common-Source Power Gain

$I_{D(off)}$ = Drain Cutoff Current

$I_{D(on)}$ = Drain ON Current

I_{DGO} = Drain-Gate Leakage

Glossary of Terms and Abbreviations (Cont'd)

I_{DSS} = Saturation Drain Current

I_{DSS1}/I_{DSS2} = Saturation Drain Current Ratio

I_F = Forward Current

I_G = Gate Operating Current

I_{G1G2} = Gate to Gate Leakage Current

$|I_{G1}-I_{G2}|$ = Differential Gate Operating Currents

I_{GBS} = Gate to Body Leakage Current

$I_{G(f)}$ = Gate Forward Current

I_{GSS} = Gate Reverse Current

I_{G1SS} = Gate 1 to Source Leakage Current

I_{G2SS} = Gate 2 to Source Leakage Current

I_{G1SSR} = Gate 1 to Source Reverse Leakage Current

I_{G2SSR} = Gate 2 to Source Reverse Leakage Current

$\bar{i}_n$ = Equivalent Open-Circuit Noise Current

I_P = Pinch-Off Current

NF = Noise Figure

P_D = Continuous Power Dissipation

P_{OV} = Peak Operating Voltage

$r_{ds(on)}$ = Drain-Source ON Resistance

$r_{DS(on)}$ = Static Drain-Source ON Resistance

Re (Y_{fg}) = Common-Gate Forward Transconductance

Re (Y_{fs}) = Common-Source Forward Transconductance

Re (Y_{ig}) = Common-Gate Input Conductance

Re (Y_{is}) = Common-Gate Output Conductance

Re (Y_{os}) = Common-Source Output Conductance

Re (Y_{rg}) = Common-Gate Reverse Transconductance

Re (Y_{rs}) = Common-Source Reverse Transconductance

r_{GS} = Common-Source Input Resistance

S = Source

t_d = Delay Time

$t_{d(off)}$ = Turn-Off Delay Time

$t_{d(on)}$ = Turn-On Delay Time

t_f = Fall Time

T_j = Junction Temperature

t_{off} = Turn-Off Time

t_{on} = Turn-On Time

T_l = Lead Temperature

t_r = Rise Time

T_{stg} = Storage Temperature

V_B = Body Voltage

V_{BB} = Body Supply Voltage

V_D = Drain Voltage

V_{DD} = Drain Supply Voltage

$V_{DS(on)}$ = Drain-Source ON Voltage

V_G = Gate Voltage

V_{GG} = Gate Supply Voltage

V_{GS} = Gate-Source Voltage

$|V_{GS1}-V_{GS2}|$ = Differential Gate-Source Voltage

ΔV_{GS} = Differential Gate-Source Voltage

$\frac{\Delta|V_{gs1}-V_{gs2}|}{\Delta T}$ = Differential Gate-Source Voltage Change with Temperature

$V_{GS(f)}$ = Gate-Source Forward Voltage

$V_{GS(th)}$ = Gate Threshold Voltage

$V_{GS(off)}$ = Gate Source Cutoff Voltage

$V_{G1S(off)}$ = Gate 1 to Source Cutoff Voltage

$V_{G2S(off)}$ = Gate 2 to Source Cutoff Voltage

V_S = Source Voltage

V_{SS} = Source Supply Voltage

Z_d = Dynamic Impedance

Z_k = Knee AC Impedance

θ_I = Current Temperature Coefficient

θ_{J-A} = Junction to Ambient Thermal Resistance

θ_{J-C} = Junction to Case Thermal Resistance

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Introduction

Siliconix is committed to your future system designs. As a multinational semiconductor manufacturer, we offer some of the industry's broadest product lines. No one gives you more analog switch ICs and power FETs to choose from. Our multiple technologies include DMOS, VMOS, CMOS, PMOS, PMOS/bipolar and bipolar. And we are constantly advancing semi-custom state-of-the-art technology.

MOSPOWER FETs

MOSPOWER identifies the "up front" technology that places Siliconix among the leaders in power device development for the 1980's, and has helped make Siliconix *the Discovery Company*.

MOSPOWER is a generic name coined by Siliconix to identify not only Siliconix's expanding family of medium and high power MOSFETs, but *all* power MOSFETs. The name also covers the many technologies used in the manufacture of these power MOSFETs which have been identified by various trade names. Vertical DMOS (double-diffused MOS); metal-gate V-groove MOS for high-frequency; lateral DMOS technology for FET arrays — all are covered by this generic name: MOSPOWER.

RF POWER FETs

MOSPOWER shadow-mask vertical technology is used to manufacture the only true power MOS transistors. The technology enables their use as RF broadband amplifiers in the 2MHz to 200MHz region, providing output powers from 2 to 120 watts. Devices are available for 12.5V or 28V operation and in a variety of packages to suit different needs. They offer the advantages of high stage gain, low baseband noise and immunity to burn-out due to mismatch. The latest addition is the 35V single-side-band 2–30MHz series.

Analog Switch ICs

Siliconix JFET, MOSFET and Integrated Circuit (IC) technologies have been utilized to produce an extensive family of Analog Switch ICs. They are used in many high-reliability military and aerospace applications such as Mercury, Gemini, Apollo and Skylab manned space programs. The family of analog switch ICs includes monolithic multi-channel switches with integral drivers. Also high performance JFET switches packaged with IC drivers offering very low ON-resistance, fast switching, excellent frequency response (DG180 series); low spike feed-through, low leakage and high OFF-isolation (DG281); low cost, single or dual supply operation (DG308, DG211); low consumption CMOS switches (DG300 series) and multiplexers with up to 16 channels (DG506A). The recent addition to the range of analog switch ICs is the Plus-40 enhanced DG5040 series with guaranteed safe operation up to 44V, and DG243CJ, the dual make-before-break equivalent of the DG5043CJ.

LSI/Linear Circuits

Siliconix is an industry leader in telecommunications circuits, A/D conversion and micropower linears. The Company's LSI or linear ICs are incorporated in products ranging from sophisticated instrumentation to consumer smoke detectors. Advanced processing capabilities used in the manufacture of such ICs range from high and low voltage CMOS to bipolar-PMOS. High reliability processing procedures combined with volume production capabilities complement state-of-the-art products.

Introduction (Cont'd)

Telecommunications

Siliconix is a high-technology manufacturer of complex, highly specialized integrated circuits for the telecommunications industry. The current product lines use the CMOS process to satisfy the low power requirements of the telecom industry. Our Loop Disconnect Dialer Circuits offer subscribers push-button dialing privileges even with exchange systems presently tied to the rotary dial pulse timing.

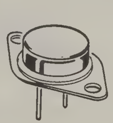
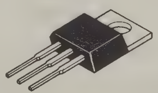
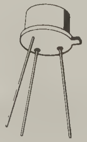
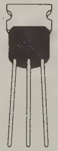
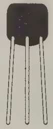
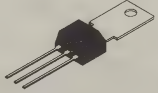
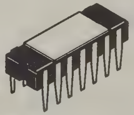
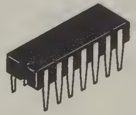
High-Reliability Devices

Siliconix's capability in providing high-reliability devices to meet stringent military or aerospace applications is amply demonstrated by the Company's qualifications as a supplier for important European projects that include Ariane, Concorde, European Airbus, the Alpha Jet and Tornado Aircraft, also Apollo, Viking and Voyager space projects.

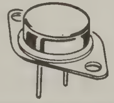
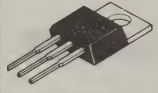
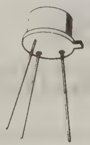
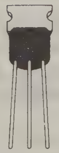
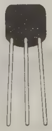
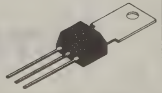
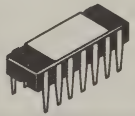
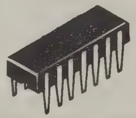
Siliconix has a number of standard Hi-Rel screening options that can be applied to standard products. These options include screening to BS9000 for analog switches and CECC standards for FETs, also MIL-STD-750 for discrete FETs. In addition, Siliconix offers certain JEDEC-registered FETs with JAN, JANTX and JANTXV processing, as well as an increasing number of QPL-listed analog switches. Special additional inspections and controls can be met and Siliconix can supply SEM-qualified products to meet individual customer requirements.

MOSPOWER
Prime Products Selector Guide

* 200°C RATING

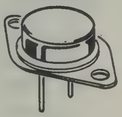
Packages:								
BV$_{DSS}$ (Volts)	**TO-3**	**TO-220**	**TO-39**	**TO-237**	**TO-92**	**TO-202**	**Quad Side Braze**	**Quad Plastic**
600-650	VNT008A 6A, 1.5Ω, 650V	VNT008D 6A, 1.5Ω, 650V						
450-500	VNP006A 20A, 0.3Ω, 500V	IRF840 8A, 0.85Ω, 500V						
	IRF450 13A, 0.4Ω, 500V	VN5001D/IRF830 4.5A, 1.5Ω, 500V						
	IRF440 8A, 0.85Ω, 500V	IRF820 2.5A, 3Ω, 500V						
	VNP002A* 6.5A, 1.5Ω, 500V							
	VN5001A/IRF430 4.5A, 1.5Ω, 500V							
	IRF420 2.5A, 3Ω, 500V							
350-400	VNM005A 25A, 0.2Ω, 400V	IRF740 10A, 0.55Ω, 400V						
	IRF350 15A, 0.3Ω, 400V	VN4000D/IRF730 5.5A, 1.0Ω, 400V						
	IRF340 10A, 0.55Ω, 400V	IRF720 3A, 1,8Ω, 400V						
	VNM001A* 8A, 1.0Ω, 400V							
	VN4000A/IRF330 5.5A, 1.0Ω, 400V							

MOSPOWER Prime Products Selector Guide

Packages:								
BV_{DSS} (Volts)	**TO-3**	**TO-220**	**TO-39**	**TO-237**	**TO-92**	**TO-202**	**Quad Side Braze**	**Quad Plastic**
120-240	VNJ004A 45A, 0.06Ω, 200V	IRF640 18A, 0.18Ω, 200V	VN2406B 0.8A, 6Ω, 240V	VN2406M 0.3A, 6Ω, 240V	VN2406L 0.21A, 6Ω, 240V			
	IRF250 30A, 0.085Ω, 200V	IRF630 9A, 0.4Ω, 200V		VN2410M 0.25A, 10Ω, 240V	VN2410L 0.16A, 10Ω, 240V			
	IRF240 18A, 0.18Ω, 200V	IRF620 5A, 0.8Ω, 200V						
	IRF230 9A, 0.4Ω, 200V	VN2406D 1.4A, 6Ω 240V						
	IRF220 5A, 0.8Ω, 200V							
60-100	VNE003A 60A, 0.035Ω, 100V	IRF540 27A, 0.085Ω, 100V	IRFF130 8A, 0.18Ω, 100V	VP1008M 0.37A, 5Ω, - 100V	VP1008L 0.23A, 5Ω, - 100V	VN88AF 1.5A, 4Ω, 80V	VQ1006P 0.40A, 4.5Ω, 90V	VQ1006J 0.40A, 4.5Ω, 90V
	IRF150 40A, 0.055Ω, 100V	VN1000D/IRF530 12A, 0.18Ω, 100V	IRFF120 6A, 0.30Ω, 100V	VN0808M 0.35A, 4Ω, 80V	VN0610L * 0.2A, 5Ω, 60V	VN80AF 1.3A, 5Ω, 80V	VQ2006P 0.41A, 5Ω, - 90V	VQ2006J 0.41A, 5Ω, - 90V
	IRF140 27A, 0.085Ω, 100V	IRF520 8A, 0.30Ω, 100V	VNE011B 4A, 0.5Ω, 100V	VN0606M 0.4A, 3Ω, 60V	VN2222L * 0.15A, 7.5Ω, 60V	VN66AF 1.7A, 3Ω, 60V	VQ1004P 0.46A, 3.5Ω, 60V	VQ1004J 0.46A, 3.5Ω, 60V
	VN1000A/IRF130 12A, 0.18Ω, 100V	VN88AD 1.7A, 4Ω, 80V	VP1008B 0.9A, 5Ω, - 100V	VN10KM 0.3A, 5Ω, 60V		VN67AF 1.6A, 3.5Ω, 60V	VQ1000P 0.225A, 5.5Ω, 60V	VQ1000J 0.225A, 5.5Ω, 60V
	IRF120 8A, 0.3Ω, 100V	VN0600D 16A, 0.12Ω, 60V	2N6661 0.9A, 4Ω, 90V	VN10LM * 0.3A, 5Ω, 60V			VQ2004P 0.41A, 5Ω, - 60V	VQ2004J 0.41A, 5Ω, - 60V
	VN0600A 16A, 0.12Ω, 60V	VN66AD 1.9A, 3Ω, 60V	2N6660 1.1A, 3Ω, 60V	VN2222LM 0.25A, 7.5Ω, 60V				
30-40	VN0400A 16A 0.12Ω, 40V	VN0400D 16A, 0.12Ω, 40V	2N6659 1.4A,, 18Ω, 35V	VN0300M 0.7A, 12Ω, 30V		VN46AF 1.6A, 3Ω, 40V	VQ1001P 0.85A, 1.0Ω, 30V	VQ1001J 0.85A, 1.0Ω, 30V
	2N6656 2A, 1.8Ω, 35V	VN0300D 2.5A, 1.5Ω, 30V	VP0300B 1.3A, 25Ω, - 30V	VP0300M 0.48A, 2.5Ω, - 30V		VN40AF 1.3A, 5Ω, 40V	VQ2001P 0.60A, 2Ω, -30V	VQ2001J 0.60A, 2Ω, - 30V
Specialty Products (N- and P-Channel Quad Arrays)							VQ3001P ± 30V, 3Ω Total	VQ3001J ± 30V, 3Ω Total
							VQ7254P ± 20V, 3Ω Total	VQ7254J ± 20V, 3Ω Total

MOSPOWER Selector Guide

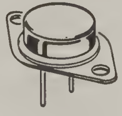
N-Channel MOSPOWER

Device	Breakdown Voltage (Volts)	$r_{DS(on)}$ (Ohms)	I_D Continuous (Amps)	Power Dissipation (Watts)	Part Number
 TO-3	650	1.5	6.0	125	VNT008A
	650	2.0	5.0	125	VNT009A
	600	1.5	6.0	125	VNS008A
	600	2.0	5.0	125	VNS009A
	500	0.3	20.0	250	VNP006A
	500	0.4	13.0	150	IRF450
	500	0.5	12.0	150	IRF452
	500	0.85	8.0	125	IRF440
	500	1.10	7.0	125	IRF440
	500	1.5	6.5	175	VNP002A*
	500	1.5	4.5	100	VN5001A
	500	1.5	4.5	75	IRF430
	500	2.0	4.0	100	VN5002A
	500	2.0	4.0	75	IRF432
	500	3.0	2.5	40	IRF420
	500	4.0	2.0	40	IRF422
	450	0.3	20.0	250	VNN006A
	450	0.4	13.0	150	IRF451
	450	0.5	12.0	150	IRF453
	450	0.85	8.0	125	IRF441
	450	1.10	7.0	125	IRF443
	450	1.5	6.5	175	VNN002A*
	450	1.5	4.5	100	VN4501A
	450	1.5	4.5	75	IRF431
	450	2.0	4.0	100	VN4502A
	450	2.0	4.0	75	IRF433
	450	3.0	2.5	40	IRF421
	450	4.0	2.0	40	IRF423
	400	0.2	25.0	250	VNM005A
	400	0.3	15.0	150	IRF350
	400	0.4	13.0	150	IRF352
	400	0.55	10.0	125	IRF340
	400	0.80	8.0	125	IRF342
	400	1.0	8.0	175	VNM001A*
	400	1.0	6.0	125	VN4000A
	400	1.0	5.5	75	IRF330
	400	1.5	5.0	125	VN4001A
	400	1.5	4.5	75	IRF332
	400	1.8	3.0	40	IRF320
	400	2.5	2.5	40	IRF322
	350	0.2	25.0	250	VNL005A
	350	0.3	15.0	150	IRF351
	350	0.4	13.0	150	IRF353
	350	0.55	10.0	125	IRF341
	350	0.80	8.0	125	IRF343
	350	1.0	8.0	175	VNL001A*
	350	1.0	6.0	125	VN3500A
	350	1.0	5.5	75	IRF331
	350	1.5	5.0	125	VN3501A
	350	1.5	4.5	75	IRF333
	350	1.8	3.0	40	IRF321
	350	2.5	2.5	40	IRF323
	200	0.06	45.0	250	VNJ004A
	200	0.085	30.0	150	IRF250
	200	0.12	25.0	150	IRF252
	200	0.18	18.0	125	IRF240

* 200°C Rating

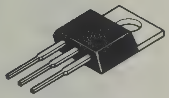
MOSPOWER Selector Guide (Cont'd)

N-Channel MOSPOWER (Cont'd)

Device	Breakdown Voltage (Volts)	$r_{DS(on)}$ (Ohms)	I_D Continuous (Amps)	Power Dissipation (Watts)	Part Number
 TO-3	200	0.22	16.0	125	IRF242
	200	0.4	9.0	75	IRF230
	200	0.6	8.0	75	IRF232
	200	0.8	5.0	40	IRF220
	200	1.2	4.0	40	IRF222
	150	0.06	45.0	250	VNG004A
	150	0.085	30.0	150	IRF251
	150	0.12	25.0	150	IRF253
	150	0.18	18.0	125	IRF241
	150	0.22	16.0	125	IRF243
	150	0.4	9.0	75	IRF231
	150	0.6	8.0	75	IRF233
	150	0.8	5.0	40	IRF221
	150	1.2	4.0	40	IRF223
	120	0.18	14.0	75	VN1200A
	120	0.25	12.0	100	VN1201A
	100	0.035	60.0	250	VNE003A
	100	0.055	40.0	150	IRF150
	100	0.08	33.0	150	IRF152
	100	0.085	27.0	125	IRF140
	100	0.11	24.0	125	IRF142
	100	0.18	14.0	100	VN1000A
	100	0.18	14.0	75	IRF130
	100	0.25	12.0	100	VN1001A
	100	0.25	12.0	75	IRF132
	100	0.3	8.0	40	IRF120
	100	0.4	7.0	40	IRF122
	90	4.0	1.9	25	2N6658
	90	4.5	1.8	25	VN99AA
	90	5.0	1.7	25	VN90AA
	80	0.18	14.0	100	VN0800A
	80	0.25	12.0	100	VN0801A
	60	0.035	60.0	250	VNC003A
	60	0.055	40.0	150	IRF151
	60	0.08	33.0	150	IRF153
	60	0.085	27.0	125	IRF141
	60	0.11	24.0	125	IRF143
	60	0.12	18.0	100	VN0600A
	60	0.15	16.0	100	VN0601A
	60	0.18	14.0	75	IRF131
	60	0.25	12.0	75	IRF133
	60	0.3	8.0	40	IRF121
	60	0.4	10.0	80	VN64GA
	60	0.4	7.0	40	IRF123
	60	3.0	2.0	25	2N6657
	60	3.5	2.0	25	VN67AA
	40	0.12	18.0	100	VN0400A
	40	0.15	16.0	100	VN0401A
	35	1.8	2.0	25	2N6656
	35	2.5	2.0	25	VN35AA

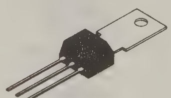
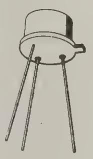
MOSPOWER Selector Guide (Cont'd)

N-Channel MOSPOWER (Cont'd)

Device	Breakdown Voltage (Volts)	$r_{DS(on)}$ (Ohms)	I_D Continuous (Amps)	Power Dissipation (Watts)	Part Number
 TO-220AB	650	1.5	6.0	125	VNT008D
	650	2.0	5.0	125	VNT009D
	600	1.5	6.0	125	VNS008D
	600	2.0	5.0	125	VNS009D
	500	0.85	8.0	125	IRF840
	500	1.10	7.0	125	IRF842
	500	1.5	4.5	75	VN5001D
	500	1.5	4.5	75	IRF830
	500	2.0	4.0	75	VN5002D
	500	2.0	4.0	75	IRF832
	500	3.0	2.5	40	IRF820
	500	4.0	2.0	40	IRF822
	450	0.85	8.0	125	IRF841
	450	1.10	7.0	125	IRF843
	450	1.5	4.5	75	VN4501D
	450	1.5	4.5	75	IRF831
	450	2.0	4.0	75	VN4502D
	450	2.0	4.0	75	IRF833
	450	3.0	2.5	40	IRF821
	450	4.0	2.0	40	IRF823
	400	0.55	10.0	125	IRF740
	400	0.80	8.0	125	IRF742
	400	1.0	6.0	75	VN4000D
	400	1.0	5.5	75	IRF730
	400	1.5	5.0	75	VN4001D
	400	1.5	4.5	75	IRF732
	400	1.8	3.0	40	IRF720
	400	2.5	2.5	40	IRF722
	350	0.55	10.0	125	IRF741
	350	0.80	8.0	125	IRF743
	350	1.0	6.0	75	VN3500D
	350	1.0	5.5	75	IRF731
	350	1.5	5.0	75	VN3501D
	350	1.5	4.5	75	IRF733
	350	1.8	3.0	40	IRF721
	350	2.5	2.5	40	IRF723
	240	6.0	1.4	20	VN2406D
	200	0.18	18.0	125	IRF640
	200	0.22	16.0	125	IRF642
	200	0.4	9.0	75	IRF630
	200	0.6	8.0	75	IRF632
	200	0.8	5.0	40	IRF620
	200	1.2	4.0	40	IRF622
	170	6.0	1.4	20	VN1706D
	150	0.18	18.0	125	IRF641
	150	0.22	16.0	125	IRF643
	150	0.4	9.0	75	IRF631
	150	0.6	8.0	75	IRF633
	150	0.8	5.0	40	IRF621
	150	1.2	4.0	40	IRF623
	120	0.18	14.0	75	VN1200D
	120	0.25	12.0	75	VN1201D
	120	6.0	1.4	20	VN1206D

MOSPOWER Selector Guide (Cont'd)

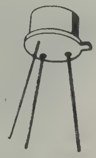
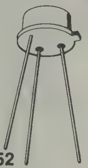
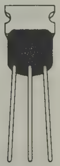
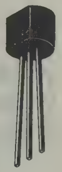
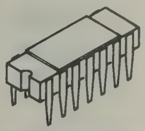
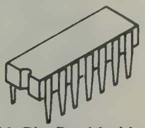
N-Channel MOSPOWER (Cont'd)

Device	Breakdown Voltage (Volts)	$r_{DS(on)}$ (Ohms)	I_D Continuous (Amps)	Power Dissipation (Watts)	Part Number
TO-220AB	100	0.085	27.0	125	IRF540
	100	0.11	24.0	125	IRF542
	100	0.18	14.0	75	VN1000D
	100	0.18	14.0	75	IRF530
	100	0.25	12.0	75	VN1001D
	100	0.25	12.0	75	IRF532
	100	0.30	8.0	40	IRF520
	100	0.40	7.0	40	IRF522
	80	0.18	14.0	75	VN0800D
	80	0.25	12.0	75	VN0801D
	80	4.0	1.7	20	VN88AD
	80	4.5	1.6	20	VN89AD
	60	0.085	27.0	125	IRF541
	60	0.11	24.0	125	IRF543
	60	0.12	18.0	75	VN0600D
	60	0.15	16.0	75	VN0601D
	60	0.18	14.0	75	IRF531
	60	0.25	12.0	75	IRF533
	60	0.30	8.0	40	IRF521
	60	0.40	7.0	40	IRF523
	60	3.0	1.9	20	VN66AD
	60	3.5	1.8	20	VN67AD
	40	0.12	18.0	75	VN0400D
	40	0.15	16.0	75	VN0401D
	40	3.0	1.9	20	VN46AD
	40	5.0	1.5	20	VN40AD
	30	1.2	2.5	20	VN0300D
 **TO-202AA**	80	4.0	1.5	15	VN88AF
	80	4.5	1.4	15	VN89AF
	80	5.0	1.3	15	VN80AF
	60	3.0	1.7	15	VN66AF
	60	3.5	1.6	15	VN67AF
	40	3.0	1.6	15	VN46AF
	40	5.0	1.3	15	VN40AF
 **TO-39**	240	6.0	0.8	6.25	VN2406B
	170	6.0	0.8	6.25	VN1706B
	120	6.0	0.8	6.25	VN1206B
	100	0.18	8.0	25	IRFF130
	100	0.25	7.0	25	IRFF132
	100	0.3	6.0	20	IRFF120
	100	0.4	5.0	20	IRFF122
	100	0.5	4.0	15	VNE010B*
	100	0.5	4.0	15	VNE011B
	90	4.0	0.9	6.25	2N6661
	90	4.5	0.9	6.25	VN99AB
	90	5.0	0.8	6.25	VN90AB
	80	0.5	4.0	15	VND010B*
	80	0.5	4.0	15	VND011B

* Low $V_{GS(TH)}$

MOSPOWER Selector Guide (Continued)

N-Channel MOSPOWER (Continued)

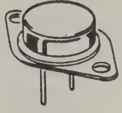
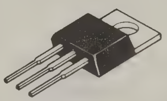
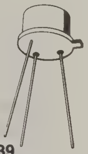
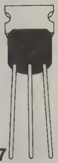
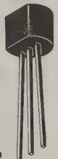
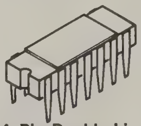
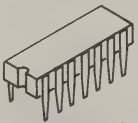
Device	Breakdown Voltage (Volts)	$r_{DS(on)}$ (Ohms)	I_D Continuous (Amps)	Power Dissipation (Watts)	Part Number
 TO-39	60	0.18	8.0	25	IRF131
	60	0.25	7.0	25	IRF133
	60	0.3	6.0	20	IRFF121
	60	0.4	5.0	20	IRFF123
	60	0.5	4.0	15	VNC010B*
	60	0.5	4.0	15	VNC011B
	60	3.0	1.1	6.25	2N6660
	60	3.5	1.0	6.25	VN67AB
	35	1.8	1.4	6.25	2N6660
	35	2.5	1.2	6.25	VN35AB
 TO-52	60	5.0	0.2	0.315	VN10KE
	60	5.0	0.2	0.315	VN10LE
 TO-237	240	6.0	0.3	1.0	VN2406M
	240	10.0	0.25	1.0	VN2410M
	170	6.0	0.3	1.0	VN1706M
	170	10.0	0.25	1.0	VN1710M
	120	6.0	0.3	1.0	VN1206M
	120	10.0	0.25	1.0	VN1210M
	80	4.0	0.35	1.0	VN0808M
	60	3.0	0.4	1.0	VN0606M
	60	5.0	0.3	1.0	VN10KM**
	60	5.0	0.3	1.0	VN10LM
	60	7.5	0.25	1.0	VN2222KM**
	60	7.5	0.25	1.0	VN2222LM
	30	1.2	0.7	1.0	VN0300M
 TO-92	240	6.0	0.21	0.4	VN2406L
	240	10.0	0.16	0.4	VN2410L
	170	6.0	0.21	0.4	VN1706L
	170	10.0	0.16	0.4	VN1710L
	120	6.0	0.21	0.4	VN1206L**
	120	10.0	0.16	0.4	VN1210L**
	60	5.0	0.2	0.4	VN0610L
	60	7.5	0.15	0.4	VN2222L
	30	1.2	0.44	0.4	VN0300L
 14-Pin Dual-In-Line (Side Braze)	90	4.5	0.40	1.3	VQ1006P
	60	3.5	0.46	1.3	VQ1004P
	60	5.5	0.225	0.5	VQ1000P
	30	1.0	0.85	1.3	VQ1001P
 14-Pin Dual-In-Line (Plastic)	90	4.5	0.40	1.3	VQ1006J
	60	3.5	0.46	1.3	VQ1004J
	60	5.5	0.225	0.5	VQ1000J
	30	1.0	0.85	1.3	VQ1001J

* Low $V_{GS(TH)}$

** Zener Protected Gate

MOSPOWER Selector Guide (Continued)

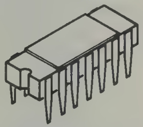
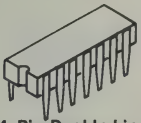
P-Channel MOSPOWER

Device	Breakdown Voltage (Volts)	rDS(on) (Ohms)	ID Continuous (Amps)	Power Dissipation (Watts)	Part Number
 TO-3	−100	0.3	12.0	75	IRF9130**
	−100	0.4	10.0	75	IRF9132**
	−60	0.3	12.0	75	IRF9131**
	−60	0.4	10.0	75	IRF9133**
 TO-220AB	−100		12.0	75	IRF9530**
	−100		10.0	75	IRF9532**
	−100	0.6	6.0	40	IRF9520**
	−100	0.8	5.0	40	IRF9522**
	−60		12.0	75	IRF9531**
	−60		10.0	75	IRF9533**
	−60	0.6	6.0	40	IRF9521**
	−60	0.8	5.0	40	IRF9523**
 TO-39	−100	5.0	0.9	6.25	VP1008B
	−80	5.0	0.9	6.25	VP0808B
	−30	2.5	1.3	6.25	VP0300B
 TO-237	−100	5.0	0.37	1.0	VP1008M
	−80	5.0	0.37	1.0	VP0808M
	−30	2.5	0.48	1.0	VP0300M
 TO-92	−100	5.0	0.37	0.4	VP1008L
	−80	5.0	0.37	0.4	VP0808L
	−30	2.5	0.48	1.0	VP0300L
 14-Pin Dual-In-Line (Side Braze)	−90	5.0	0.600	1.3	VQ2006P
	−60	5.0	0.600	1.3	VQ2004P
	−30	2.0	0.600	1.3	VQ2001P
 14-Pin Dual-In-Line (Plastic)	−90	5.0	0.600	1.3	VQ2006J
	−60	5.0	0.600	1.3	VQ2004J
	−30	2.0	0.600	1.3	VQ2001J

** Available 4th Qtr. 1983

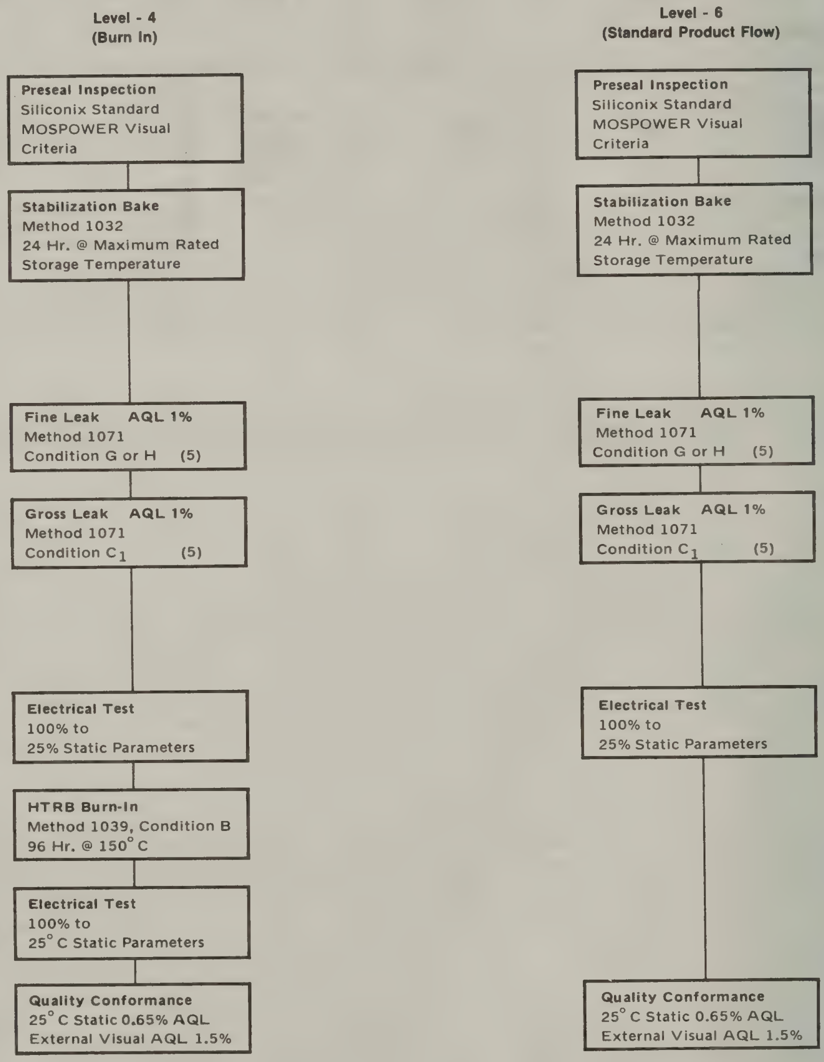
MOSPOWER Selector Guide (Cont'd)

N- and P-Channel Quad MOSPOWER

Device	Breakdown Voltage (Volts)	$r_{DS(on)}$ (Ohms)	I_D Continuous (Amps)	Power Dissipation (Watts)	Part Number
 14-Pin Dual-In-Line (Side Braze)	30	3.0**	N- 0.600 P- 0.850	1.3	VQ3001P
	20	3.0**	N- 0.600 P- 0.850	1.3	VQ7254P
 14-Pin Dual-In-Line (Plastic)	30	3.0**	N- 0.600 P- 0.850	1.3	VQ3001J
	20	3.0**	N- 0.600 P- 0.850	1.3	VQ7254J

**Total (N + P)

MOSPOWER
Commercial/Industrial Process Flow(7)



Level - 4
(Burn In)

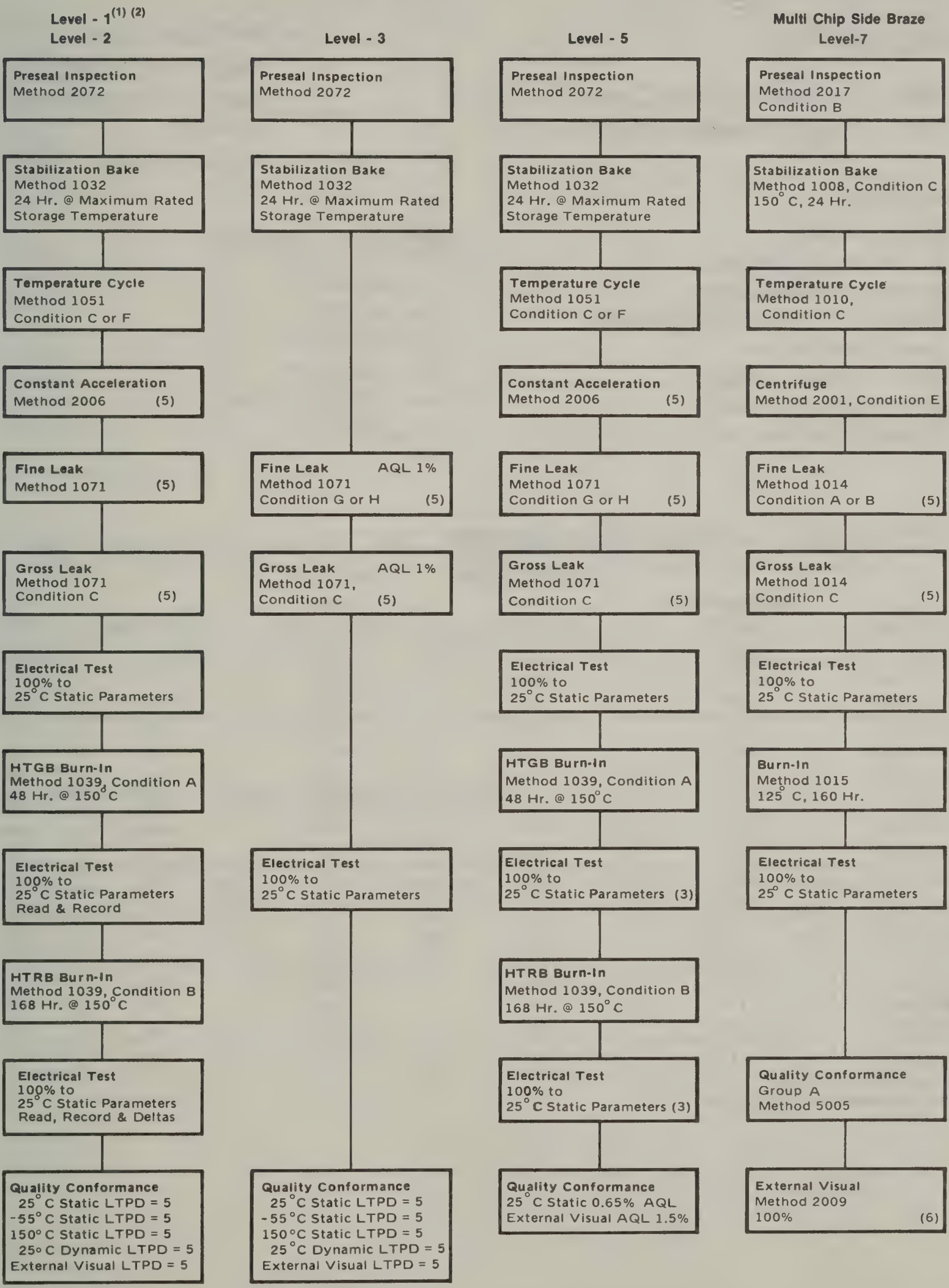
- **Preseal Inspection** Siliconix Standard MOSPOWER Visual Criteria
- **Stabilization Bake** Method 1032 24 Hr. @ Maximum Rated Storage Temperature
- **Fine Leak** **AQL 1%** Method 1071 Condition G or H (5)
- **Gross Leak** **AQL 1%** Method 1071 Condition C_1 (5)
- **Electrical Test** 100% to 25% Static Parameters
- **HTRB Burn-In** Method 1039, Condition B 96 Hr. @ 150° C
- **Electrical Test** 100% to 25° C Static Parameters
- **Quality Conformance** 25° C Static 0.65% AQL External Visual AQL 1.5%

Level - 6
(Standard Product Flow)

- **Preseal Inspection** Siliconix Standard MOSPOWER Visual Criteria
- **Stabilization Bake** Method 1032 24 Hr. @ Maximum Rated Storage Temperature
- **Fine Leak** **AQL 1%** Method 1071 Condition G or H (5)
- **Gross Leak** **AQL 1%** Method 1071 Condition C_1 (5)
- **Electrical Test** 100% to 25% Static Parameters
- **Quality Conformance** 25° C Static 0.65% AQL External Visual AQL 1.5%

NOTES:
(1) Level – 1: U.S. Build, U.S. Test.
(2) Level – 2: Overseas Build, U.S. Test (Screening & QCI).
(3) No Read & Record, No Deltas.
(4) Group B and C testing is additional.
(5) Hermetic Only.
(6) Physical Dimensions Excluded. The latest revision of MIL-STD-883 is applicable.
(7) Levels 1 thru 6: Latest revision of MIL-STD-750 is applicable.
(8) Level 7: Latest revision of MIL-STD-883 is applicable.

MOSPOWER
Military/Hi-Rel Process Flow(4) (7) (8)



Level - 1[1] [2] Level - 2	Level - 3	Level - 5	Multi Chip Side Braze Level-7
Preseal Inspection Method 2072	**Preseal Inspection** Method 2072	**Preseal Inspection** Method 2072	**Preseal Inspection** Method 2017 Condition B
Stabilization Bake Method 1032 24 Hr. @ Maximum Rated Storage Temperature	**Stabilization Bake** Method 1032 24 Hr. @ Maximum Rated Storage Temperature	**Stabilization Bake** Method 1032 24 Hr. @ Maximum Rated Storage Temperature	**Stabilization Bake** Method 1008, Condition C 150° C, 24 Hr.
Temperature Cycle Method 1051 Condition C or F		**Temperature Cycle** Method 1051 Condition C or F	**Temperature Cycle** Method 1010, Condition C
Constant Acceleration Method 2006 (5)		**Constant Acceleration** Method 2006 (5)	**Centrifuge** Method 2001, Condition E
Fine Leak Method 1071 (5)	**Fine Leak** AQL 1% Method 1071 Condition G or H (5)	**Fine Leak** Method 1071 Condition G or H (5)	**Fine Leak** Method 1014 Condition A or B (5)
Gross Leak Method 1071 Condition C (5)	**Gross Leak** AQL 1% Method 1071, Condition C (5)	**Gross Leak** Method 1071 Condition C (5)	**Gross Leak** Method 1014 Condition C (5)
Electrical Test 100% to 25° C Static Parameters		**Electrical Test** 100% to 25° C Static Parameters	**Electrical Test** 100% to 25° C Static Parameters
HTGB Burn-In Method 1039, Condition A 48 Hr. @ 150° C		**HTGB Burn-In** Method 1039, Condition A 48 Hr. @ 150° C	**Burn-In** Method 1015 125° C, 160 Hr.
Electrical Test 100% to 25° C Static Parameters Read & Record	**Electrical Test** 100% to 25° C Static Parameters	**Electrical Test** 100% to 25° C Static Parameters (3)	**Electrical Test** 100% to 25° C Static Parameters
HTRB Burn-In Method 1039, Condition B 168 Hr. @ 150° C		**HTRB Burn-In** Method 1039, Condition B 168 Hr. @ 150° C	
Electrical Test 100% to 25° C Static Parameters Read, Record & Deltas		**Electrical Test** 100% to 25° C Static Parameters (3)	**Quality Conformance** Group A Method 5005
Quality Conformance 25° C Static LTPD = 5 -55° C Static LTPD = 5 150° C Static LTPD = 5 25° C Dynamic LTPD = 5 External Visual LTPD = 5	**Quality Conformance** 25° C Static LTPD = 5 -55° C Static LTPD = 5 150° C Static LTPD = 5 25° C Dynamic LTPD = 5 External Visual LTPD = 5	**Quality Conformance** 25° C Static 0.65% AQL External Visual AQL 1.5%	**External Visual** Method 2009 100% (6)

NOTES:
(1) Level — 1: U.S. Build, U.S. Test.
(2) Level — 2: Overseas Build, U.S. Test (Screening & QCI).
(3) No Read & Record, No Deltas.
(4) Group B and C testing is additional.
(5) Hermetic Only.
(6) Physical Dimensions Excluded. The latest revision of MIL-STD-883 is applicable.
(7) Levels 1 thru 6: Latest revision of MIL-STD-750 is applicable.
(8) Level 7: Latest revision of MIL-STD-883 is applicable.

RF Power FETs Selector Guide

n-channel enhancement-mode RF Power FETs designed for. . .

HF/VHF/UHF Amplifiers Class A, B, C, D or E. High Dynamic Range Amp

BENEFITS

- Infinite VSWR
- No Thermal Runaway
- Broadband Capability
- Class A, B C, D, or E Operation
- Low Noise Figure
- High Dynamic Range
- Simple Bias Circuitry
- S-Parameter Design

ORDERING INFORMATION

DX XX XXX X

X — Package Code
XXX — Power Output (Watts)
XX — Suggested Operating Voltage
DX — Product Code

PACKAGE CODES

S = 380SOEF
T = 500JOF
U = 500SOEF
V = Push-Pull
W = C-220 Standard
Z = 280SOE

12.5 Volt DC — 300 MHz Series

Part Number	Test Frequency* (MHz)	Rated Power Out (Watts) @ 12.5 V_{DC}	Min. Gain (dB) 12.5 V, 175 MHz	Min. BV_{DSS}	θJc (°C/W)
DV1202S	175	2.0	10.0	45	17.6
DV1202W	175	2.0	10.0	45	14.1
DV1202Z	175	2.0	10.0	45	17.6
DV1205S	175	5.0	10.0	45	8.8
DV1205W	175	5.0	10.0	45	7.0
DV1205Z	175	5.0	10.0	45	8.8
DV1210S	175	10.0	10.0	45	4.4
DV1210W	175	10.0	10.0	45	3.5
DV1210Z	175	10.0	10.0	45	4.4
DV1220S	175	20.0	10.0	45	2.2
DV1220W	175	20.0	10.0	45	1.8
DV1230T	175	30.0	9.5	45	1.5
DV1230W	175	30.0	9.3	45	1.2
DV1240T	175	40.0	9.0	45	1.1
DV1240U	175	40.0	8.6	45	1.1
DV1240W	175	40.0	9.0	45	0.9
DV1260T	175	60.0	8.0	45	0.73

*All parts tested at 20:1 VSWR.
Note: See application notes AN80-4, AN80-6.

RF Power FETs Selector Guide (Cont'd)

28 Volt DC — 300 MHz Series

Part Number	Test Frequency* (MHz)	Rated Power Out (Watts) @ 28 V_{DC}	Min. Gain (dB) 28 V, 175 MHz	Min. BV_{DSS}	θJc (°C/W)
DV2805S	175	5	10	80	17.6
DV2805W	175	5	10	80	14.1
DV2805Z	175	5	10	80	17.6
DV2810S	175	10	10	80	8.8
DV2810W	175	10	10	80	7.0
DV2810Z	175	10	10	80	8.8
DV2820S	175	20	10	80	4.4
DV2820W	175	20	10	80	3.5
DV2820Z	175	20	10	80	4.4
DV2840S	175	40	10	80	2.2
DV2840W	175	40	10	80	1.8
DV2880T	175	80	10	80	1.1
DV2880U	175	80	10	80	1.1
DV2880W	175	80	10	80	0.9
DV28120T	175	120	10	80	0.73
DV28120U	175	120	9	80	0.73
VMP4	175	20	10	60	4.4

*All parts tested at 20:1 VSWR.

28 Volt Push-Pull — DC-300 MHz Series

Part Number	Test Frequency (MHz)	Test Voltage (V_{DS})	P_{in} (Max.) (Watts)	P_{out} @ 28 V (Watts)	G_{PS} (Min.) Power Gain (dB)	θJc Thermal Impedance (°C/W)
DV2880V	175	28	8	80	10	1.1
DV28120V	175	28	12	120	10	0.73

100 Volt DC — 300 MHz Series

Part Number	Test Frequency* (MHz)	Rated Power Out (Watts) @ 12.5 V_{DC}	Min. Gain (dB) 12.5 V, 175 MHz	Min. BV_{DSS}	θJc (°C/W)
DVD030S	175	25	13	220	4.40
DVD150T	175	120	10	220	0.73

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Analog Switches Selector Guide

Application	Feature of Application	Important Parameters	Major Tradeoffs	Suggested Switches
Battery Operated or Battery Back-Up Supply	1) Low Power	Low Supply Current		**CMOS DG304-DG308, DG304A, DG307A, DG309** DG300-DG303, DG381-DG390, DG300A-DG303A, DG381A-DG390A
	2) Minimum Number of Power Supplies	Only One or Two Supplies Needed		**CMOS DG300-DG308A, DG300A-DG307A, DG309** (Can Also Be Used As Single Supply) CMOS DG211, DG200A, DG201A, DG202, DG212 (For MUX: DG506-DG509, DG506A-DG509A, DG528, DG529)
	3) Low Standby Power	Low Standby Current		**CMOS DG304-DG308A, DG211, DG304A-DG307A, DG309, DG212**
Audio	1) Low Signal Distortion	Low $r_{DS(on)}$; Constant $r_{DS(on)}$	JFET is Constant, $r_{DS(on)}$; Signal Range Limited Toward Negative Supply; CMOS Slight $r_{DS(on)}$ Variation, Full Signal Range	**JFET DG180-DG191** CMOS DG300-DG308A, DG381-DG390, DG300A-DG307A, DG309, DG381A-DG390A, DG5040-DG5045 DG243 (Make-Before-Break)
	2) Low Noise (Channel)	Low $r_{DS(on)}$		CMOS DG300-DG308A, DG381-DG390, DG300A-DG307A, DG309, DG381A-DG390A, DG5040-DG5045, DG243 JFET DG180-DG191
	3) Wide Signal Range	±15V Signal Range		**CMOS DG300-DG308, DG381-DG390, DG300A-DG307A, DG309, DG381A-DG390A, DG5040-DG5045, DG243** CMOS DG200, DG200A, DG201, DG201A, DG202, DG211, DG212 (MUX: DG506-DG509, DG506A-DG509A, DG528, DG529)
		Signal Range is From the Positive Supply to Above the Negative Supply	Higher $r_{DS(on)}$ (Must Stay Above Negative Supply By 5V to 7.5V)	**JFET (75Ω) DG182, DG185, DG188, DG191** (10Ω, 30Ω) Remainder of DG181-DG190 Family
	4) Large Dynamic Range	Wide Signal Range and Low Thermocouple Noise		**CMOS DG304-DG308A, DG304A-DG307A, DG309** DG300-DG303, DG381-DG390, DG211, DG300A-DG303A, DG381A-DG390A, DG212
Video (High Frequency)	1) High OFF Impedance, Small Feedthrough of Signal	High OFF Isolation	Higher $r_{DS(on)}$	**JFET (30Ω, 75Ω) DG181, DG182, DG184, DG185, DG187, DG188, DG190, DG191** CMOS DG200, DG201, DG211, DG200A, DG201A, DG202, DG212 CMOS DG300-DG308A, DG381-DG390, DG300A-DG307A, DG309, DG381A-DG390A, DG5040-DG5045, DG243
	2) Good Impedance Matching, Minimum Signal Drop Across Switch	Low $r_{DS(on)}$	Lower OFF Isolation	**JFET (10Ω) DG180, DG183, DG186, DG189** (30Ω) DG181, DG184, DG187, DG190 CMOS DG300-DG308A, DG211 DG300A-DG307A, DG309, DG212

Bold Print = Recommended for the application

Analog Switches Selector Guide (Cont'd)

Application	Feature of Application	Important Parameters	Major Tradeoffs	Suggested Switches
Sample and Hold	1) Low Droop Rate	Low Leakage	Higher ON Resistance	**CMOS DG300A-DG307A, DG300, DG309 DG381A-DG390A** **CMOS DG300-DG308A, DG381-DG390, DG5040-DG5045** JFET DG180-DG191 CMOS DG211, DG200A, DG201A, DG202, DG212
	2) Low Sample to Hold Offset	Low Charge Coupling	Higher ON Resistance	**CMOS DG200A, DG201A, DG202, DG212, DG211** JFET DG181, DG182 (30Ω, 75Ω) DG184, DG185, DG187, DG188, DG190, DG191 CMOS DG300-DG308A, DG300A-DG307A, DG309
	3) Fast Acquisition Speed	Low ON Resistance	Higher Leakage Higher Charge Coupling	**JFET (10Ω) DG180, DG183, DG186, DG189** (30Ω, 75Ω) Remainder of DG181-DG191 Family CMOS DG300-DG307, DG381-DG390, DG300A-DG307A CMOS DG211, DG212 CMOS DG381A-DG390A, DG200A, DG201A, DG202
Switching to High Impedance Inputs	1) Low Error Voltage	Low Leakage		**CMOS DG300A-DG307A, DG381A-DG390A** **CMOS DG300-DG307, DG381-DG390, DG5040-DG5045, DG211, DG200A, DG201A, DG212**
	2) Low Switching Transient Error Voltage	Low Charge Coupling		**CMOS DG200A, DG201A, DG202, DG212** **CMOS DG211** DG300-DG307, DG381-DG390, DG300A-DG307A, DG381A-DG390A
Low Cost	1) Best Performance for Lowest Cost	Monolithic Good Switch Performance		**CMOS DG211, DG212, DG303, DG309, DG308A, DG300-DG307, DG5040-DG5045** DG381-DG390, DG200A, DG201A, DG202, DG300A-DG307A, DG243, DG381A-DG390A
Military System	1) Hi-Rel Specified			**BS9000** **JM38510/XXXXX**
Differential Signal Switching	1) Good Matching of Switch Parameters	Monolithic Switch		**CMOS DG300, DG302, DG303, DG304, DG243, DG306, DG307, DG308A, DG381, DG384, DG390, DG309** CMOS DG211, DG5040-DG5045, DG300A, DG302A, DG303A, DG304A, DG306A, DG307A, DG309, DG381A, DG384A, DG390A, DG200A, DG207A, DG202, DG212
	2) Low Thermocouple Offset Voltage	Drain and Source of FET Switch in Close Proximity on *Small Chip*	JFET Switches Not Monolithic	**JFET DG183, DG184, DG185**
		Low Power Dissipation on Switch Driver		**CMOS DG304, DG306, DG307, DG308A DG304A, DG309** DG300-DG303, DG300A-DG303A, DG306A, DG307A, DG381-DG390, DG381A-DG390A, DG309

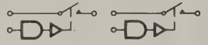
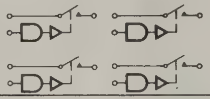
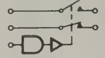
Bold Print = Recommended for the application

Analog Switches Selector Guide (Cont'd)

Application	Feature of Application	Important Parameters	Major Tradeoffs	Suggested Switches
Small Signal ($<1V$)	1) Low Noise (Channel)	Low $r_{DS(on)}$	Higher Leakages	**JFET (10Ω) DG180, DG183, DG186, DG189** (30Ω, 75Ω) Remainder of DG181-DG191 Family
	2) Low Charge Coupling			**CMOS DG300A-DG307A, DG309, DG381A-DG390A, DG212, DG308A** CMOS DG300-DG308, DG381-DG390, DG211
	3) High Impedance Inputs of Load	Low Leakage	Higher $r_{DS(on)}$	**CMOS DG300-DG308A, DG381-DG390, DG211, DG5040-DG5045, DG243, DG309** DG200-DG201 JFET DG181, DG182, DG184, DG185, DG187, DG188, DG190, DG191 CMOS DG300A-DG307A, DG309, DG381A-DG390A, DG212
	4) Low Thermocouple Offset Voltage	Low Power Switch		**CMOS DG304-DG307, DG304A-DG307A, DG381A-DG390A** DG300-DG303, DG381-DG390, DG300A-DG303A
		Drain and Source of FET Switch in Close Proximity on *Small Chip*		**JFET DG180-DG190 Family**
Multiplexing	1) Break-Before-Make Switching	t_{on} is Greater Than t_{off}		**CMOS DG506, DG506A, DG507, DG507A, DG508, DG508A, DG509, DG509A, DG528, DG529 (Latchable)**
	2) Binary Controlled Logic Inputs	Binary Decoding Stage on Chip		PMOS DG501, DG503
	3) Differential Multiplexing	Dual Switching Action		CMOS DG507, DG509, DG507A, DG509A, DG529
	4) D/A Conversion	Binary Weighted ON Resistance and Channel Resistance to Minimize Error		NMOS DG515, DG516

Bold Print = Recommended for the application

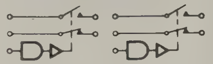
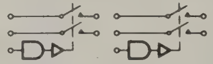
Analog Switches

Basic Part No. (Note 1)	Switch Type	Analog Voltage Range (V) (Note 4)	$r_{DS(on)}$ Max (Ω) (Note 4)	$I_{D(off)}$ (nA)	Switching Time (μsec)		Logic Levels (V)		Opt. Supply Voltage (V)				Comments	Switch Configuration
					t_{ON}	t_{OFF}	V_{INL}	V_{INH}	(+) Sup. V+	(−) Sup. V−	Logic Sup. V_L	Ref. Sup. V_R		
SINGLE CHANNEL SPST														
DG5040	Plus 40 CMOS	+ 15 to − 15	50	1	1.0	0.5	0.8	2	15	− 15	5	—	TTL Compatible	1 SPST Switch per Package
TWO CHANNEL SPST														
DG180	N-JFET	+ 10 to − 12.5	10	10	0.3	0.25	0.8	2.0	10	− 20	5	0	Break-Before-Make	
		+ 10 to − 7.5	10	10	0.3	0.26	0.8	2.0	15	− 15	5	0	15 V Supplies	
DG181	N-JFET	+ 10 to − 12.5	30	1	0.15	0.13	0.8	2.0	10	− 20	5	0	Break-Before-Make	
		+ 10 to − 7.5	30	1	0.15	0.13	0.8	2.0	15	− 15	5	0	15 V Supplies JAN/11101	
DG182	N-JFET	+ 10 to − 15	75	1	0.25	0.13	0.8	2.0	10	− 20	5	0	Break-Before-Make	
		+ 10 to − 10	75	1	0.25	0.13	0.8	2.0	15	− 15	5	0	15 V Supplies JAN/11102	**2 SPST Switches per Package**
DG200A	Plus 40 CMOS	+ 15 to − 15	70	2	1.0	0.5	0.8	2.4	15	− 15	—	—	TTL In	
DG281	N-JFET	+ 15 to − 15	300	0.2	0.15	0.13	0.8	2.0	15	− 15	5	0	Low Charge Injection	
DG300	CMOS	+ 15 to − 15	50	1	0.3	0.25	0.8	4.0	15	− 15	—	—	Low Power, TTL In JAN/11601	
DG300A	Plus 40 CMOS	+ 15 to − 15	50	1	0.3	0.25	0.8	4.0	15	− 15	—	—	Low Power, TTL In	
DG304	CMOS	+ 15 to − 15	50	1	0.25	0.15	3.5	11.0	15	− 15	—	—	Low Power, CMOS In JAN/11605	
DG304A	Plus 40 CMOS	+ 15 to − 15	50	1	0.25	0.15	3.5	11.0	15	− 15	—	—	Low Power, CMOS In	
DG381	CMOS	+ 15 to − 15	50	1	0.3	0.25	0.8	4.0	15	− 15	—	—	Low Power, DG181 Pin Out	
DG381A	Plus 40 CMOS	+ 15 to − 15	50	1	0.3	0.25	0.8	4.0	15	− 15	—	—	Low Power, DG181 Pin Out	
DG5041	Plus 40 CMOS	+ 15 to − 15	50	1	1.0	0.5	0.8	2.0	15	− 15	5	—	TTL Compatible	
FOUR CHANNEL SPST														
DG201A	Plus 40 CMOS	+ 15 to − 15	175	1	1.0	0.5	0.8	2.4	15	− 15	—	—	TTL In	**4 SPST Switches per Package**
DG202	Plus 40 CMOS	+ 15 to − 15	175	1	1.0	0.5	0.8	2.4	15	− 15	—	—	TTL In	
DG211	Plus 40 CMOS	+ 15 to − 15	175	5	0.5	0.4	0.8	2.4	15	− 15	5	—	Low Cost, TTL In	
DG212	Plus 40 CMOS	+ 15 to − 15	175	5	0.6	0.45	0.8	2.4	15	− 15	5	—	Low Cost, TTL In	
DG308A	Plus 40 CMOS	+ 15 to − 15	100	1	0.2	0.15	3.5	11.0	15	− 15	—	—	Low Cost CMOS In	
DG309	Plus 40 CMOS	+ 15 to − 15	100	5	0.2	0.15	3.5	11.0	15	− 15	—	—	Low Cost CMOS In	
ONE CHANNEL SPDT														
DG186	N-JFET	+ 10 to − 12.5	10	10	0.3	0.25	0.8	2.0	10	− 20	5	0	Break-Before-Make	
	N-JFET	+ 15 to − 7.5	10	10	0.3	0.25	0.8	2.0	15	− 15	5	0	15 V Supplies	
DG187	N-JFET	+ 10 to − 12.5	30	1	0.15	0.13	0.8	2.0	10	− 20	5	0	Break-Before-Make	
	N-JFET	+ 15 to − 7.5	30	1	0.15	0.13	0.8	2.0	15	− 15	5	0	15 V Supplies JAN/11105	
DG188	N-JFET	+ 10 to − 15	75	1	0.25	0.13	0.8	2.0	10	− 20	5	0	Break-Before-Make	
	N-JFET	+ 15 to − 10	75	1	0.25	0.13	0.8	2.0	15	− 15	5	0	15 V Supplies JAN/11106	**1 SPST Switch per Package**
DG287	N-JFET	+ 15 to − 7.5	300	0.2	0.15	0.13	0.8	2.0	15	− 15	5	0	Break-Before-Make	
DG301	CMOS	+ 15 to − 15	50	1	0.3	0.25	0.8	4.0	15	− 15	—	—	Low Power, TTL In JAN/11602	
DG301A	Plus 40 CMOS	+ 15 to − 15	50	1	0.3	0.25	0.8	4.0	15	− 15	—	—	Low Power, TTL In	
DG305	CMOS	+ 15 to − 15	50	1	0.25	0.15	3.5	11.0	15	− 15	—	—	Low Power, CMOS In JAN/11605	
DG305A	Plus 40 CMOS	+ 15 to − 15	50	1	0.25	0.15	3.5	11.0	15	− 15	—	—	Low Power, CMOS In	
DG387	CMOS	+ 15 to − 15	50	1	0.3	0.25	0.8	4.0	15	− 15	—	—	Low Power, DG187 Pin Out	
DG387A	Plus 40 CMOS	+ 15 to − 15	50	1	0.3	0.25	0.8	4.0	15	− 15	—	—	Low Power, DG187 Pin Out	
DG5042	Plus 40 CMOS	+ 15 to − 15	50	1	1.0	0.5	0.8	4.0	15	− 15	5	—	TTL Compatible	

NOTES:

1. The devices shown in **boldface** are recommended parts for new designs.
2. The appropriate switching characteristic for multiplexers is $t_{TRANSITION}$, not t_{ON}, t_{OFF}.
3. $V_{REF} = 1.5$ V is used when supply voltages < ± 15 V are used. Not needed when supply voltages of ± 15 are used.
4. Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail. Values shown are for temperature suffix A.
5. Device normally operates with resistor to + 10 V.

Analog Switches (Cont'd)

Basic Part No. (Note 1)	Switch Type	Analog Voltage Range (V) (Note 4)	$r_{DS(on)}$ Max (Ω) (Note 4)	$I_{D(off)}$ (nA)	Switching Time (μsec)		Logic Levels (V)		Opt. Supply Voltage (V)				Comments	Switch Configuration
					t_{ON}	t_{OFF}	V_{INL}	V_{INH}	(+) Sup. V+	(−) Sup. V−	Logic Sup. V_L	Ref. Sup. V_R		
TWO CHANNEL SPDT														
DG189	N-JFET	+10 to −12.5	10	10	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to −7.5	10	10	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies	
DG190	N-JFET	+10 to −12.5	30	1	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make JAN/11107	
	N-JFET	+15 to −7.5	30	1	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	
DG191	N-JFET	+10 to −15	75	1	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make JAN/11108	
	N-JFET	+15 to −10	75	1	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	**2 SPDT Switches per Package**
DG243	Plus 40 CMOS	+15 to −15	50	1	0.5	1.0	0.8	2.0	15	−15	5	—	Make-Before-Break (DG191 Pin Out)	
DG290	N-JFET	+15 to −7.5	300	0.2	0.15	0.13	0.8	2.0	15	−15	5	0	Break-Before-Make	
DG303	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In JAN/11604	
DG303A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In	
DG307	CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In JAN/11608	
DG307A	Plus 40 CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In	
DG390	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG190 Pin Out	
DG390A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG190 Pin Out	
DG5043	Plus 40 CMOS	+15 to −15	50	1	1.0	0.5	0.8	2.0	15	−15	5	—		
ONE CHANNEL DPST														
DG5044	Plus 40 CMOS	+15 to −15	50	1	1.0	0.5	0.8	2	15	−15	5	—	TTL Compatible	1 DPST Switch per Package
TWO CHANNEL DPST														
DG183	N-JFET	+10 to −12.5	10	10	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to −7.5	10	10	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies	
DG184	N-JFET	+10 to −12.5	30	1	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to −7.5	30	1	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	
DG185	N-JFET	+10 to −15	75	1	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	**2 DPST Switches per Package**
	N-JFET	+15 to −10	75	1	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	
DG284	N-JFET	+15 to −7.5	300	0.2	0.15	0.13	0.8	2.0	15	−15	5	0	Break-Before-Make	
DG302	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In	
DG302A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In	
DG306	CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In	
DG306A	Plus 40 CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In	
DG384	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG184 Pin Out	
DG384A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG184 Pin Out	
DG5045	Plus 40 CMOS	+15 to −15	50	1	1.0	0.5	0.8	2.0	15	15	5	—		

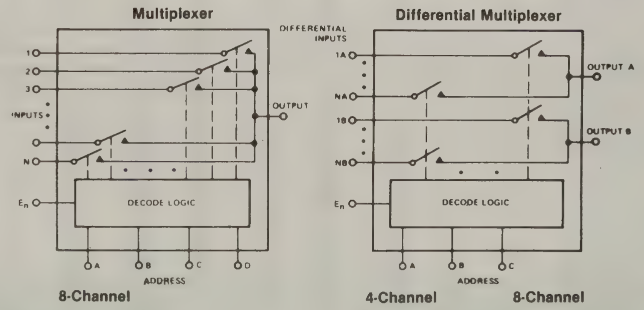
NOTES:

1. The devices shown in **boldface** are recommended parts for new designs.
2. The appropriate switching characteristic for multiplexers is $t_{TRANSITION}$, not t_{ON}, t_{OFF}.
3. $V_{REF} = 1.5$ V is used when supply voltages $< \pm 15$ V are used. Not needed when supply voltages of ± 15 are used.
4. Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail. Values shown are for temperature suffix A.
5. Device normally operates with resistor to + 10 V.

Multiplexers *and* Multiplexers with Input Latches

Basic Part No.	Process Type	Analog Voltage Range (V) (Note 4)	$r_{DS(on)}$ Max (Ω) (Note 4)	$I_{D(off)}$ (nA)	Transition Time (μsec) (Note 2)	Logic Levels (V) V_{INL}	Logic Levels (V) V_{INH}	Supply Voltage (V) (+) Sup. V+	Supply Voltage (V) (−) Sup. V−	Comments
EIGHT CHANNEL MUX + ENABLE										
DG501	PMOS	+5 to −5	150-240	8	1.5	0.6	3.5	5	−20	Logic Pullup Resistors
DG503	PMOS	+10 to −10	150-800	8	1.5	0.6	8.5	10	−20	
DG508A	Plus 40 CMOS	+10 to −15	400	10	1.0	0.8	2.4	15	−15	Break-Before-Make
DG528	Plus 40 CMOS	+15 to −15	400	10	1.0	0.8	2.4	+15	−15	Latches On Inputs
SIXTEEN CHANNEL MUX + ENABLE										
DG506A	Plus 40 CMOS	+15 to −15	400	10	1.0	0.8	2.4	15	−15	Break-Before-Make
FOUR CHANNEL DIFFERENTIAL MUX + ENABLE										
DG509A	Plus 40 CMOS	+15 to −15	400	10	1.0	0.8	2.4	15	−15	Break-Before-Make
DG529	Plus 40 CMOS	+15 to −15	400	10	1.0	0.8	2.4	15	−15	Latches On Inputs
EIGHT CHANNEL DIFFERENTIAL MUX + ENABLE										
DG507A	Plus 40 CMOS	+15 to −15	400	5	1.0	0.8	2.4	+15	−15	Break-Before-Make

Switch Configurations



NOTES:

1. The devices shown in **boldface** are recommended parts for new designs.
2. The appropriate switching characteristic for multiplexers is $t_{TRANSITION}$, not t_{ON}, t_{OFF}.
3. $V_{REF} = 1.5$ V is used when supply voltages < ±15 V are used. Not needed when supply voltages of ±15 are used.
4. Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail. Values shown are for temperature suffix A.
5. Device normally operates with resistor to +10 V.

Analog Switches Product Information

Drivers and Gates

Basic Part No. (Notes 1 & 2)	Switch Type	$r_{DS(on)}$ Max. (Ω) (Note 3)	Analog Voltage Range (p-p V) (Note 3)	Switching Time (µs)		Logic Input for ON Switch	Logic Levels (V)		Opt. Sup. Voltage (V)			Comments
				t_{ON}	t_{OFF}		V_{INL}	V_{INH}	(+) Sup. V_1	(−) Sup. V_2	Logic Sup. V_I	
One Channel SPST												
DG5040	CMOS Plus-40	50	30	1.0	0.5	1	0.8	2.0	15	−15	5	
Two Channel SPST												
DGM111	PMOS	75-200	20	0.3	1.0	0	0.5	4.6	10	−20	5	
DG133	N-JFET	30	20	0.6	1.6	1	0.8	2.5	12	−18	—	See DG181 For New Design
DG134	N-JFET	80	20	0.6	1.6	1	0.8	2.5	12	−18	—	See DG182 For New Design
DG141	N-JFET	10	20	1.0	2.5	1	0.8	2.5	12	−18	—	See DG180 For New Design
DG151	N-JFET	15	15	1.0	2.5	1	0.8	2.5	15	−15	—	See DG180 For New Design
DG152	N-JFET	50	15	0.8	1.6	1	0.8	2.5	15	−15	—	See DG181 For New Design
DG180	N-JFET	10	20	0.3	0.25	0	0.8	2.0	10	−20	5	Break-Before-Make
		10	15	0.3	0.25	0	0.8	2.0	15	−15	5	15 V Supplies
***DG181**	N-JFET	30	20	0.15	0.13	0	0.8	2.0	10	−20	5	Break-Before-Make
		30	15	0.15	0.13	0	0.8	2.0	15	−15	5	15 V Supplies
***DG182**	N-JFET	75	20	0.25	0.13	0	0.8	2.0	10	−20	5	Break-Before-Make
		75	20	0.25	0.13	0	0.8	2.0	15	−15	5	15 V Supplies
***DG200A**	CMOS Plus-40	70	30	1.0	0.5	0	0.8	2.4	15	−15	—	
DG281	N-JFET	300	20	0.15	0.13	0	0.8	2.0	15	−15	5	Break-Before-Make
***DG300**	CMOS	50	30	0.300	0.250	1	0.8	4.0	15	−15	—	
***DG381**	CMOS	50	30	0.300	0.250	0	0.8	4.0	15	−15	—	
***DG304**	CMOS	50	30	0.250	0.150	1	3.5	11.0	15	−15	—	CMOS compatible
***DG5041**	CMOS Plus-40	50	30	1.0	0.5	1	0.8	2.0	15	−15	5	Break-Before-Make
Four Channel SPST												
***DG172**	PMOS	150-450	20	0.3	0.75	0	0.8	2.0	10	−20	5	
***DG201A**	CMOS Plus-40	175	30	0.6	0.45	0	0.8	2.4	15	−15	—	
DG201HS	CMOS Plus-40	50	30	.05	.04				15	-15		Super Fast Switch with input latches
DG221	CMOS Plus-40	100	30						15	-15		
***DG202**	CMOS Plus-40	175	30	0.6	0.45	1	0.8	2.4	15	−15	—	
***DG211**	CMOS Plus-40	175	30	1.0	0.5	0	0.8	2.4	15	−15	5	
***DG212**	CMOS Plus-40	175	30	1.0	0.5	1	0.8	2.4	15	−15	5	
***DG308A**	CMOS Plus-40	100	30	0.2	0.15	1	3.5	11.0	15	−15	—	Single Supply Operation
***DG309**	CMOS Plus-40	100	30	0.2	0.15	0	3.5	11.0	15	−15	—	Single Supply Operation
Five Channel SPST												
DG125	PMOS	100-450	20	0.3	2.0	0	0.5	4.6	10	−20	5	
One Channel SPDT												
DG143	N-JFET	80	20	0.8	1.6	(Note 4)	2.0	3.0	12	−18	—	See DG188 For New Design
DG144	N-JFET	30	20	0.8	1.6	(Note 4)	2.0	3.0	12	−18	—	See DG187 For New Design
DG146	N-JFET	10	20	1.0	2.5	(Note 4)	2.0	3.0	12	−18	—	See DG186 For New Design
DG161	N-JFET	15	15	1.0	2.5	(Note 4)	2.0	3.0	15	−15	—	See DG186 For New Design
DG162	N-JFET	50	15	0.8	1.6	(Note 4)	2.0	3.0	15	−15	—	See DG187 For New Design
DG186	N-JFET	10	20	0.3	0.25	(Note 5)	0.8	2.0	10	−20	5	Break-Before-Make
	N-JEFT	10	15	0.3	0.25	(Note 5)	0.8	2.0	15	−15	5	15 V Supplies
***DG187**	N-JFET	30	20	0.15	0.13	(Note 5)	0.8	2.0	10	−20	5	Break-Before-Make
	N-JFET	30	15	0.15	0.13	(Note 5)	0.8	2.0	15	−15	5	15 V Supplies
***DG188**	N-JFET	75	20	0.25	0.13	(Note 5)	0.8	2.0	10	−20	5	Break-Before-Make
	N-JFET	75	20	0.25	0.13	(Note 5)	0.8	2.0	15	−15	5	15 V Supplies
DG287	N-JFET	300	20	0.15	0.13	(Note 5)	0.8	2.0	15	−15	5	Break-Before-Make

*Devices recommended for new designs are indicated in **bold face** type.

Analog Switches Product Information (Cont'd)

Drivers and Gates (Cont'd)

Basic Part No. (Notes 1 & 2)	Switch Type	$r_{DS(on)}$ Max. (Ω) (Note 3)	Analog Voltage Range (p-p V) (Note 3)	Switching Time (μs)		Logic Input for ON Switch	Logic Levels (V)		Opt. Sup. Voltage (V)			Comments
				t_{ON}	t_{OFF}		V_{INL}	V_{INH}	(+) Sup. V_1	(−) Sup. V_2	Logic Sup. V_l	
One Channel SPDT (Cont'd)												
***DG301**	CMOS	50	30	0.300	0.250	(Note 5)	0.8	4.0	15	−15	—	
***DG387**	CMOS	50	30	0.300	0.250	(Note 5)	0.8	4.0	15	−15	—	
***DG305**	CMOS	50	30	0.250	0.150	(Note 5)	3.5	11.0	15	−15	—	CMOS compatible
SI3002	PMOS	100-400	20	1.0	1.5	(Note 5)	0.8	2.0	10	−20	—	
***DG5042**	CMOS Plus-40	50	30	1.0	0.5	(Note 5)	0.8	2.0	15	−15	5	Break-Before-Make
Two Channel SPDT												
DG189	N-JFET	10	20	0.3	0.25	(Note 5)	0.8	2.0	10	−20	5	Break-Before-Make
	N-JFET	10	15	0.3	0.25	(Note 5)	0.8	2.0	15	−15	5	15V Supplies
***DG190**	N-JFET	30	20	0.15	0.13	(Note 5)	0.8	2.0	10	−20	5	Break-Before-Make
	N-JFET	30	15	0.15	0.13	(Note 5)	0.8	2.0	15	−15	5	15V Supplies
***DG191**	N-JFET	75	20	0.25	0.13	(Note 5)	0.8	2.0	10	−20	5	Break-Before-Make
	N-JFET	75	20	0.25	0.13	(Note 5)	0.8	2.0	15	−15	5	15V Supplies
***DG243**	CMOS Plus-40	50	30	1.0	0.5	(Note 5)	0.8	2.0	15	−15	5	Make-Before-Break
DG290	N-JFET	300	20	0.15	0.13	(Note 5)	0.8	2.0	15	−15	5	Break-Before-Make
***DG303**	CMOS	50	30	0.300	0.250	(Note 5)	0.8	4.0	15	−15	—	
***DG390**	CMOS	50	30	0.300	0.250	(Note 5)	0.8	4.0	15	−15	—	
***DG307**	CMOS	50	30	0.250	0.150	(Note 5)	3.5	11.0	15	−15	—	CMOS compatible
***DG5043**	CMOS Plus-40	50	30	1.0	0.5	(Note 5)	0.8	2.0	15	−15	5	Break-Before-Make
One Channel DPST												
***DG5044**	CMOS Plus-40	50	30	1.0	0.5	(Note 5)	0.8	2.0	15	−15	5	Break-Before-Make
Two Channel DPST												
DG126	N-JFET	80	20	0.6	1.6	1	0.8	2.5	12	−18	—	See DG185 For New Design
DG129	N-JFET	30	20	0.6	1.6	1	0.8	2.5	12	−18	—	See DG184 For New Design
DG140	N-JFET	10	20	1.0	2.5	1	0.8	2.5	12	−18	—	See DG183 For New Design
DG153	N-JFET	15	15	1.0	2.5	1	0.8	2.5	15	−15	—	See DG183 For New Design
DG154	N-JFET	50	15	0.6	1.6	1	0.8	2.5	15	−15	—	See DG185 For New Design
DG183	N-JFET	10	20	0.3	0.25	1	0.8	2.0	10	−20	5	Break-Before-Make
	N-JFET	10	15	0.3	0.25	1	0.8	2.0	15	−15	5	15V Supplies
***DG184**	N-JFET	30	20	0.15	0.13	1	0.8	2.0	10	−20	5	Break-Before-Make
	N-JFET	30	15	0.15	0.13	1	0.8	2.0	15	−15	5	15V Supplies
***DG185**	N-JFET	75	20	0.25	0.13	1	0.8	2.0	10	−20	5	Break-Before-Make
	N-JFET	75	20	0.25	0.13	1	0.8	2.0	15	−15	5	15V Supplies
DG284	N-JFET	300	20	0.15	0.13	1	0.8	2.0	15	−15	5	Break-Before-Make
***DG302**	CMOS	50	30	0.300	0.250	1	0.8	4.0	15	−15	—	
***DG384**	CMOS	50	30	0.300	0.250	1	0.8	4.0	15	−15	—	
***DG306**	CMOS	50	30	0.250	0.150	1	3.5	11.0	15	−15	—	CMOS compatible
***DG5045**	CMOS Plus-40	50	30	1.0	0.5	1	0.8	2.0	15	−15	5	Break-Before-Make
One Channel DPDT												
DG139	N-JFET	30	20	0.8	1.6	(Note 4)	2.0	3.0	12	−18	—	See DG191 For New Design
DG142	N-JFET	80	20	0.8	1.6	(Note 4)	2.0	3.0	12	−18	—	See DG190 For New Design
DG145	N-JFET	10	20	1.0	2.5	(Note 4)	2.0	3.0	12	−18	—	See DG189 For New Design
DG163	N-JFET	15	15	1.0	2.5	(Note 4)	2.0	3.0	15	−15	—	See DG189 For New Design
DG164	N-JFET	50	15	0.8	1.6	(Note 4)	2.0	3.0	15	−15	—	See DG191 For New Design
Eight Channel MUX + Enable												
DG501	PMOS	150-250	10	1.5	(Note 8)	(Note 7)	0.6	3.5	5	−20	—	Logic Pullup Resistors
DG503	PMOS	150-800	20	1.5	(Note 8)	(Note 7)	0.6	8.5	10	−20	—	

*Devices recommended for new designs are indicated in **bold face** type.

Analog Switches Product Information (Cont'd)

Drivers and Gates (Cont'd)

Basic Part No. (Notes 1 & 2)	Switch Type	$r_{DS(on)}$ Max. (Ω) (Note 3)	Analog Voltage Range (p-p V) (Note 3)	Switching Time (μs)		Logic Input for ON Switch	Logic Levels (V)		Opt. Sup. Voltage (V)			Comments
				t_{ON}	t_{OFF}		V_{INL}	V_{INH}	(+) Sup. V_1	(−) Sup. V_2	Logic Sup. V_l	
Eight Channel MUX + Enable (Cont'd)												
***DG508A**	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	−15	—	
***DG528**	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	−15	—	With Input Latches
SI3705	PMOS	150-400	10	1.5	(Note 8)	(Note 7)	0.6	3.5	5	−20	—	See DG501/No Pullup Resistors
Sixteen Channel MUX + Enable												
***DG506A**	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	−15	—	Break-Before-Make
Four Channel Differential MUX												
***DG509A**	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	−15	—	Break-Before-Make
***DG529**	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	−15	—	With Input Latches
Eight Channel Differential MUX + Enable												
***DG507A**	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	−15	—	Break-Before-Make
Four Channel SPDT D/A Converter Summing Node Switches												
DG515	NMOS	See Comments	—	0.120	0.170	(Note 5)	0.5	7.5	8.0	0	—	$R_1 = 6.25\Omega$, $R_2 = 12.5\Omega$, $R_3 = 25\Omega$, $R_4 = 50\Omega$
Ten Channel SPDT D/A Converter Summing Node Switches												
DG516	NMOS	See Comments	—	0.120	0.170	(Note 5)	0.5	7.5	8.0	0	—	$R_1 = 100\Omega$, $R_2 = 200\Omega$ $R_3 = 400\Omega$, $R_4 = 800\Omega$ $R_5 = 1600\Omega$ $R_{6-10} = 3200\Omega$

Multiple FET Switches

Siliconix P-Channel MOSFET & DMOS Switches are available for such applications as sequential switching (commutation), signal processing, modulation, and A-to-D conversion. The MOSFET is normally OFF. These devices are also available with Siliconix drivers in a single package.

Basic Part Number (Note 2)	Circuit Function			Switch Type	Pull Up On Gate	r_{DS} Max. (V)		BV_{DSS}	$I_{S(off)}$ (nA)	$V_{GS(th)}$		C_{gs} Typ. (pF)	C_{ds} Typ. (pF)	C_{sb} Typ. (pF)
	SOURCES	DRAINS	GATES			@ $V_S = +10V$	@ $V_S = -10V$			Min.	Max.			
G115	6	1	6	SP6T	Yes	100	450	−30	0.5	−1.5	−4.0	0.9	0.4	2
G118	6	1	8	SP6T	No	100	450	−30	0.5	−1.5	−4.0	0.9	0.4	2
G119	6	2	3	DP3T	Yes	100	450	−30	0.5	−1.5	−4.0	1.8	0.4	2
G122	4	2	2	DPDT	Yes	100	450	−30	0.5	−1.5	−4.0	1.8	0.4	2
G123	4	2	4	2 × SPDT	Yes	100	450	−30	0.5	−1.5	−4.0	1.8	0.4	2
***SD5000**	4	4	4	4 × SPST	No	50		20	10.0	0.1	2.0	3.5	0.5	4
***SD5001**	4	4	4	4 × SPST	No	50		10	10.0	0.1	2.0	3.5	0.5	4
***SD5002**	4	4	4	4 × SPST	No	50		15	10.0	0.1	2.0	3.5	0.5	4
***SD5200**	4	4	4	4 × SPST	No	80		30	1000	0.5	2.0	3.5	0.5	4

*Devices recommended for new designs are indicated in **bold face** type.

Drivers for MOS FET Switches

These drivers were designed to function as a level shifter and buffer between low level logic and the control gate of FET analog switches. Output voltage ratings are as high as 50V.

Basic Part Number (Note 2)			Function and Uses	at Rated Current(s)	OFF Level $V_{(OUT)OFF}$ at Rated Current or $I_{(OUT)OFF}$ at Rated Voltage	Input Logic for V_{OUT} (low)	V_{INL} (V)	V_{INH} (V) (I_{INH}) (mA)	Optimum Supply Voltage (V)				Switching Time,(μs)	
									V_1	V_2	V_L	V_R	t_{ON}	t_{OFF}
D125	6	6	Six Separate MOSFET Drivers	0.4V@5mA	0.1μA@10V	0	0.5	4.6	(Note 9)	-20	5	–	0.5	1.2
D129	7	4	Four Channel (BV = 50) MOSFET Driver with Decode	0.7V@10mA	0.1μA@10V	1	0.7	2.2	(Note 9)	-20	–	–	0.25	0.8
***D169**	2	4	Dual High-Speed Drivers with Complementary Outputs designed to drive high-capacity loads.	1.2V@1mA 3.0V@40mA	1.1V@1mA 2.5V@40mA		0.8 0.8	2.0 2.0	15 15	-15 -15	5 5	0 0	t_d+ 0.17 0.17	t_d- 0.20 0.20
				V_{OH}	V_{OL}									
D469	4	4	Quad High Speed Driver	V_{DD} -2.0V @200mA V_{DD} -0.2V @10mA	2.0V@200mA 0.2V@10mA	1	0.8	2.0	+12V, GND				0.045	
Si7250	4	8	Quad High Speed Driver	V_{DD} -2.0V @200mA V_{DD} -0.2V @10mA	2.0V@200mA 0.2V@10mA	Output & Complement Available	0.8	2.0	+12V, GND				0.150	

Pulse Width Modulators

Basic Part Number (Note 2)	Function and Uses	Operating Freq.	V_{OL} @ Rated Current	V_{OH} @ Rated Current	Supply Voltage
PWM25	Pulse Width Modulator for SMPS to drive NPN or N channel MOSPOWER Devices	10Hz-400kHz with Dead Time Adjust	0.4V @ 20mA 2.5V @ 100mA	V+ –2V@20mA V+ –3V@100mA	+8.5V to +35V
PWM27	Pulse Width Modulator for S SMPS to drive PNP or P channel MOSPOWER Devices	10Hz-400kHz with Dead Time	0.4V @ 20mA 2.5V @ 100mA	V+ –2V@20mA V+ –3V@100mA	+8.5V to +35V
PWM125	Pulse Width Modulator for SMPS to drive N channel MOSPOWER Devices	10Hz - 800kHz with 100ns Dead Time	0.4V @ 20mA 2.5V @ 100mA	V+ –2V@20mA V+ –3V@100mA	+8.5V to +35V
PWM127	Pulse Width Modulators for SMPS to drive P channel MOSPOWER Devices	10Hz - 800kHz with 100ns Dead	0.4V @ 20mA 2.5V @ 100mA	V+ –2V@20mA V+ –3V@100mA	+8.5V to +35V

Voltage Converters

Basic Part Number (Note 2)	Function and Uses	Voltage Range	Quiescent Current	Output Voltage	Output Voltage @ Output Current
Si7661	Voltage Doubler/Inverter	+4.5V to +20V	2mA Max	–20V to +20V	–18V to +18V @ 20mA

NOTES:

(1) *Devices recommended for new designs are indicated in **bold face** type.
(2) See pages 7-26 through 7-28 for package and temperature designations for most products.
(3) Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail.
(4) Input reference voltage of 2.5V is required (see data sheets).
(5) See data sheet for switch state of differential switches.
(6) Current Driven Device I_{INH} = 1mA.
(7) For truth table see data sheet.
(8) The appropriate switching characteristic for multiplexers is $t_{TRANSTION}$, not t_{ON}, t_{OFF}.
(9) Device normally operates with resistor — to +10V.
(10) (C_L = 35pF).

LSI/Linear Product Information

A/D Converters

3½-Digit High Performance	**LD110/LD111A** 16-pin plastic DIPs	±3½-Digit A/D Converter Accuracy 0.02% ±1 count Auto zero Auto polarity 10μV resolution Typical T.C. of 5 ppm/°C A usable 20mV scale	Three voltage ranges: 1.999V, 199.9mV & 19.99mV Sampling rate up to 40 samples/s Differential input capability Over-range & under-range signals TTL compatible
4½-Digit	**LD120/121A** 16- & 18- pin plastic DIP respectively	±4½-Digit A/D Converter Accuracy 0.005% ±1 count Auto zero Auto polarity TTL compatible Internal clock Linear to 28,500 counts	Two voltage ranges: 2.0V & 200.00mV 1 to 5 samples/s 25% inter-digit blanking MUX BCD outputs 0.5 count stability on 2.0V range Monolithic design
4½-Digit	**LD122/LD121A** 16- & 18- pin plastic DIP respectively	±4½-Digit A/D Converter Accuracy 0.005% ±1 count 1μV resolution for 20 mV FS Auto zero Auto polarity TTL compatibility Internal clock Linear to 28,500 counts	MUX BCD outputs Two over-range outputs, under-range, blink inhibit and convert-on-command capability Interfaces to external circuitry and microprocessors

Micropower Linears

Triple Op Amp	**L144** 14-pin plastic, ceramic, flat-pack & Dice	±1.5 to ±18V supply Programmable supply current Internally compensated 0.4V/μs slew rate	80dB gain with 20kΩ load Drives large capacitive loads ±30V differential input Monolithic construction
Quad Comparator	**L161** 16-pin plastic, ceramic, flat-pack & Dice	±1.5 to ±18V supply Single supply operation Programmable supply current 3V/μs slew rate	Gain greater than 20V/mV Sensing near ground ±30V differential input CMOS Logic compatible

Telecommunications Products

Loop Disconnect Dialer (pulse dialer)	**DF320** 18-lead plastic & CERDIP		Operation from 2.5V to 5V supply Low standby power dissipation; 3μW Low dynamic power consumpion; 600μW On-chip oscillator for 3.579545 MHz crystal Redial capability Hold capability delays impulsing Post-impulsing pause of 33 ms Mask during impulsing and inter-digit pause Selectable make-break ratio 10, 16, 20, 932 Hz impulsing rates Inter-digital pause of 800 ms

LSI/Linear Product Information (Cont'd)

Loop Disconnect Dialer (pulse dialer) (Cont'd)	**DF320A**		Same as DF320, except post-impulsing pause of 500ms
	DF322		Same as DF320, except mask during impulsing only
	DF328 16-lead plastic		Same as DF320, except 10, 932Hz impulsing rates No hold capability during impulsing
	DF820 18-lead plastic		Number entry without impulsing, last number redial up to 24 digits, dial and redial of internal PABX calls whilst maintaining last external call for redial later. Indefinite digit storage, Number entry > 24 digits allowed but no redial, Reset delay allows line breaks to be ignored, single and double contact keypad interface, multiple mute and dial pulse outputs, on chip regulator.

Interface

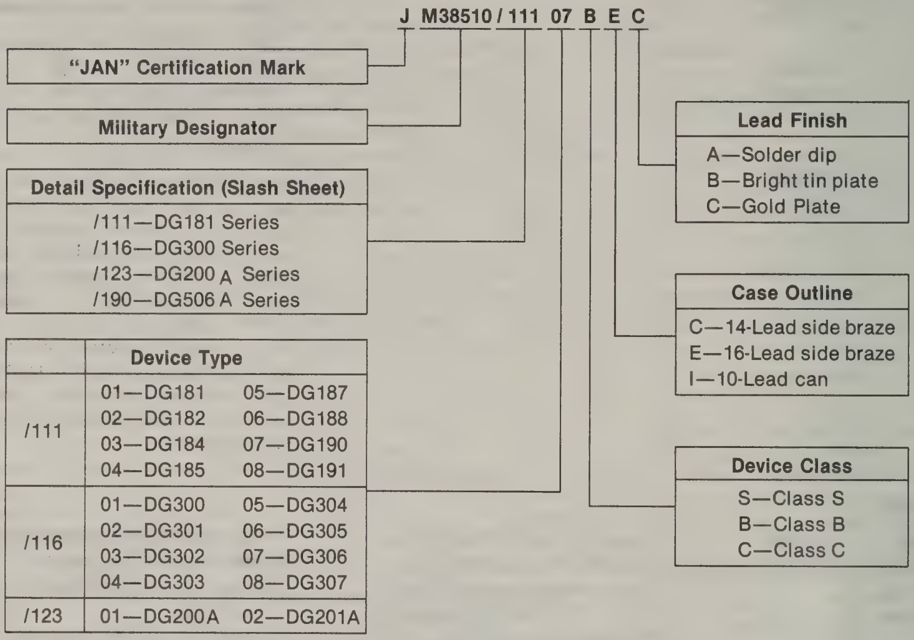
Four-digit MUX'd BCD to LCD Display Driver	**DF412** 40-pin plastic	Decodes MUX BCD to LCD 4-Digit drive capability Low power consumption TTL, DTL, CMOS compatible Can be ganged to drive more than 4 digits	7-segment LCD drive signals Drives large LCDs easily Can be clocked using an external oscillator Internal oscillator available

Analog Switches

JAN 38510

Several Siliconix Analog Switches are available fully certified on the QPL (Qualified Parts List) published monthly by Defense Electronics Supply Center (DESC). The QPL numbers follow this format: JM38510/XXXXX. Refer to the current Siliconix Price List for available part types and order numbers.

JAN Part Numbering System



J M38510 / 111 07 B E C

"JAN" Certification Mark

Military Designator

Detail Specification (Slash Sheet)

/111—DG181 Series
/116—DG300 Series
/123—DG200 A Series
/190—DG506 A Series

	Device Type	
/111	01—DG181	05—DG187
	02—DG182	06—DG188
	03—DG184	07—DG190
	04—DG185	08—DG191
/116	01—DG300	05—DG304
	02—DG301	06—DG305
	03—DG302	07—DG306
	04—DG303	08—DG307
/123	01—DG200A	02—DG201A

Lead Finish

A—Solder dip
B—Bright tin plate
C—Gold Plate

Case Outline

C—14-Lead side braze
E—16-Lead side braze
I—10-Lead can

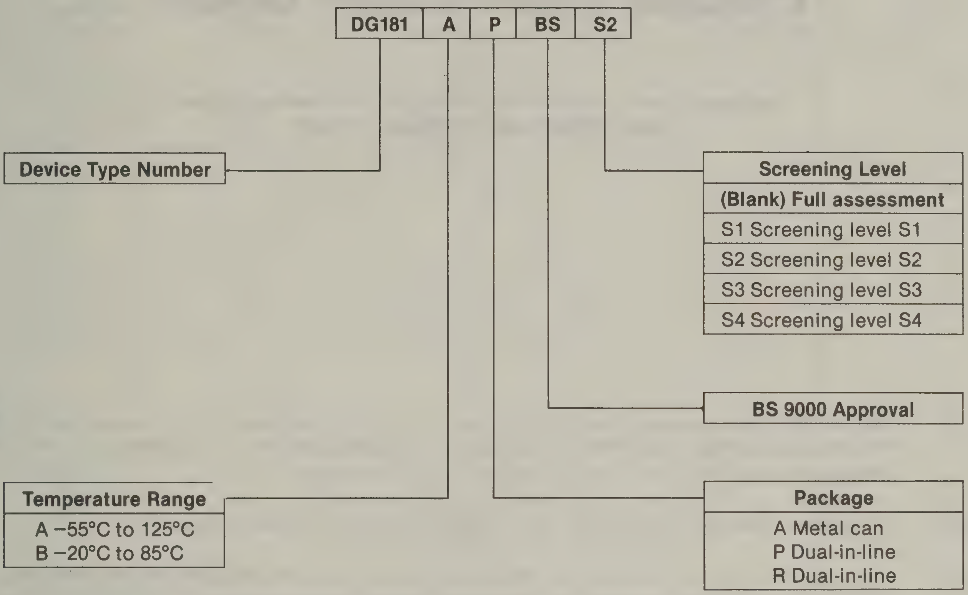
Device Class

S—Class S
B—Class B
C—Class C

Part Number	Order Part Number	Generic Part Number
JM38510/11101BCC	SJM181BCC	DG181AP/883
JM38510/11101BIC	SJM181BIC	DG181AA/883
JM38510/11102BCC	SJM182BCC	DG182AP/883
JM38510/11102BIC	SJM182BIC	DG182AA/883
JM38510/11103BEC	SJM183BEC	DG184AP/883
JM38510/11104BEC	SJM185BEC	DG185AP/883
JM38510/11105BCC	SJM187BCC	DG187AP/883
JM38510/11105BIC	SJM187BIC	DG187AA/883
JM38510/11106BCC	SJM188BCC	DG188AP/883
JM38510/11106BIC	SJM188BIC	DG188AA/883
JM38510/11107BEC	SJM190BEC	DG190AP/883
JM38510/11108BEC	SJM191BEC	DG191AP/883
JM38510/11601BCC	SJM300BCC	DG300AP/883
JM38510/11601BIC	SJM300BIC	DG300AA/883
JM38510/11602BCC	SJM301BCC	DG301AP/883
JM38510/11602BIC	SJM301BIC	DG301AA/883
JM38510/11603BCC	SJM302BCC	DG302AP/883
JM38510/11604BCC	SJM303BCC	DG303AP/883
JM38510/11605BCC	SJM304BCC	DG304AP/883
JM38510/11605BIC	SJM304BIC	DG304AA/883
JM38510/11606BCC	SJM305BCC	DG305AP/883
JM38510/11606BIC	SJM305BIC	DG305AA/883
JM38510/11607BCC	SJM306BCC	DG306AP/883
JM38510/11608BCC	SJM307BCC	DG307AP/883
JM38510/12303BCC	SJM200BCC	DG200A AP/883
JM38510/12303BIC	SJM200BIC	DG200A AA/883
JM38510/12304BEC	SJM201BEC	DG201A AP/883

Analog Switches
BS9000

BS9000 Part Numbering System



Approved Parts		
Generic Part No.	Generic Part No.	Generic Part No.
DG126/ /BS	DG180/ /BS	DG300A /BS
DG129/ /BS	DG181/ /BS	DG301A /BS
DG133/ /BS	DG182/ /BS	DG302A /BS
DG134/ /BS	DG183/ /BS	DG303A /BS
DG139/ /BS	DG184/ /BS	DG304A /BS
DG140/ /BS	DG185/ /BS	DG305A /BS
DG141/ /BS	DG186/ /BS	DG306A /BS
DG142/ /BS	DG187/ /BS	DG307A /BS
DG143/ /BS	DG188/ /BS	DG308A /BS
DG144/ /BS	DG189/ /BS	DG381A /BS
DG145/ /BS	DG190/ /BS	DG384A /BS
DG146/ /BS	DG191/ /BS	DG387A /BS
DG151/ /BS	DG200A /BS	DG390A /BS
DG152/ /BS	DG201A /BS	
DG153/ /BS	DG501/ /BS	
DG154/ /BS	DG503/ /BS	
DG161/ /BS	DG506A /BS	
DG162/ /BS	DG507A /BS	
DG163/ /BS	DG508A /BS	
DG164/ /BS	DG509A /BS	
	SI3705/ /BS	

*Contact one of the Silixonix sales offices for latest information.

Process Option Flow Chart

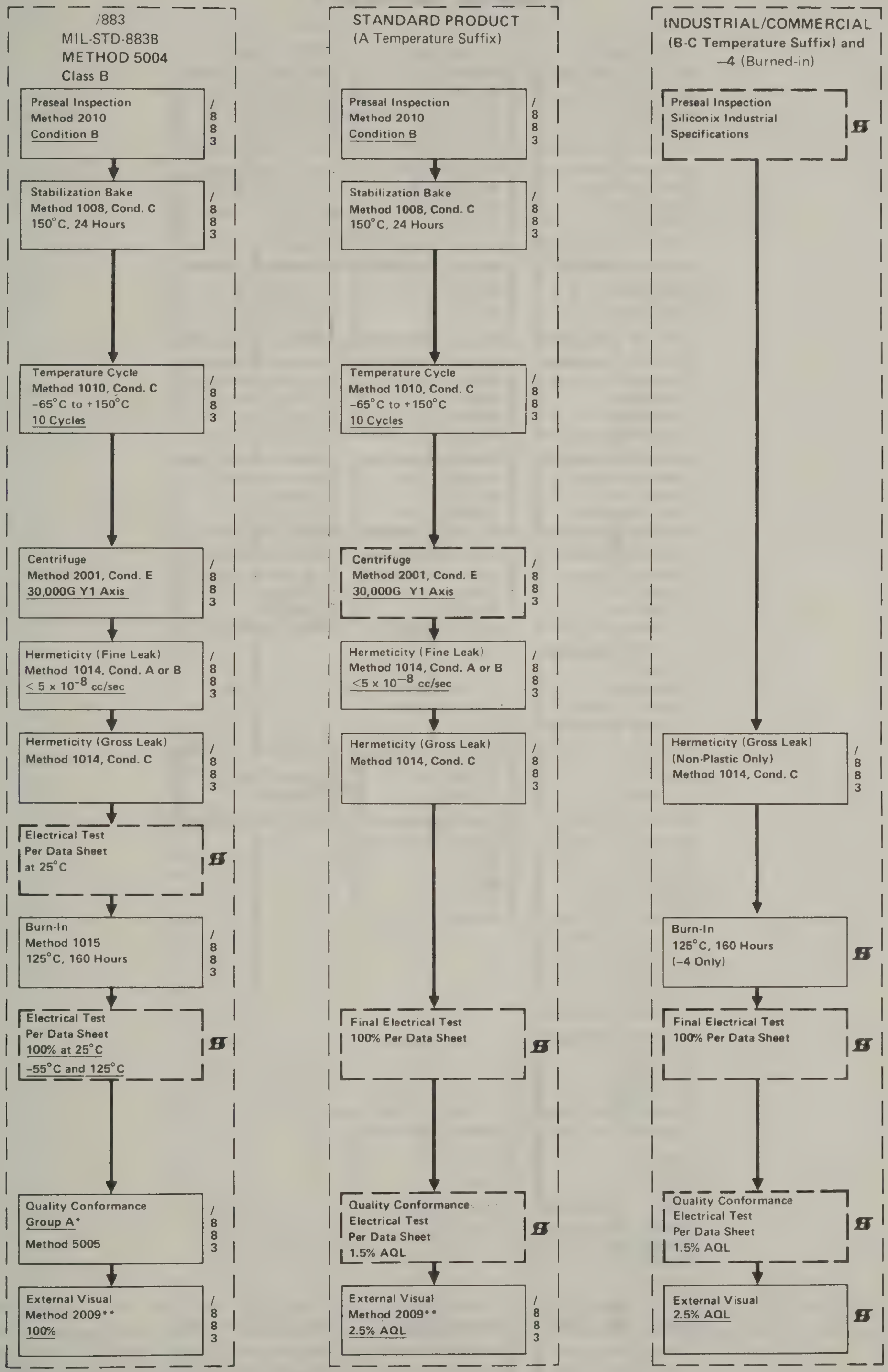
The Process Option Flow Chart shows the standard screening options provided by Siliconix for Integrated Circuits

Column 1: Denotes the screening process for MIL-883, Class B. To order a part screened to this option, add a "/883" following the package suffix letter. If Group B or C Quality Conformance is also required, call out as a separate line item. Parts in this classification are carried in inventory.

Column 2: Is the screening procedure for military grade standard products ("A" temperature suffix).

Column 3: Is the normal screening procedure for industrial and commercial grade products (B and C temperature suffixes). An industrial and commercial grade product (B and C temperature range) may be given a 160 hour burn-in at 125°C by adding a Dash 4 (–4) following the package suffix letter.

Process Option Flow Chart



*Group B and C tests done to customer order on /883 parts

**Physical Dimensions Excluded

The latest revision of MIL-STD-883 is applicable

Introduction 1

Data Sheets 2

Selector Guides 3

Geometry 4

Application Notes 5

Appendices 6

Other Products 7

Worldwide Sales Offices

8

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